GBT-SCA Updates

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(alphabetic order)

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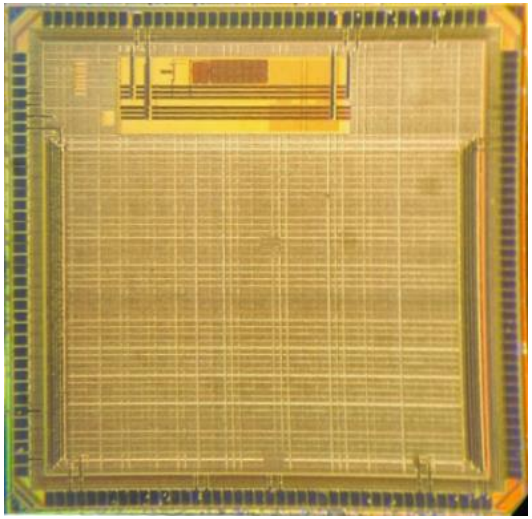
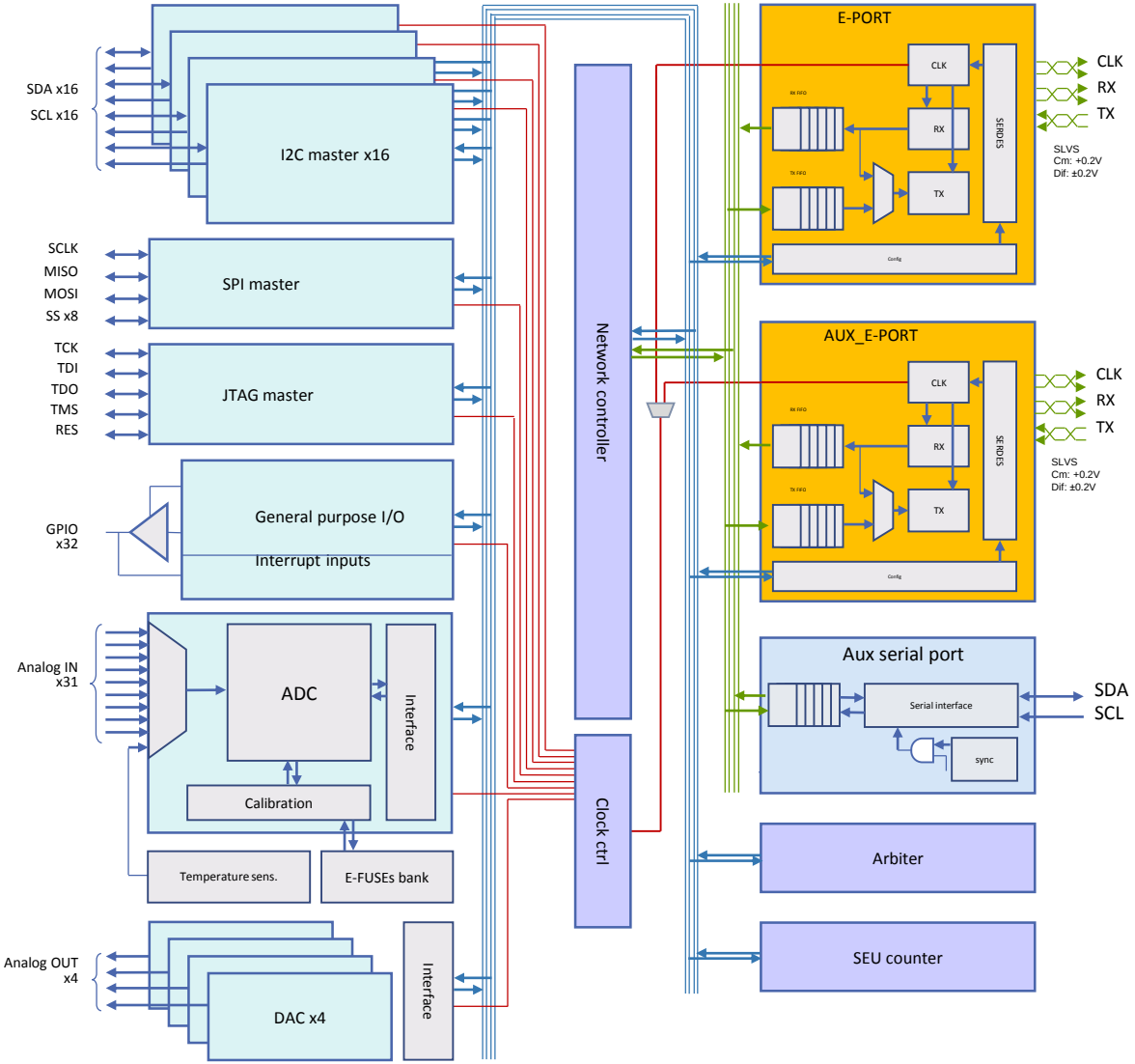
CERN

GBT-SCA




SDA x16
SCL x16
I2C master x16
SCLK
MISO
MOSI
SS x8
SPI master
TCK
TDI
TDO
TMS
RES
JTAG master
GPIO x32
General purpose I/O
Interrupt inputs
Analog IN x31
ADC
Interface
Calibration
Temperature sens.
E-FUSEs bank
Analog OUT x4
DAC x4
Interface
Network controller
Clock ctrl
E-PORT
CLK
RX
TX
SERDES
SLVS
Cm: +0.2V
Dif: ±0.2V
AUX_E-PORT
CLK
RX
TX
SERDES
SLVS
Cm: +0.2V
Dif: ±0.2V
Aux serial port
Serial interface
sync
SDA
SCL
Arbiter
SEU counter

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Changes of the GBT-SCA V2

- A new version of the SCA was prototyped in October 2015 with minor changes
- Improved ADC performances
  - The ADC of the SCA was modified to improve the TID tolerance
  - Better linearity, better noise performances,
- Allowed higher voltages supply for the periphery VDD
- Minor changes on the I2C masters
  - The SDA line can now be tristate

E-port communication

Status:

- Start-up and communication ← Tested
- Connect and reset commands ← Tested
- Switching between primary and auxiliary port ← Tested

Core Logic

Status:

- Digital functionalities ← Tested
- Receive/Reply and communication related ← Tested
- Enable/Disable (clk gating) of all communication interfaces ← Tested

I2C ports

Status:

- Read operations in 7bit addressing mode ← Tested
- Read operations in 10bit addressing mode ← Tested
- Write operations in 7bit addressing mode ← Tested
- Write operations in 10bit addressing mode ← Tested

SPI port

Status:

- Read and write operations with different settings and frequencies ← Tested
- Read and write operations on commercial hardware (memory) ← Tested

JTAG port

Status:

- Operations with different settings and frequencies ← Tested

GPIO port

- Parallel port as output ← Tested
- Parallel port as input/tristate ← Tested

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ADC

- Conversion operation and reply on all the 31 inputs ← Tested
- Crosstalk between the 31 Inputs ← Tested
- Gain Calibration logic ← Tested
- Internal temperature sensor ← Tested
- 100 µA Current sources on the ADC pads ← Tested
- Offset ← Tested

ADC Differential Nonlinearity

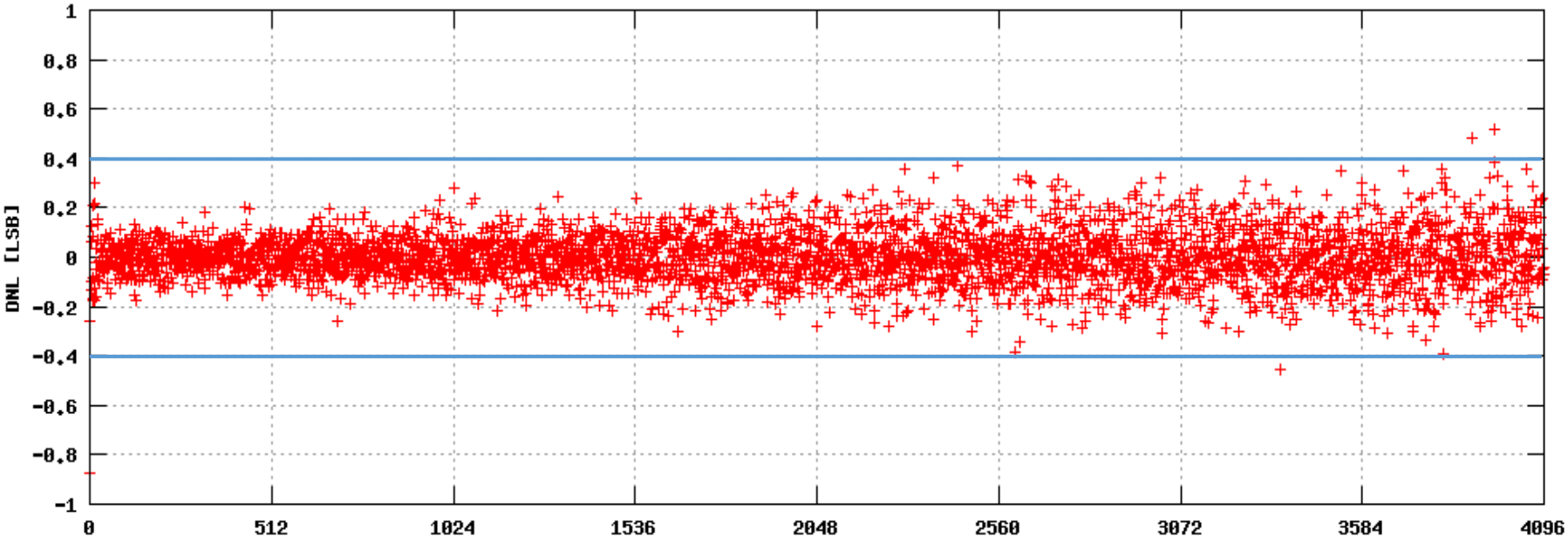

Figure 3: ADC DNL extrapolated with Instagram method with linear ramp in input, 1600 average samples per bin, source voltage from 16 bit DAC.

ADC Integral Nonlinearity

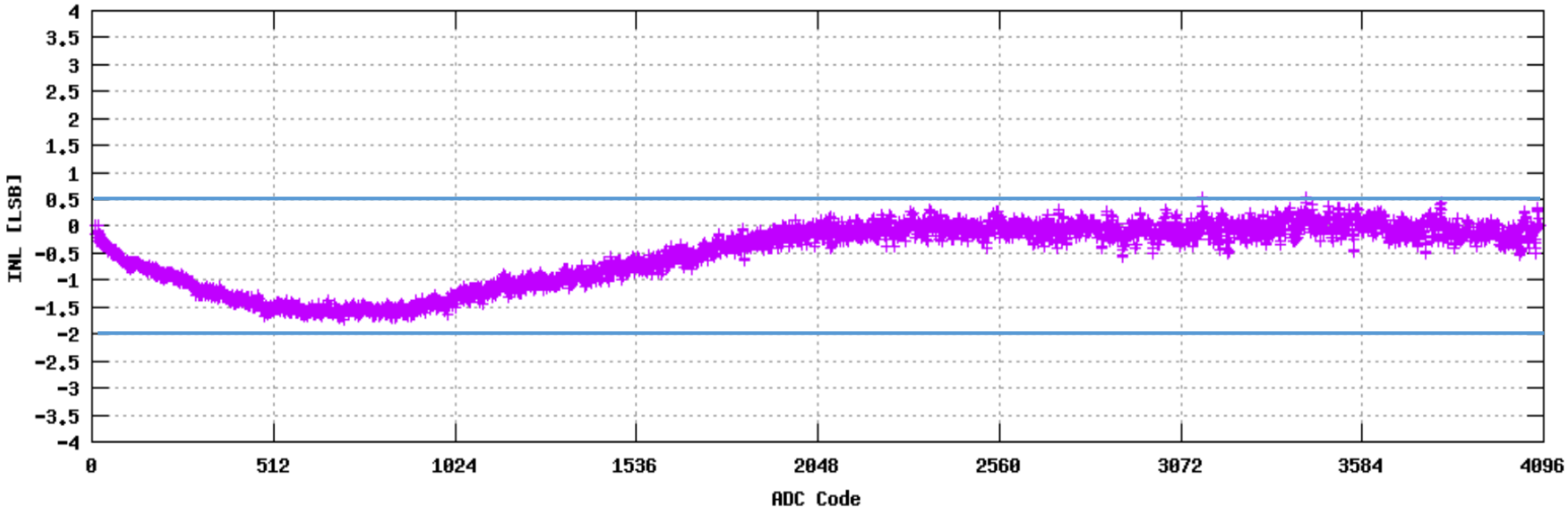

Figure 4: ADC INL extrapolated with Instagram method with linear ramp in input, 1600 average samples per bin, source voltage from 16 bit DAC.

ADC noise performances

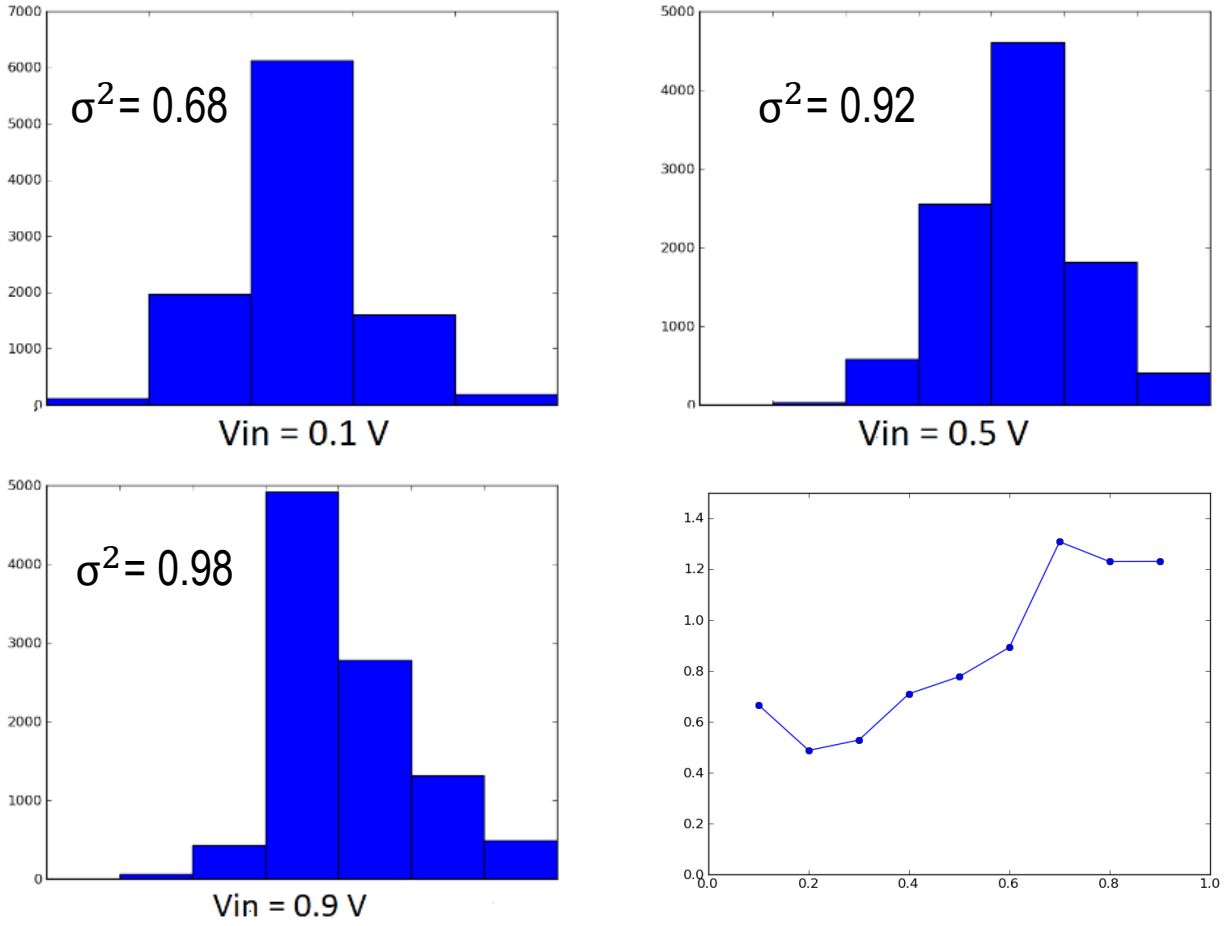

Figure 5: Conversion result distribution with fixed input voltage at 0.1V, 0.5V and 0.9V. One been represents 1 count of the ADC

ADC Offset

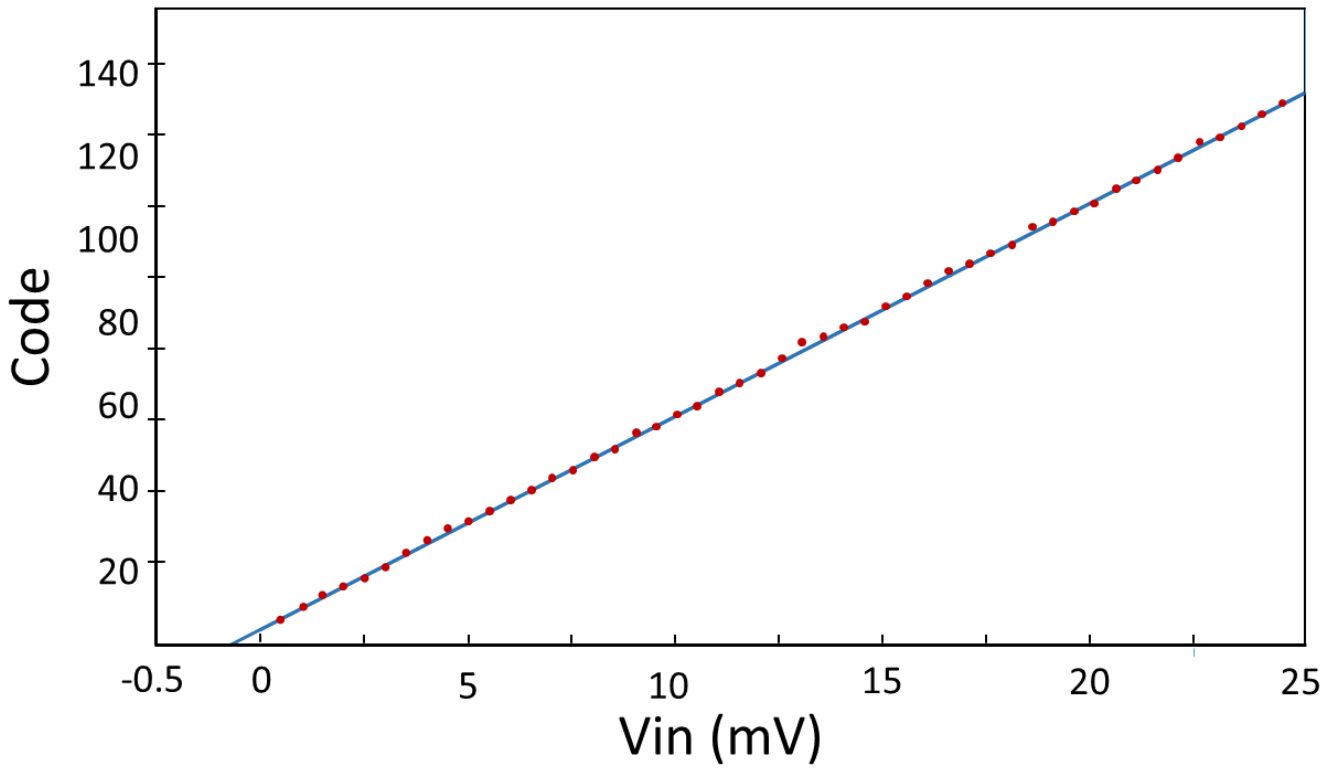

Figure 6: ADC Samples close to 0.0 V. From the fitting of the samples (uncalibrated data without offset and gain correction) it is possible to extrapolate the offset due to the comparator. This offset is correctly evaluated and subtracted by the ADC internal state machine, giving the expected correct result.

ADC TID tests 1/2

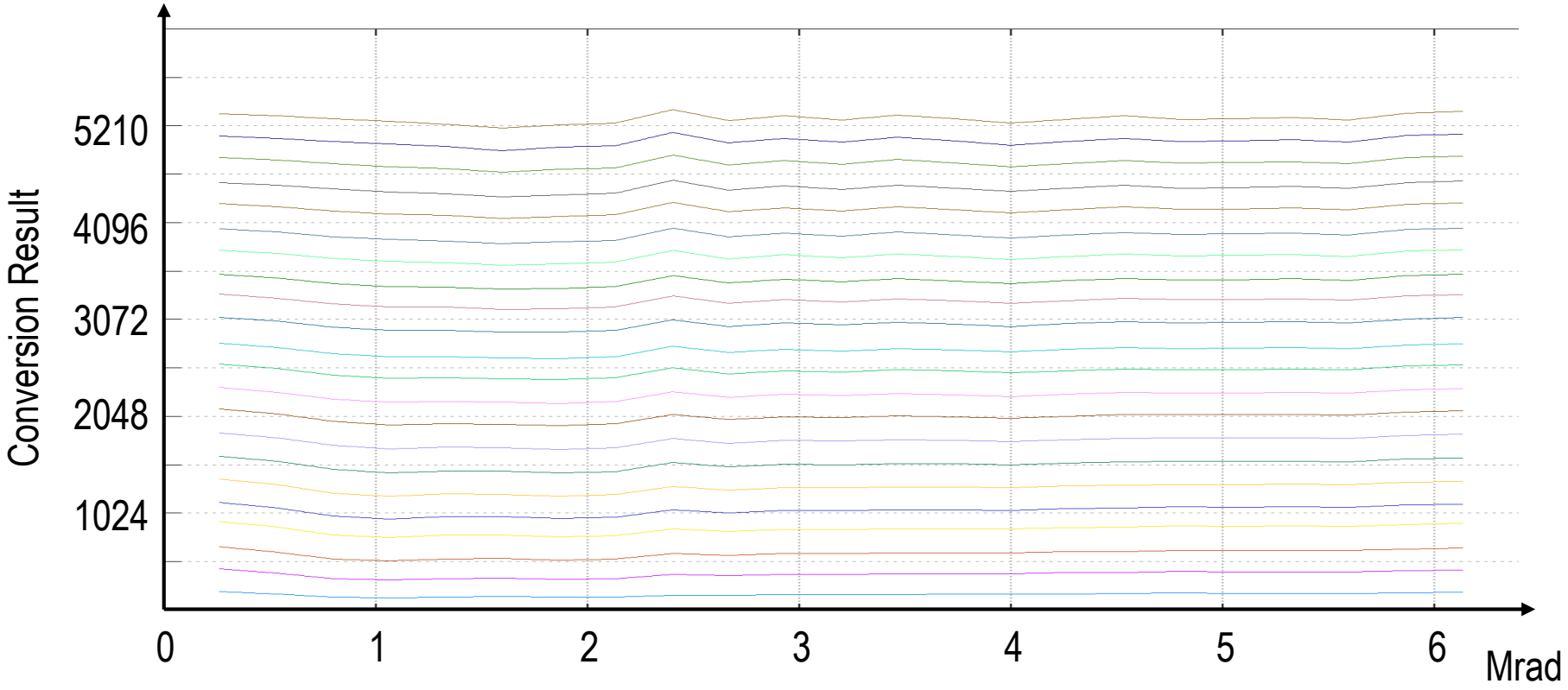

Figure 7: ADC conversion result with input voltage from 0.0V to 1.0V with steps of 0.1V. A set of measurements is taken every 200 Krad. Dose rate of 800 Krad/h.

ADC TID tests 2/2

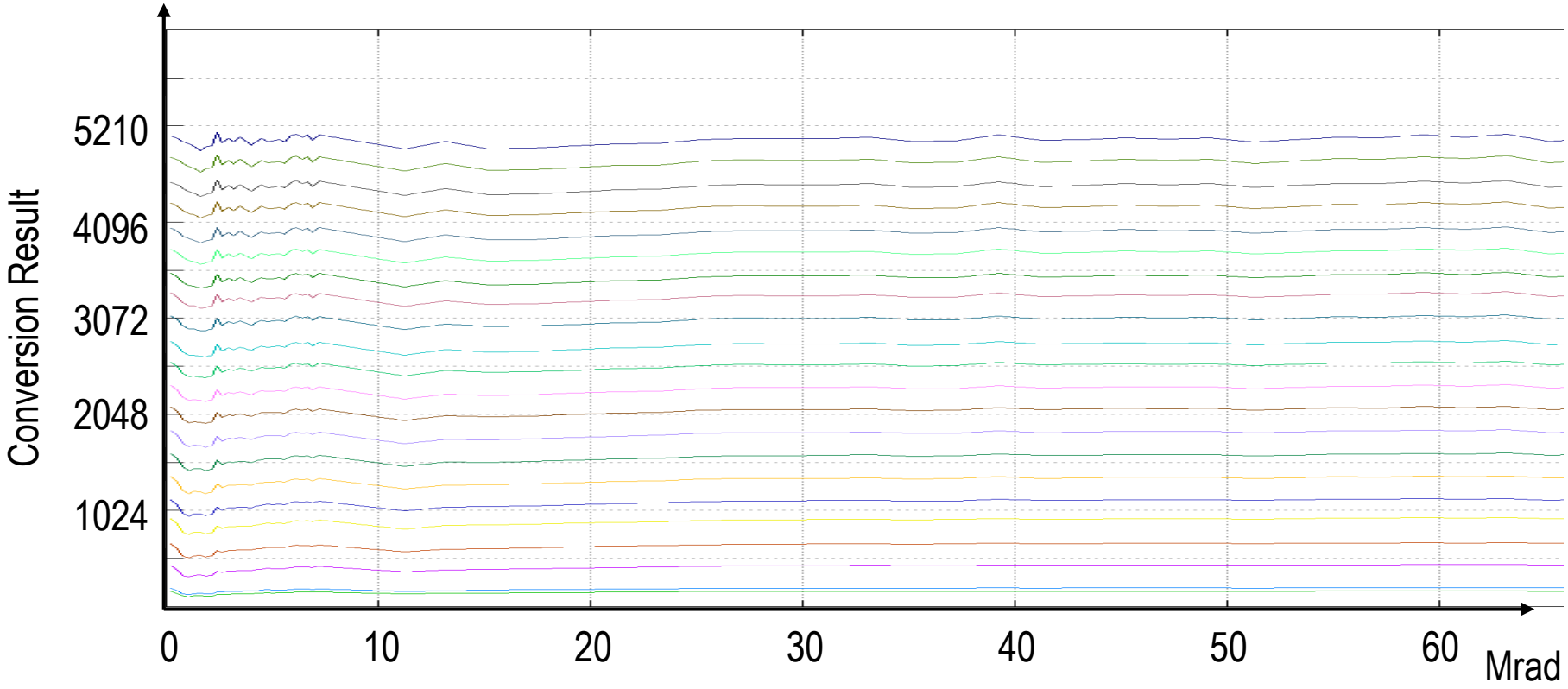

Figure 7: ADC conversion result with input voltage from 0.0V to 1.0V with steps of 0.1V. Dose rate of 800 Krad/h up to 6 Mrad and 8 Mrad/h up to 70 Mrad

ADC Calibration Procedure

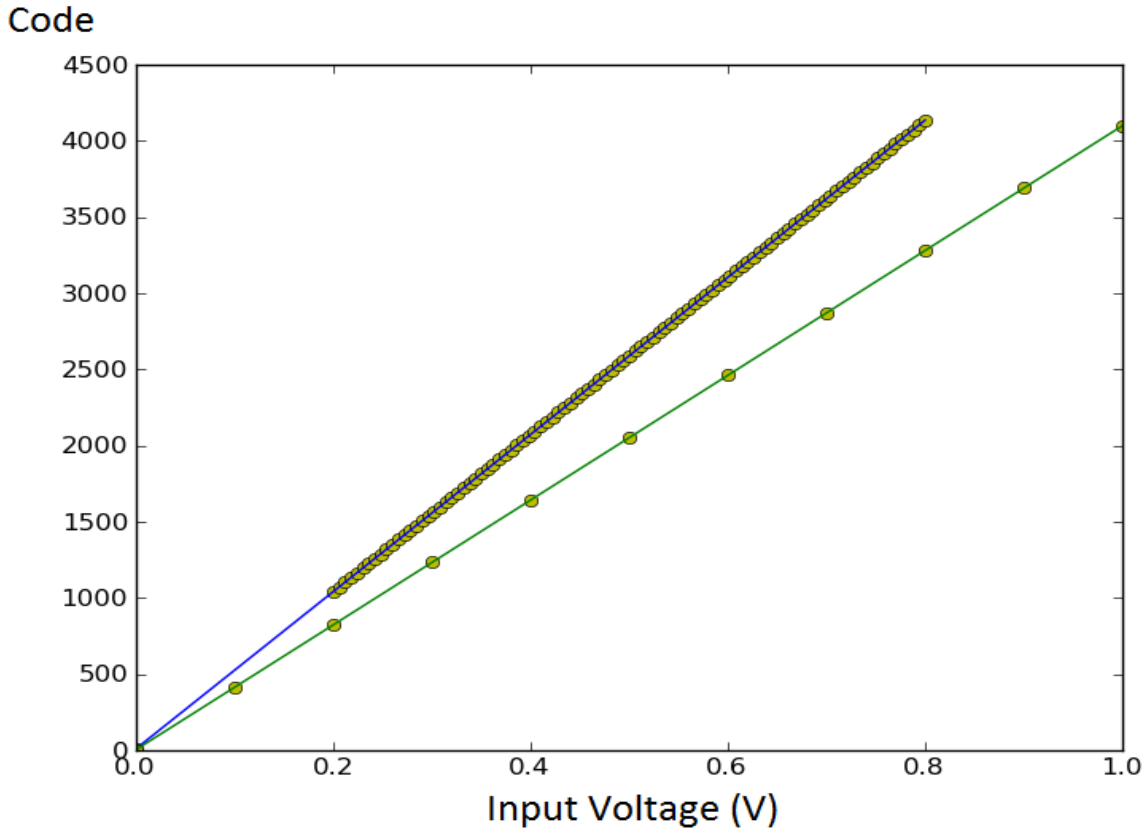

Figure 9: calibration procedure implemented on the chip. The blue line represents the linear interpolation of several samples on the ADC before to apply the calibration procedure, while the green line represent the slope after calibration.

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Production plans

- Engineering run Scheduled for the 1st July 2016
- Volume of 20 000 samples
- Unpackaged cheeps will come back in October 2016
- Packaged chips will be ready for early 2017

Thanks!