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FCC Task 11: activities progress reports

Total dose sensitivity of deep submicron CMOS technology

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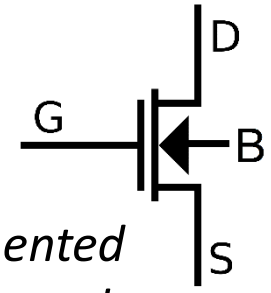
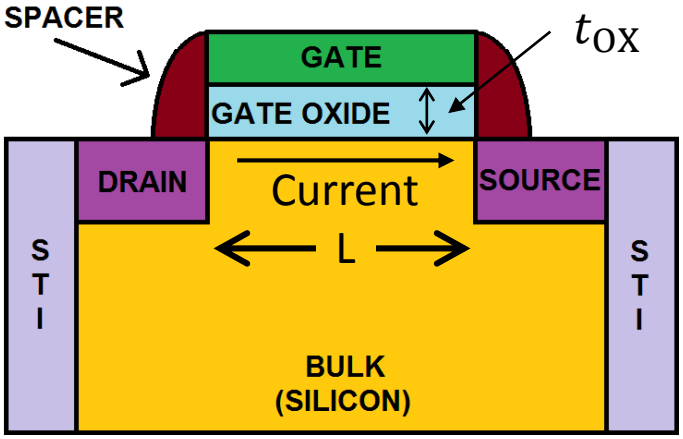
- MOS transistor is the most important device in digital electronic.

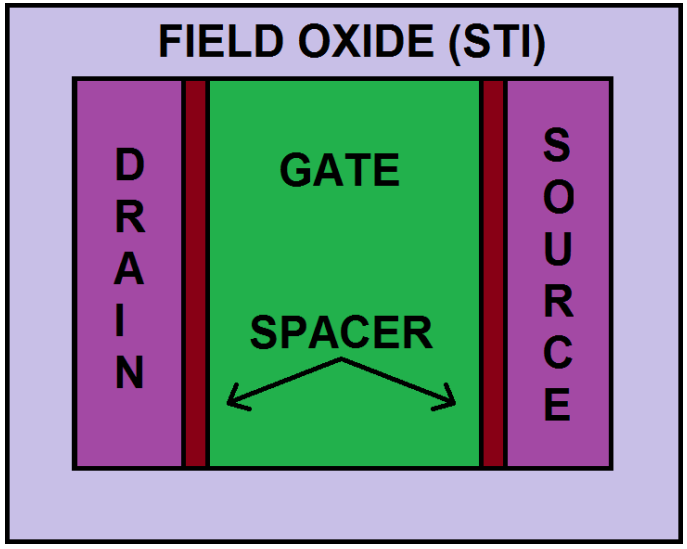




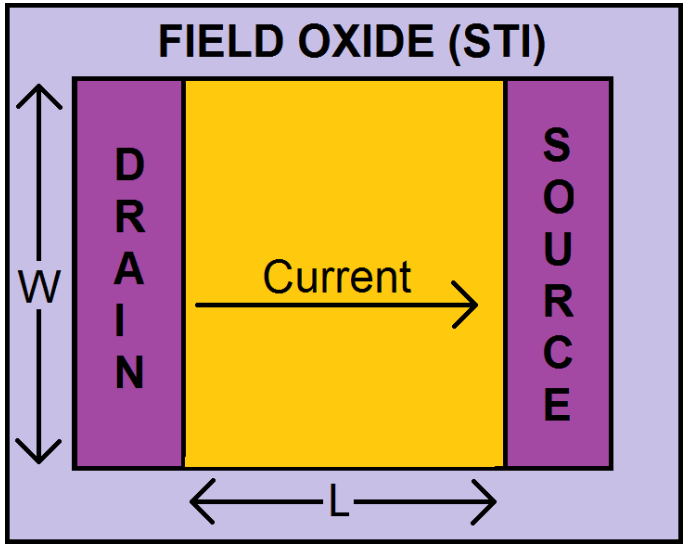
MOS Cross Section

- *"The total number of instrumented channels is about 80 million, each containing approximately 1,000 transistors"* [1].

[1] AAD, G., et al. ATLAS pixel detector electronics and sensors. *Journal of Instrumentation*, 2008

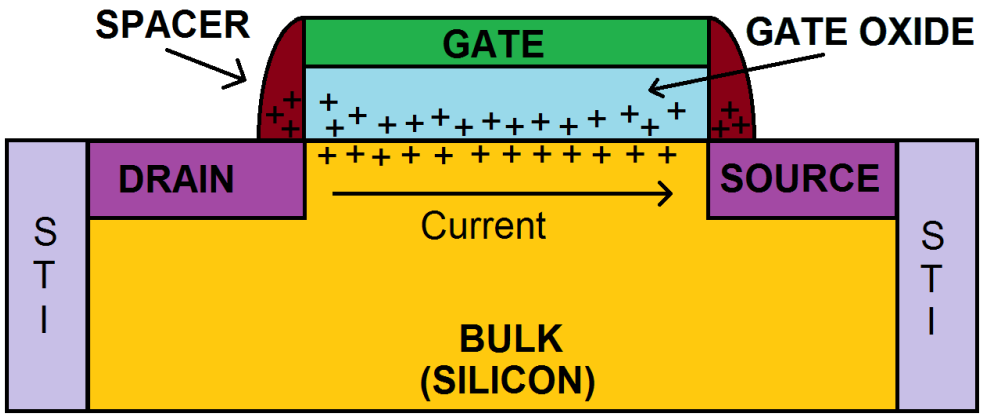


MOS Top View

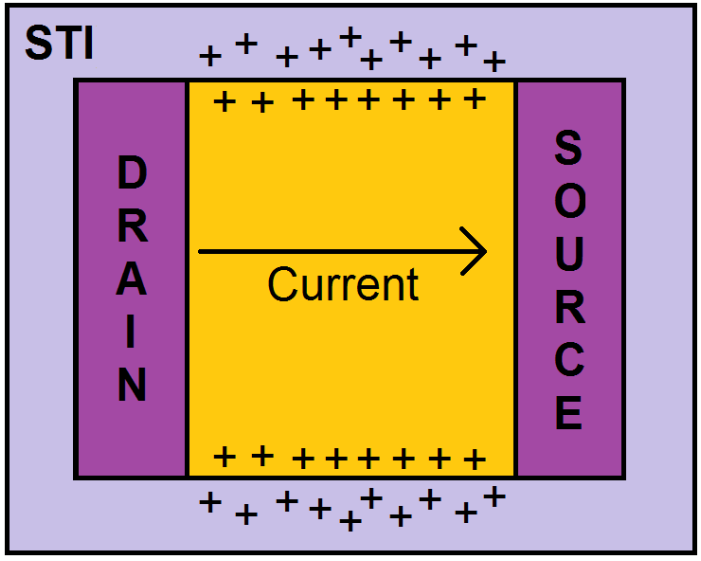


MOS Top View
(Below gate oxide)

❑ The most rad-sensitive part of the CMOS technology are the oxides.

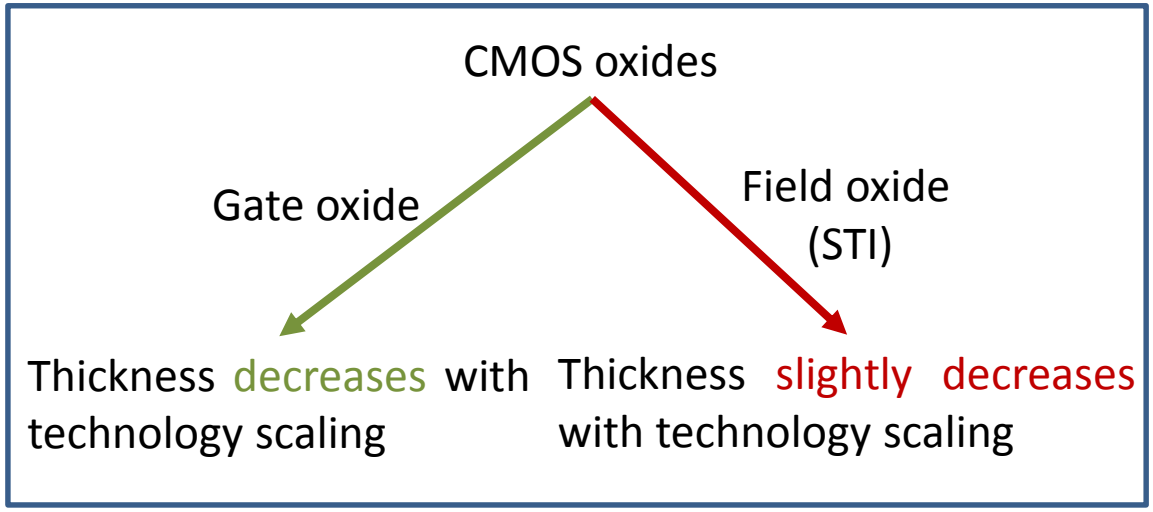


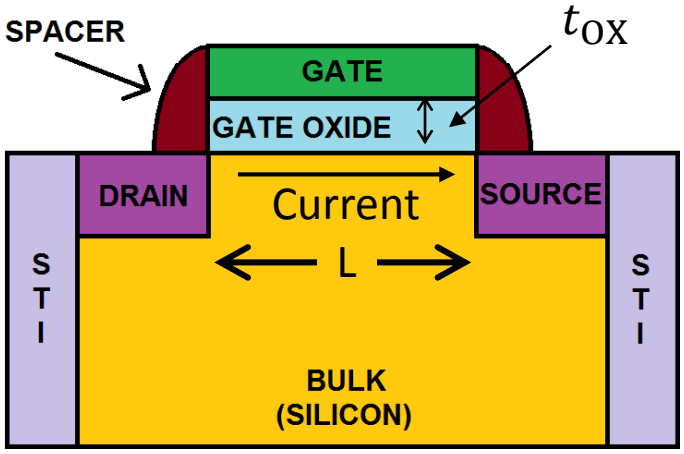
MOS Cross Section



MOS Top View

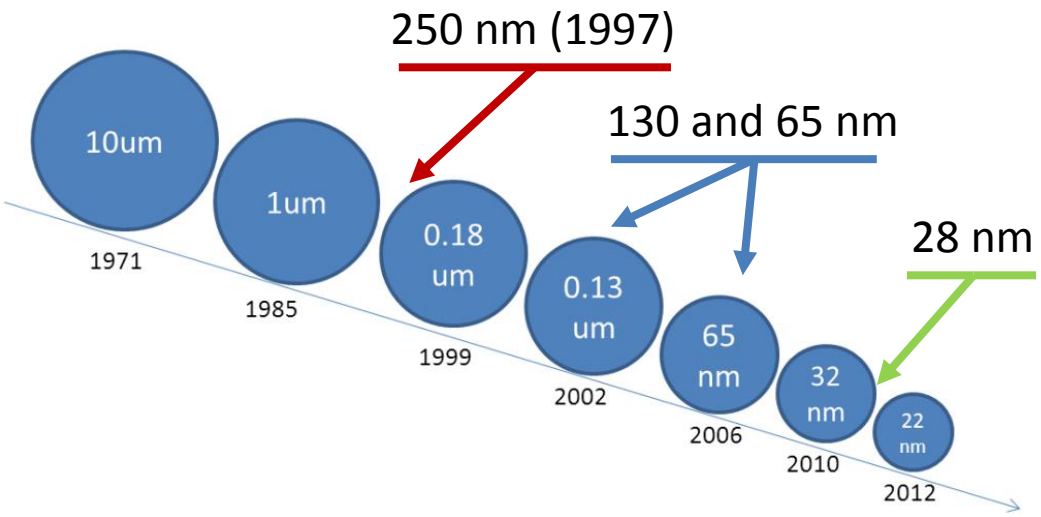
- Radiation hardness improves when thickness of oxides decreases.





MOS Cross Section

- In modern technology the thickness of gate oxide (t_{ox}) is less than 2nm -> gate oxide can be extremely radiation hard.

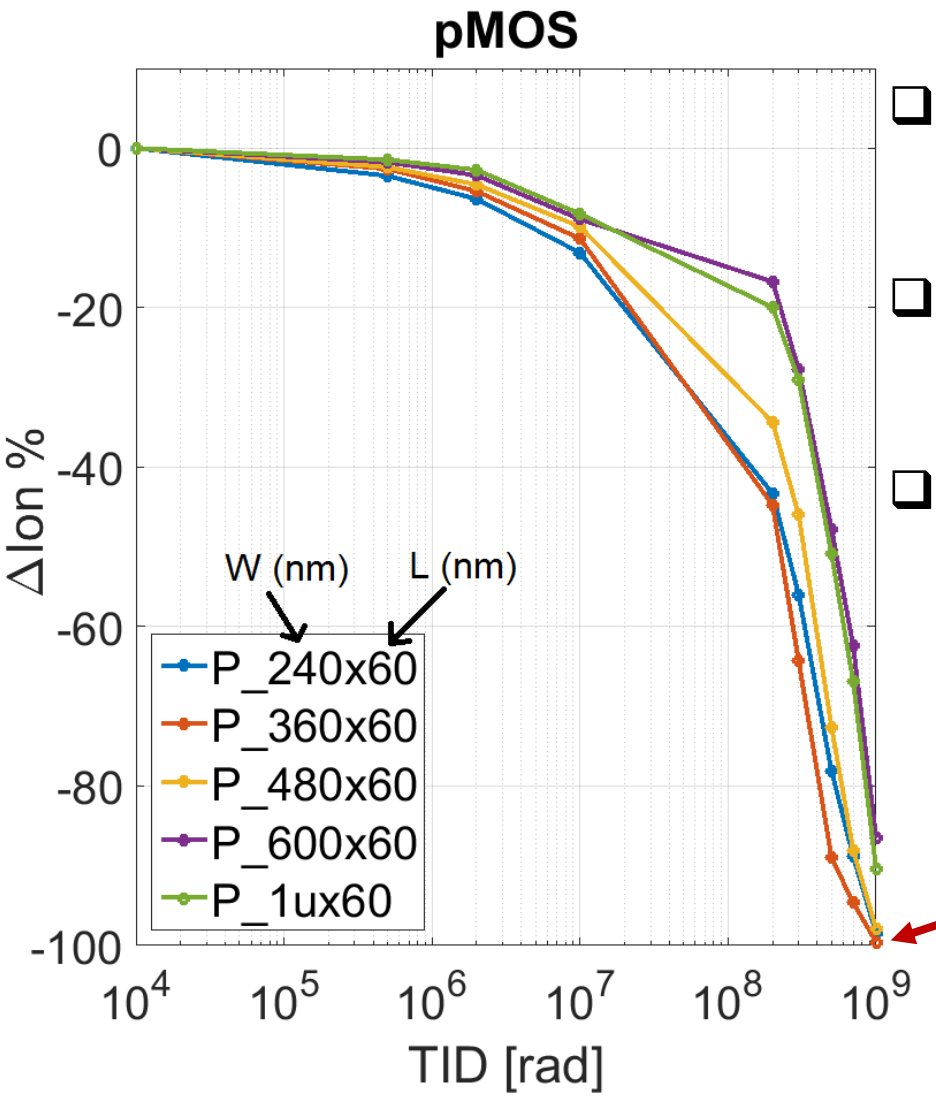


- The technology node is defined by the minimum channel length (L).

- The technology currently used in the LHC experiments is the 250nm.

- LHC upgrades will increase the Total Radiation Dose that detectors and devices have to withstand.

- We are mainly studying the 65nm technology, that has been proposed for the new pixel detectors used in the HL-HLC and we started to investigate the radiation response of 28nm MOS technology.



- Irradiation strongly affect CMOS 65nm performances (Ion).
- In HL-LHC pixels of inner layer will be exposed at $\mathrm{TID} = 1\mathrm{Grad}$ in ten years.
- The smaller transistors have a very large Ion degradation.

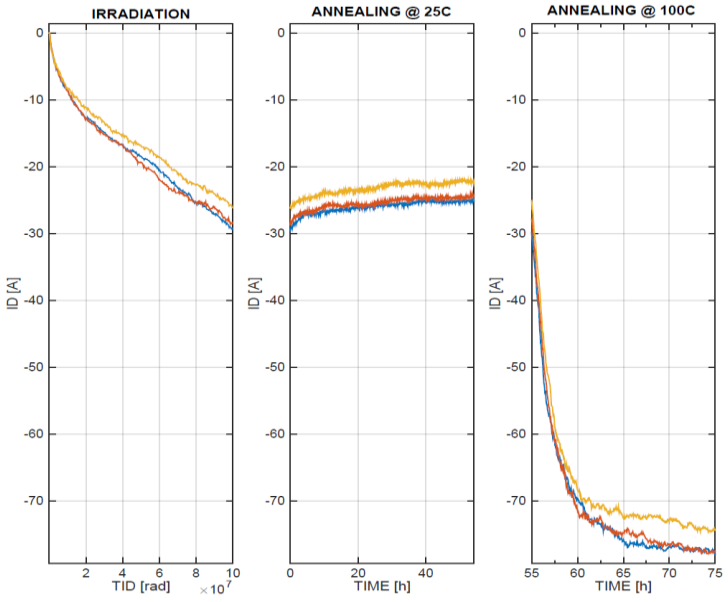
65nm pMOS
$\Delta I_{ON} \cong 100\%$

TID = Total Ionizing Dose

I_{ON} = Drain current at $\mathrm{V_{gs}} = \mathrm{V_{ds}} = \mathrm{V_{dd}} = \pm 1.2\mathrm{V}$

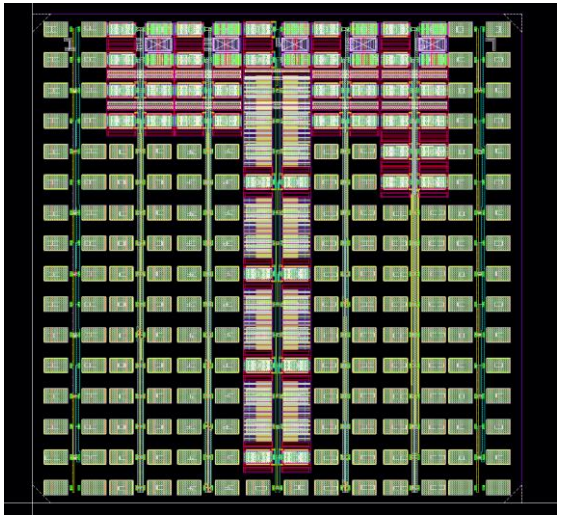
- Evolution during irradiation is strongly depended on many parameters:
  - Transistor size (W and L)
  - Temperature
  - Bias
  - Dose Rate

- Unexpected evolution after irradiation (depended on size, temperature and bias) and a further degradation of I_{ON}.



- At very high TID the devices have a complex radiation response
  - More experiment are needed to understand what will be the evolution in the real environment.

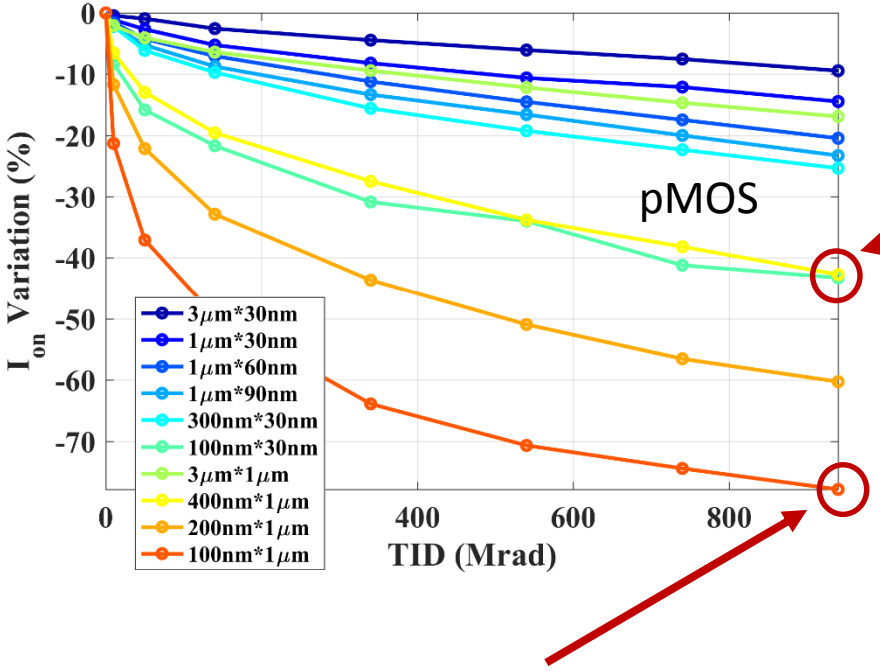
- New test chip with new test structures will be available soon. This will hopefully allow a deeper understanding of radiation effects.



- New kind of measurements in collaboration with University of Padova (Italy) and Vanderbilt University (USA).

- We are also measuring the radiation response of 65nm technology produced by different suppliers.

- We started to study the 28nm technology, in collaboration with EPFL (ICLAB) and INFN.



pMOS 65nm	$\Delta I_{ON} \cong 100\%$ (1Grad)
pMOS 28nm	$\Delta I_{ON} \cong 75\%$ (1Grad) *

* In 28nm technology the worst case is not the minimum size transistor, but the one with smaller W (100nm) and larger L (1μm)

- We just begin to understand the causes of high degradation of the CMOS technology's performances after irradiation.
  - At very high TID the 65nm MOS transistors have a large performance degradation.
  - Current degradation is due to isolation oxides, not to gate oxide.
  - We began to study more advanced technologies than 65nm but more experiment are needed.
- New test chip with new test structures will be available soon and new kind of measurements are scheduled.