Status of SS QD/QPS

- Commissioning took place between May 25th and May 30th.
- QD/QPS has been upgraded
  - Modified logic
  - Modified diode dump trays (Energy absorbers)
  - New contactors
  - New external dump resistor modules
  - New DCCT system
  - dI/dt signals for all coils
  - Improved noise performance
- Now all energy is extracted from the magnets under most “fault-detection” scenarios.

Status of SS QD/QPS II

- SSU:
  - All the interlocks for SSU and SSD have been commissioned
  - SSU cold checkout has been successfully completed.
  - SSU QD balancing have been successfully completed and the threshold values have been set.
  - For SSU successful discharge event was triggered at 50 A.
  - SSU was ramped up to 120 A
    - Stopped when wire gauge readings for end walls indicated potential issue

Status of SS QD/QPS III

- SSD:
  - SSD cold checkout has been successfully completed.
    - During the checkout we have found out that on the instrumentation tree connector side the associated V-taps for the C and J pins were swapped. This was the reason why the E1-C-E2 circuit Center tap (VTM09) and the M2 VTM03 V-taps were considered to be broken. We reconfigured the CVT Box and we were able to revive the functionality of these V-taps; to be connected to the right FPGA and QC channels.
    - With regard to QD/QPS, SSD now has same functionality of SSU
  - SSD QD balancing have been successfully completed and the threshold values have been set.

Work Remaining

- For both SSU and SSD the current readout for the E1-C-E2 circuits (SSD and SSU) needs to be adjusted to ensure that the current reading is consistent with the current flowing in the magnets. The difference should not be larger than few mAs. This requires to:
  - Modify the dump resistor diodes. Most likely needs to be increased the number of diodes that are the placed in series with the dump resistors. The diode opening voltage for each leg should be at least 2V or larger.
  - And maybe to re-locate all three DCCTs to be in the current loop the magnet sees.
- SSD QD Coils GUI needs to be re-labeled to be consistent with the input signals.
- SSU ISOAMP offsets for the LTS and HTS channels needs to be introduced.
- QD Lead thresholds need to be set to allowable minimums
- Filter boxes (for SSU and SSD) need to be reconfigured:
  - For all magnet voltage segments the time constant needs to be changed to 1 sec. (Better noise performance)
- Re-do balancing for the QD coils.
- Ramp the current to nominal values for SSU and SSD individually and then simultaneously.