Exceptional conditions during powering tests-the rules

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My understanding of the issue after discussions with:

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Contents

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What are exceptional conditions?

- There is no! Except...:
  - Cryo conditions not met in the whole powering sub-sector for nominal operation, but OK in part of it and/or for a subset of tests
  - Based on MPP table, request to mask the cryo interlocks to go on the tests

State	Target K	Cryo_START K	Cryo_Maintain K	Circuit	what steps can be executed	Notes
CRYO_OK_2.1K	2,1	2,15	2,35	All	All up to PNO	Liquid everywhere
CRYO_OK_2.5K	2,5	2,6	2,8	RB, IPQ (not the Q6 with MQTL)	PCC, PIC2, PLI1	Liquid everywhere,
				600A-N-line, 60 A, 120 A	PCC, PIC2, PCS, PLI, PNO	with possible exception of RQ busbars
				600A spool, RQ	PIC2	
CRYO_OK_3.5K	3,5	3,6	3,8	60 A, 120 A	PCC, PIC2, PNO	GHe in RQ busbars,
				600 A-N-Line	PCC, PIC2	Possible gas pockets in magnets
CRYO_OK_4.5K	4,5	4,6	4,8	600 A	PIC2	
				60 A, 120 A	PCC, PIC2	GHe everywhere

N.B. PIC2 is at 0 A for all 60 A, 120 A and 600A circuits

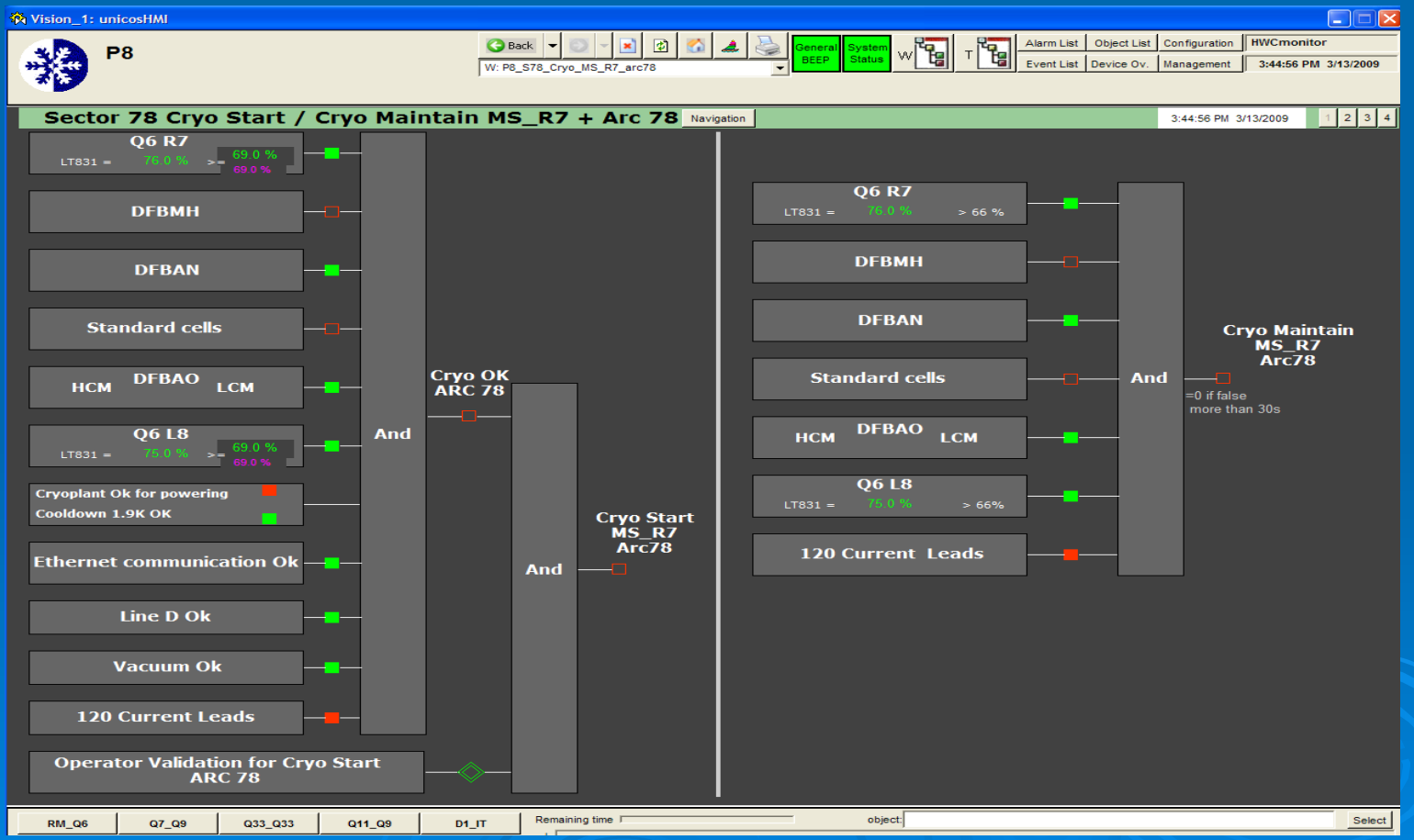
Other exceptional conditions?

- Problems in current leads, He level, transient after a quench,... : local problem for powering but preventing having the CryoMaintain/CryoStart for the rest of the sector
  - Force signal to set CryoMaintain/CryoStart OK to go on commissioning of other circuits
- Access in the tunnel during phase 2 (see Matteo's talk)
  - Software interlocks/procedure?

➔ Exceptional conditions means trying to gain flexibility to go on with commissioning by masking or forcing signals

CryoStart/CryoMaintain

- The cryo interlocks needed to start powering tests (both) and go on the tests (CryoMaintain)



CryoMaintain: from Cryo-side

- CryoMaintain signal cannot be forced if conditions not OK
- But it is possible to force signal read from hardware (temperature, level) to a fixed value to provide CRYO_START and CRYO_MAINTAIN = OK:
  - equivalent to deactivate the regulation
  - equivalent to manual control by the cryo operator, dedicated to this task
  - -> Only 1 simulated value per sector (= per operator)
- Cryo OP can do the forcing, but decision given to the expert level
- If value is forced, a little yellow F is displayed on the synoptic

CryoStart

- Mandatory manual validation by the operator to start a test
- Signal can be forced and/or blocked
- Was used during transient phase to restart test faster:
  - Example : after quench in Q5, to restart a test in Q4D2 (same sub-sector)
  - On demand of the HW coordinator or EiC
  - In parallel, locking of the concerned circuit at the PIC level (Q5 in previous example)

Forced signals in 2008

- Was used to allow commissioning of circuits in case of:
  - He level not within tolerance because of problem on gauge level or transient after a quench
  - Problem on current leads
- Forcing of temperature or level in a current lead is also possible during beam operation if not a main circuit (define on the case by case basis with ABP and EiC)

Procedure to set a signal to a fixed value in 2008

•Cryo expert together with Point Owner identify the leads whose values are going to be forced (the correspondence between current leads and electrical circuits is obtained from the layout DB).

2)Point Owner blocks the circuit at the PIC level, opens an incident in the Powering Pages and sends an email to the HW Coordinators asking for their OK to force the cryo signals.

3)The HW Coordinator gives his OK by email to the CRYO expert.

4)The Cryo expert forces the values which should give CRYO_START and CRYO_MAINTAIN.

- in this case PIC does not mask any interlock signal but just prevents us from powering the circuits

• Once the issue is solved, the real signal values are re-established by the CRYO expert, an email is send from the CRYO expert to the HW Coordinators who authorizes the Point Owner to unblock the circuit and to close the incident.

What are the risks?

- Consequence in case of powering of the wrong circuit:
  - Overheating (current leads),
  - Risk of quench (blocked gauge level)
- 2 layers of protection:
  - Cryo interlocks first to trigger at a reversible level
  - The QPS triggered by the developing voltage
- Forcing signal = loss of first level of protection, the reversible one
  - We still have the second level (QPS)
  - Increased damage risk
- In the future, thermo switches on top of current lead will help (part of LHC in 2009/2010)

Procedure to mask CryoStart/CryoMaintain (2008)

- If really needed (for instance to carry out tests without current in the magnets) with the following steps:

  1)The EIC asks the PIC expert to mask the signal/s.

  –The PIC expert sends an e-mail to the HW Coordinator asking OK to mask the signal.

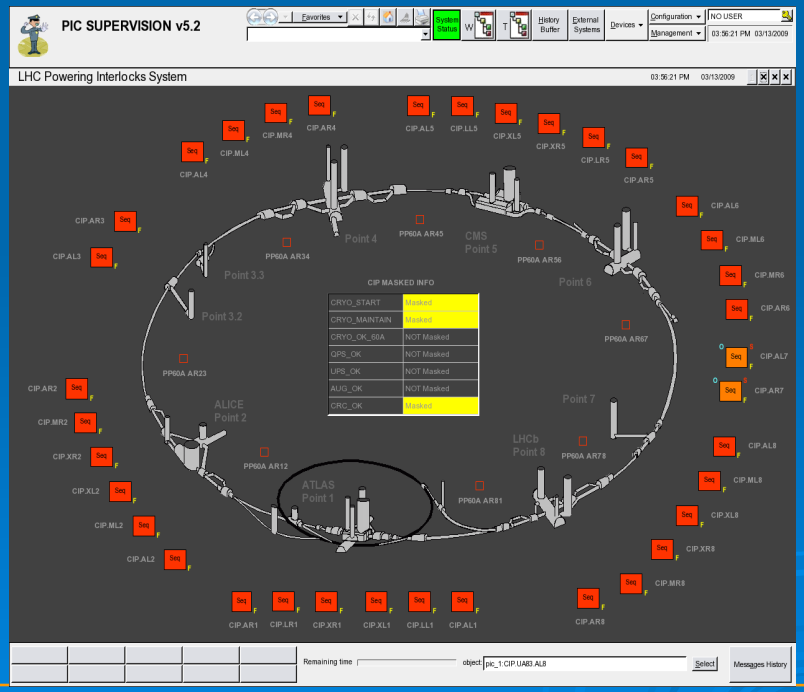
  –The HW Coordinator gives his OK by email to the PIC expert.

  –The PIC expert masks the signal and unmask it once the masking is not needed anymore sending an email to the HW Coordinator informing that the interlock signals have been unmasked.

- Only the software CRYO_START and/or CRYO_MAINTAIN can be masked at the PIC level

PIC: Masked settings

- A summary view which show that at least 1 signal is masked in the whole machine
- A detailed view (CRYO_START, CRYO_MAINTAIN, CRYO_START_PP60A, QPS_OK, UPS_OK, AUG_OK, CRC_OK) for all the PICs
- Only PIC expert can mask



CIPC	CRYO_START	CRYO_MAINTAIN	CRYO_START_PP60A	QPS_OK	UPS_OK	AUG_OK	CRC_OK	LASER MODE
CIP.UJ16.XR1							Masked	0
CIP.UJ16.LR1							Masked	0
CIP.UJ16.AR1							Masked	0
CIP.UA23.AL2							Masked	0
CIP.UA23.ML2							Masked	0
CIP.UA23.XL2							Masked	0
CIP.UA27.XR2							Masked	0
CIP.UA27.MR2							Masked	0
CIP.UA27.AR2							Masked	0
CIP.UJ33.AL3							Masked	0
CIP.UJ33.AR3							Masked	0
CIP.UA43.AL4							Masked	0
CIP.UA43.ML4							Masked	0
CIP.UA47.MR4							Masked	0
CIP.UA47.AR4							Masked	0
CIP.USC55.AL5							Masked	0
CIP.USC55.LL5							Masked	0
CIP.USC55.XL5							Masked	0
CIP.UJ56.XR5							Masked	0
CIP.UJ56.LR5							Masked	0
CIP.UJ56.AR5							Masked	0
CIP.UA63.AL6							Masked	0
CIP.UA63.ML6							Masked	0
CIP.UA67.MR6							Masked	0
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CIP.TZ76.AL7							Masked	0
CIP.TZ76.AR7							Masked	0
CIP.UA83.AL8	Masked	Masked					Masked	0
CIP.UA83.ML8							Masked	0
CIP.UA83.XL8							Masked	0
CIP.UA87.XR8							Masked	0
CIP.UA87.MR8							Masked	0
CIP.UA87.AR8							Masked	0
CIP.UJ14.AL1							Masked	0
CIP.UJ14.LL1							Masked	0
CIP.UJ14.XL1							Masked	0

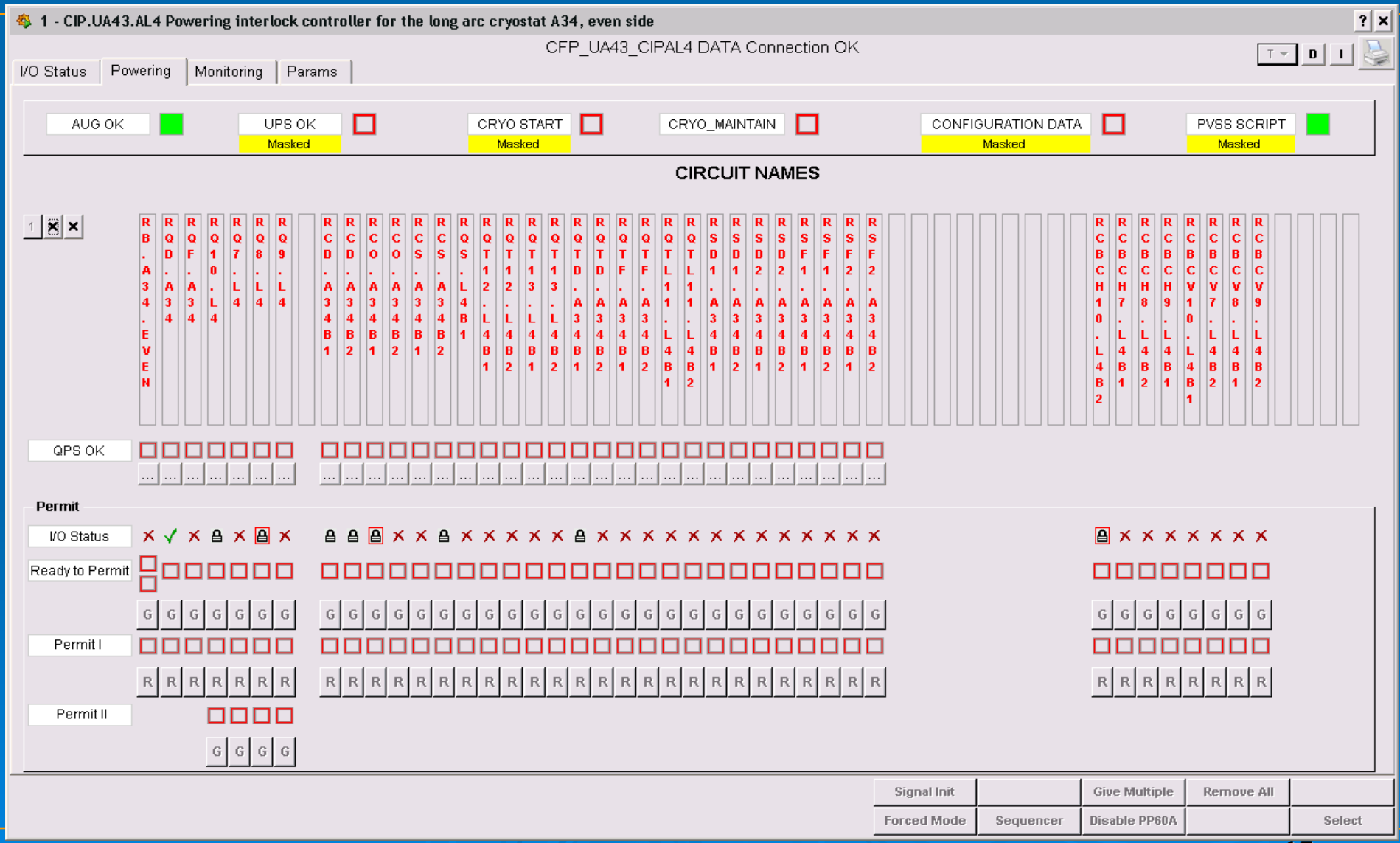
Feedback on the procedure

- Procedure based on e-mail exchange
- Procedure worked fine to set-up the exceptional conditions
- But treatment of the problem could be improved:
  - 2 or 3 near misses because procedure to come back to normal situation was not properly followed
- Problem of traceability of the block circuits in the long term (and with several sectors), because of 3 inputs to synchronize:
  - Report from equipment experts that problem is solved
  - Unblock at the PIC level
  - Update the web page

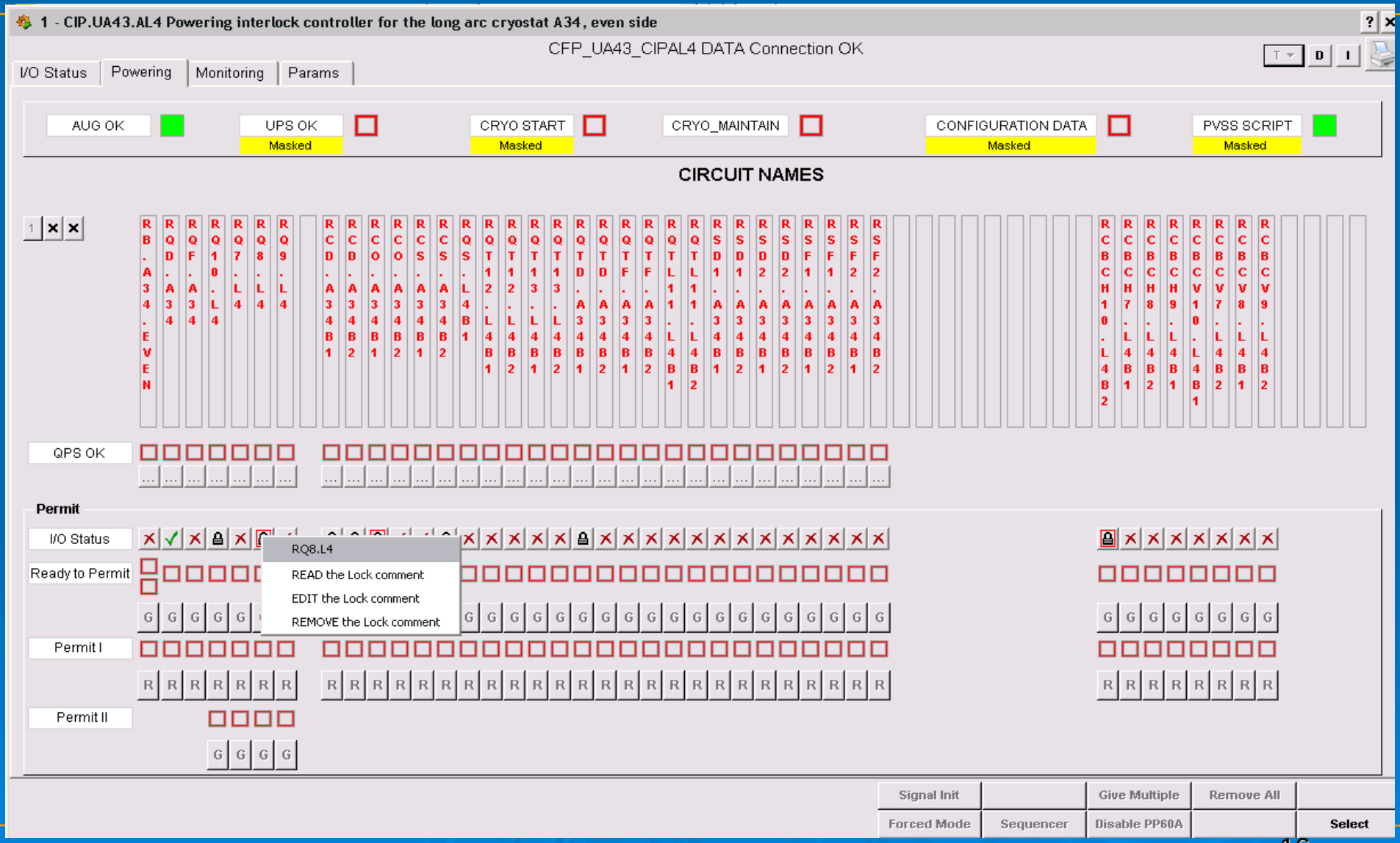
Improvements for 2009

- 2 layers of lock/unlock at the PIC level
- The standard block : individual lock of each circuit, by EiC/expert (the one used last year)
- Introduction of the superlock at PIC to allow traceability
  - All info inside the same tool
  - Possibility to distinguish between operational block and the real Hardware problems block
  - Possible to enter comments that are visible to every users, to replace the powering pages ?
- Superlock used only by point owners?
-

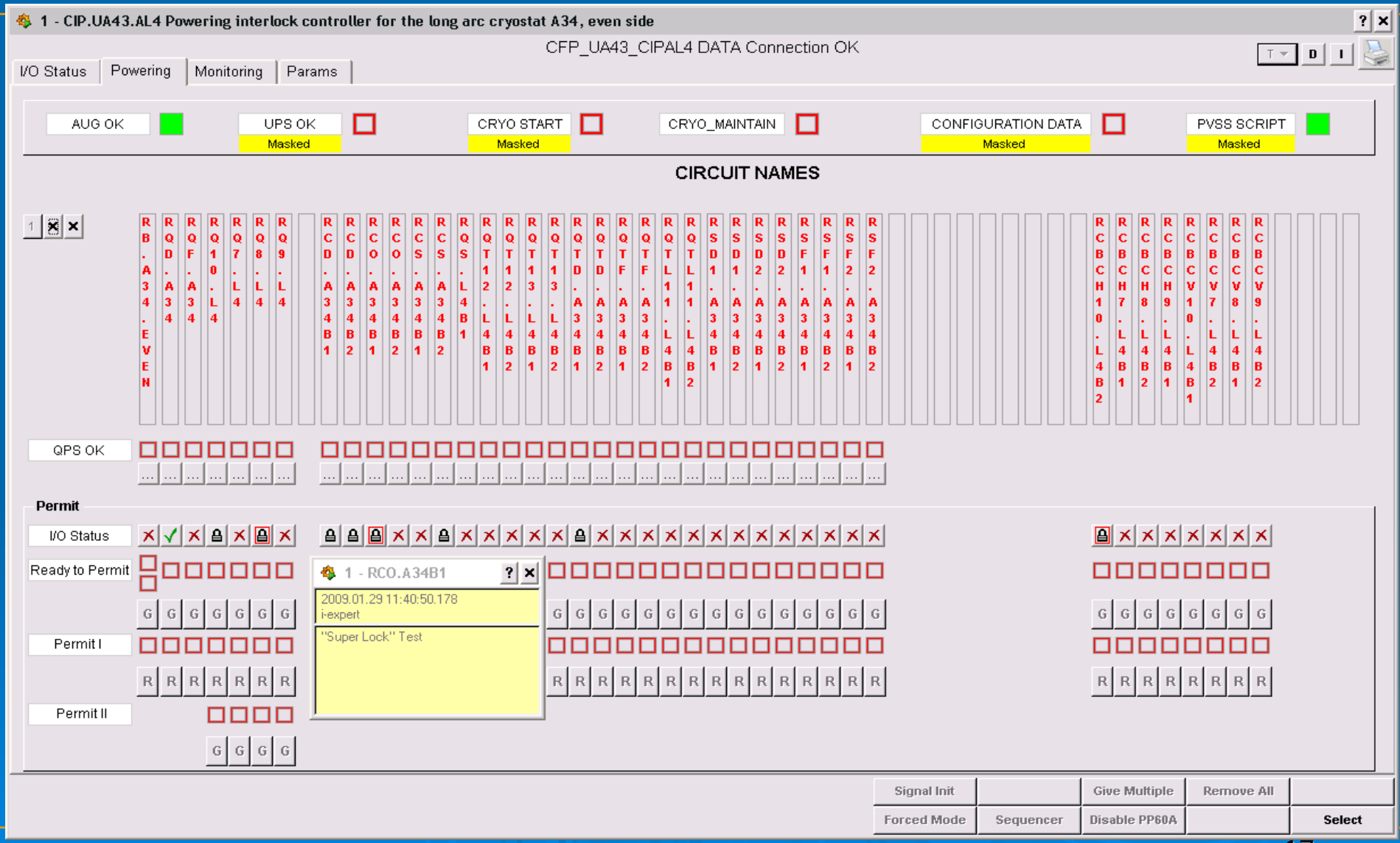
PIC: Superlock



PIC: Superlock



PIC: Superlock



PIC: The global lock

- The “Lock all / Unlock all” buttons:
  - To ease locking a full sector for giving access or for lock all but one for PC specialists tests
  - The “Unlock all“ will act only on the normal lock, the previously set superlocks will remain
  - EiC role
- On the TO DO list, but no principle issue

Improvements of procedures for 2009

- Circuits names added to the Cryo synoptic for common language:
  - Not needed anymore to go to layout database for correspondence between current leads and associated circuits, once validated
- Add EiCs in copy of the e-mail exchange :
  - Could use a kind of JIRA follow-up (as CO issues or MPP issues)?
- Systematically remove all mask and force signals at the end of the test day?

Conclusion

- Exceptional conditions = replacing interlocks by procedure to gain flexibility in the tests
  - expect fewer exceptional conditions than last year ...
- procedures used several times last year and will be improved following the feedback:
  - Improved PIC interface should allow a better follow-up of the problems
  - Minimized number of manual action
  - procedures in place but boundary conditions should be advertised enough for guidelines.
- Still only procedures to replace interlocks... shall we need other level/re-definitions of software interlocks as “garde-fou”?