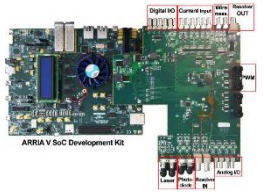
BI-BWS LINK



Beam Wire Scanner (BWS) serial link requirements and architecture

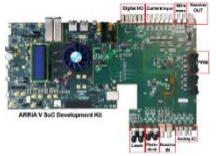
J. Emery for the BWS electronics team

Ad-hoc BI-TB meeting for inter-FPGA communication

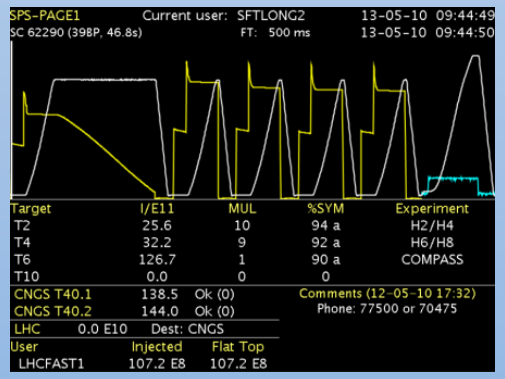
29.06.2016

BWS system connections

BI-BWS LINK



General Machine Timing (GMT)
Low jitter < 1ns, Granularity: 1ms



Beam Synchronous timing (BST)
Bunch synchronisation
(25 ns accurate clock)

Revolution frequency synchro
Triggers: scan start, post-mortem
Granularity: 89us (LHC), low jitter < 1ns

Beam Energy and Intensity

CISV or BCT ?

Expert monitoring

FESA class

Settings

Control room (CCC)

Logging storage
Long term storage for offline analysis

C P U

T I M I N G

BST receiver

CISV receiver ?

Serial link

Trigger input

ACQUISITION AND SUPERVISION

Ethernet TCP/IP – RJ45/SFP+

Serial link

BWS Drive code

INTELLIGENT DRIVE

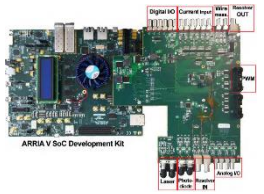
PHASE 1

PHASE 2

Beams Department

BWS link services requirement list

BI-BWS LINK



1) Data integrity
   Error detection, correction and/or retransmission.
   Notification and statistics.

2) Event transport
   Trigger and IO port replication between the 2 ends
   Link latency jitter < **0.1us**, (1km ~5us, Fused Silica 10°C up => +27ps)
   Automatic transmission time evaluation

3) Transparent interconnect SoC bus
   Interconnection of internal FPGA bus transparently (Memory Mapping),
   data blocks transfer between FPGA (2 directions), use of DMA mechanism, etc. PSB >= **118 Mbits/s**

4) Streaming links
   Interconnection of internal FPGA bus transparently (Stream interfaces: 1..N @ >= **1Mbit/s**)
   transparent connections for streaming mechanism

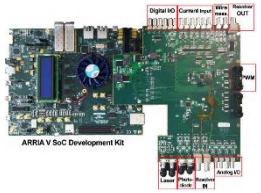
5) Virtual JTAG over the link (investigation)
   JTAG chain over the link: Use of vendor tool for logic analyser (SignalTap),
   memory/register content modification, probing by using Boundary Scan (tbc)

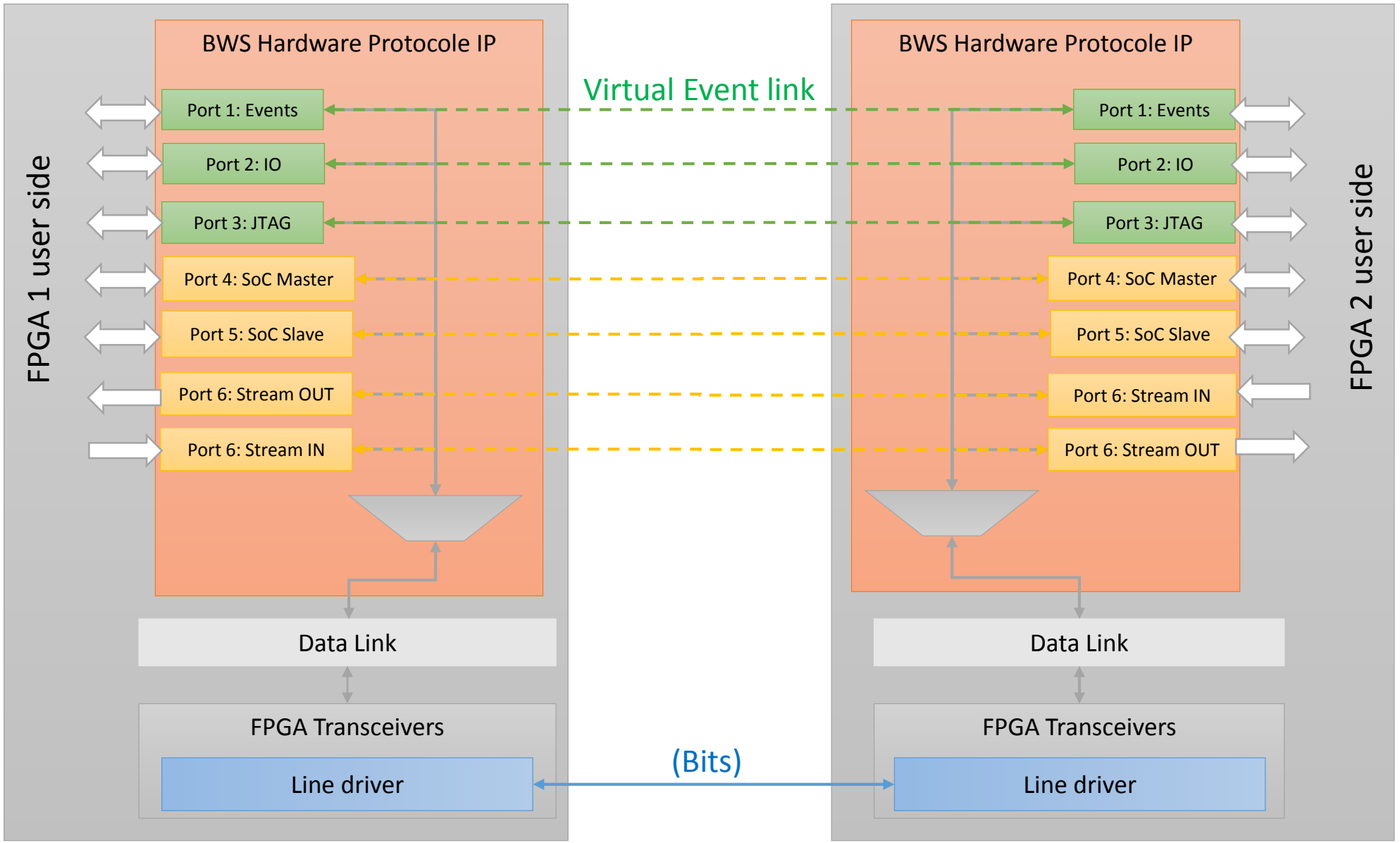
6) None-volatile memory management
   External flash management over the link.
   Read/write flash of program or settings.

Listed in the technical specification "**Beam wire scanner data and events digital link**" EDMS 1701798

IP core concept

BI-BWS LINK

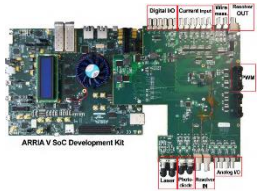




Development scheduled

Could probably be based on GBT layer (tbc)

Protocol layer architecture



Memory mapping between FPGAs
Access to any address transparently

single access and Large set of data

Bandwidth constrained

Timely constrained

SoC mapping master-slave

flash interface

external NVM interface

Point-to-point link

'Streaming link'

Virtual communication (Horizontal)

(Packets)

High Level BWS Protocole

Virtual JTAG debug tools & boundary scan?

JTAG chain

Triggers

Events/triggers

Digital IO

signals replication

(Frame)

Low level BWS Protocole

Data Link

Real communication (Vertical)

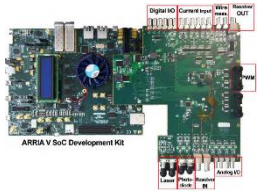
FPGA Transceivers

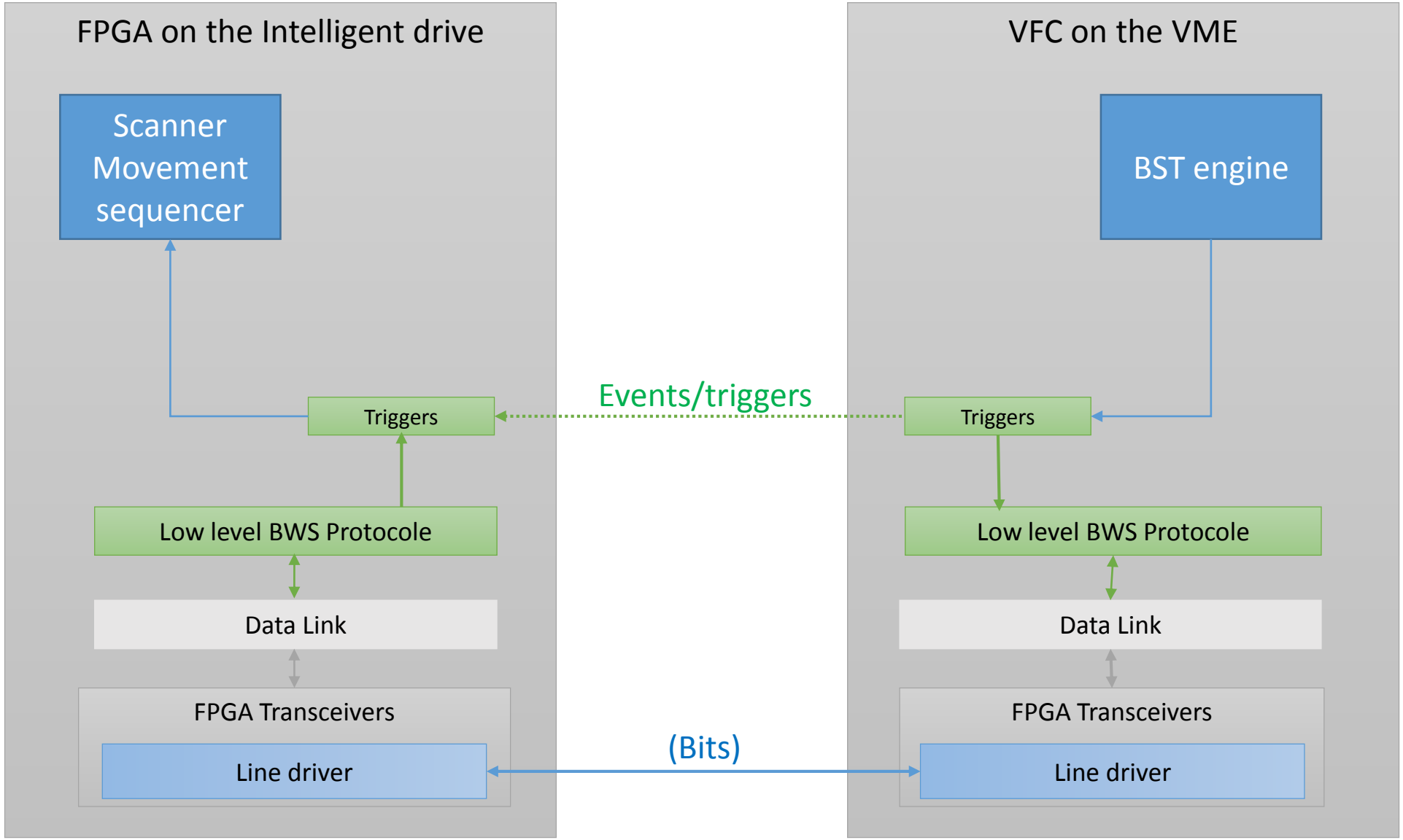
Line driver

(Bits)

Use case: Scanner movement start trigger

BI-BWS LINK





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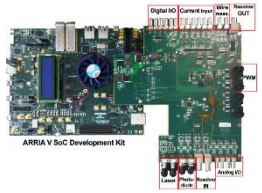
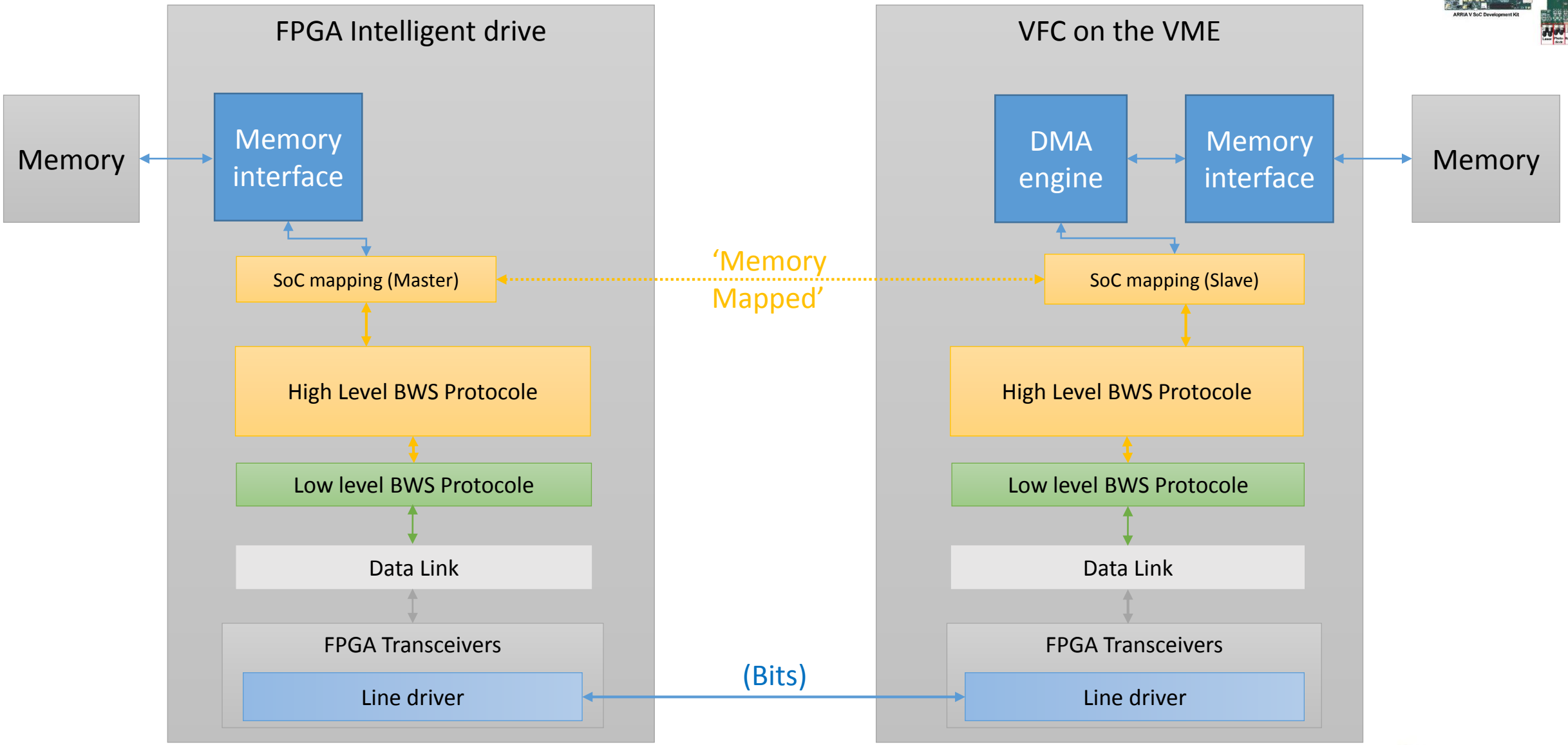
Use case: data collection after a measurement

BI-BWS LINK





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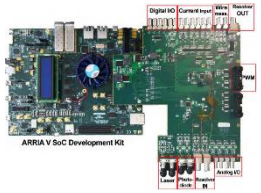
Use case: JTAG chain over serial link

BI-BWS LINK



FPGA Intelligent drive

Logic analyser

Memory - register read/write contents

Virtual JTAG (Altera)

JTAG interface

Low level BWS Protocole

Data Link

FPGA Transceivers

Line driver

Virtual JTAG chain

(Bits)

VFC on VME

JTAG

Virtual JTAG (Altera)

JTAG inteface

Low level BWS Protocole

Data Link

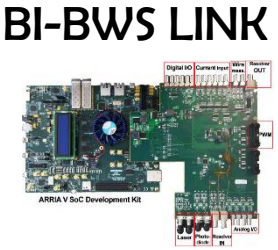
FPGA Transceivers

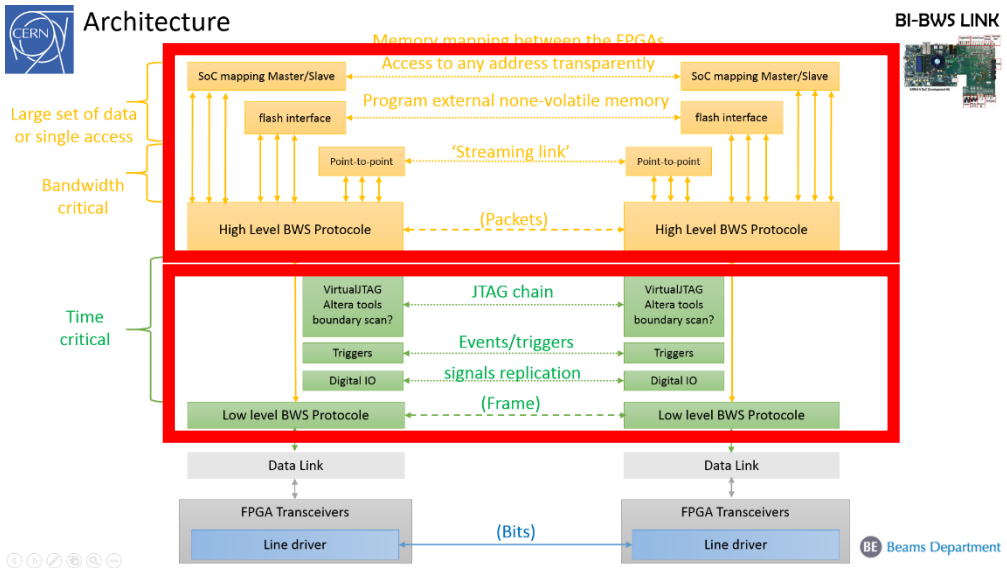
Line driver

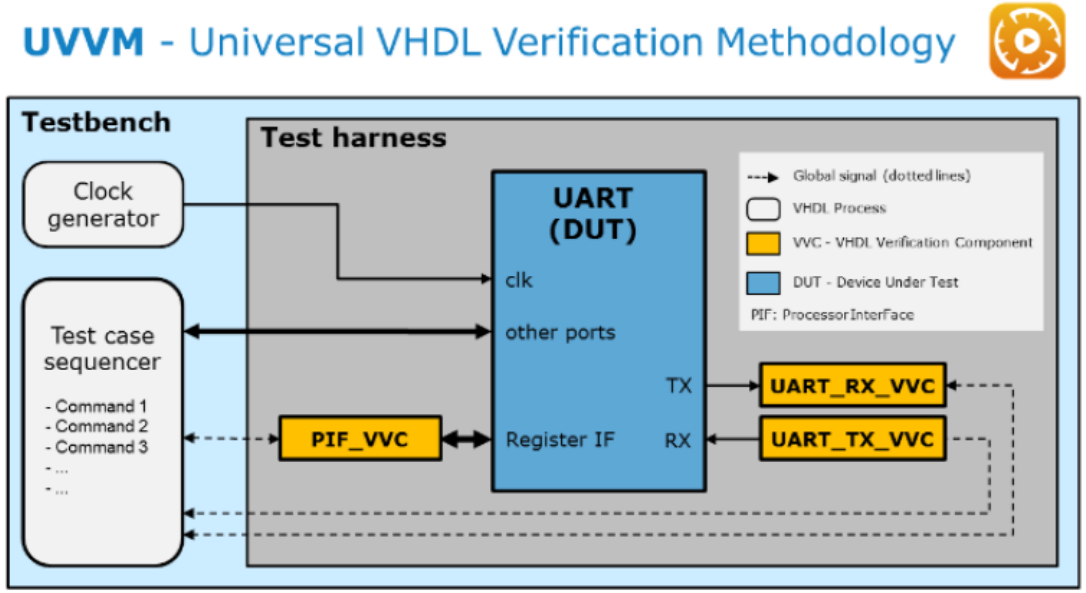
USB to JTAG

Verification methodology

- Management of the complexity
  - multiple ports in
  - multiple ports out
  - priority levels
- Transaction Level Modelling (TLM)
- VHDL - 2008 based
- UVVM (Universal VHDL Verification Methodology)
  Open source
  http://bitvis.no/products/uvvm/
- Similar approach that UVM (in systemVerilog)
- Assertions based verification for the interfaces ports

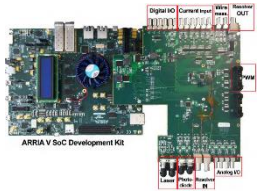






Implementation

BI-BWS LINK



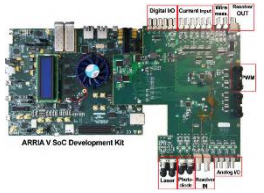
- Master Student will work with me
  for the implementation and the verification environment
  (from September 2016)
- Possibility to include additional requirements of potential users
- Master thesis, code and verification environment will be made accessible to users

Hes·so
Haute Ecole Spécialisée
de Suisse occidentale

ReDS
Reconfigurable & embedded
Digital Systems

Summary

BI-BWS LINK



- Services requirement described for the BWS serial link
- Transport of data and events trough the same channel
- Based on layered architecture of communication systems
- Low level layer for timely constraints signals, events, IO replication, JTAG
- High level layer for transparent mapping of SoC domains, streaming links
- Physical and data link layer could be using GBT defined protocol (tbc)

- Other potential users are welcome to contact me to discuss additional requirements to be include in this implementation

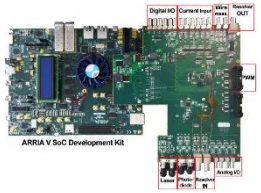
Additional slides

FPGA Architectures

Intelligent Drive FPGA (ID-FPGA)

VME Acquisition and supervision FPGA (AS-FPGA)

BI-BWS LINK



FPGA

EMAC

ARM CPU

Slave ↔ Interface DACs

Slave ↔ PWM

Slave ↔ Motor feedback

Slave ↔ Interface ADCs

EXTERNAL SDRAM Interfaces

events

DMA

Soc bus Master

Soc bus Slave

BWS Hardware Protocole IP

Transceivers

flash interface

Digital IO

Virtual JTAG

FPGA

EXTERNAL SDRAM Interface

VME BUS Interface

CPU

events

Transceivers

BWS Hardware Protocole IP

DMA

Soc bus Master

Soc bus Slave

Virtual JTAG

Digital IO

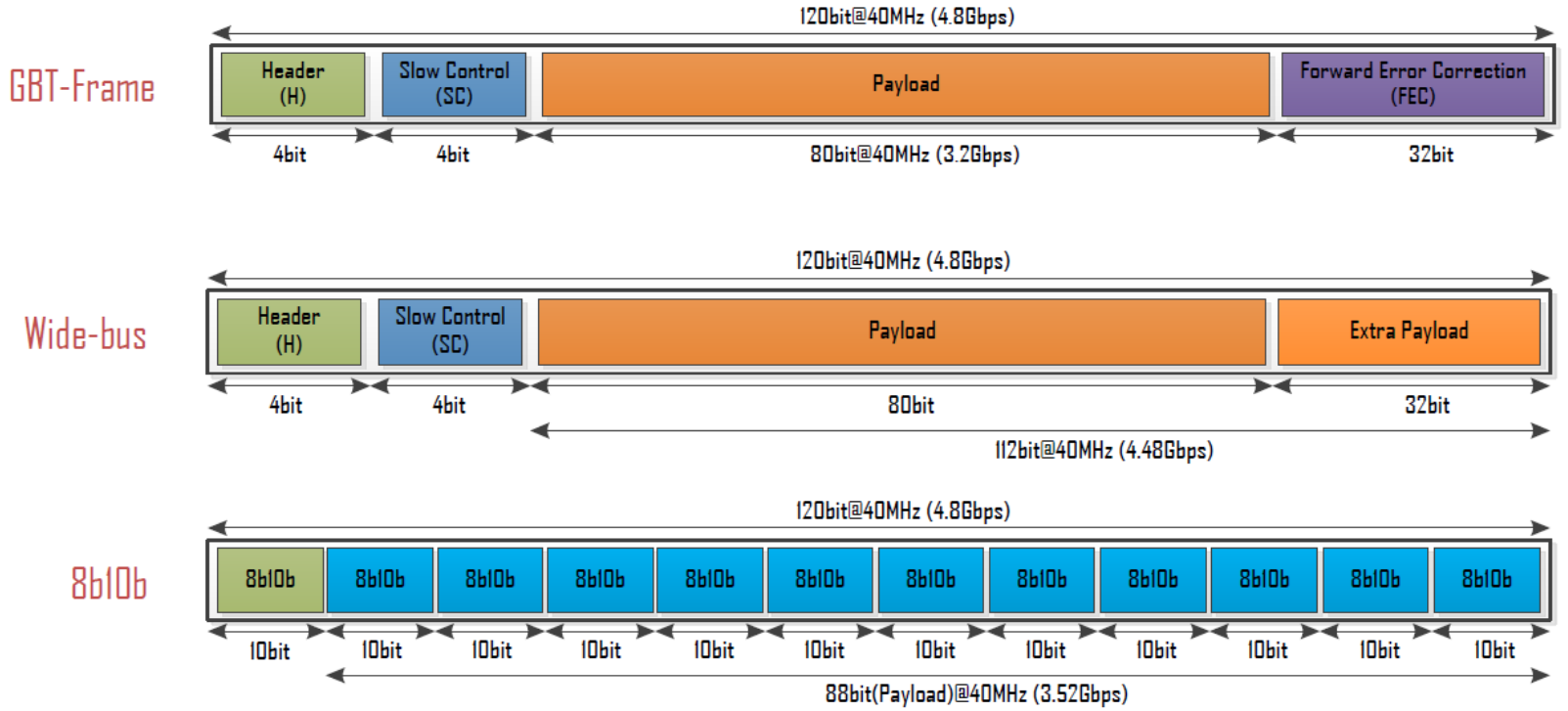
flash interface

The context: "multiple needs" (3 of 5)

PH-ESE-BE

Multiple Configurations

- Encoding



Manoel Barros Slide