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## Real-time Data Acquisition and Processing System for MHz Repetition Rate Image Sensors

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One of the optimization goals of a particle accelerator is to reach the highest possible beam peak current. For that to happen the electron bunch propagating through the accelerator should be kept relatively short along the direction of its travel. In order to obtain a better understanding of the beam composition it is crucial to evaluate the electric charge distribution along the  $\mu\text{m}$ -scale packets. The task of the Electro-Optic Detector (EOD) is to imprint the beam charge profile on the spectrum of light of a laser pulse. The actual measurement of charge distribution is then extracted with a spectrometer based on a diffraction grating.

The article focuses on developed data acquisition and processing system called the High-speed Optical Line Detector (HOLD). It is a 1D image acquisition system which solves several challenges related to capturing, buffering, processing and transmitting large data streams with use of the FPGA device. It implements a latency-optimized custom architecture based on the AXI interfaces. The HOLD device is realized as an FPGA Mezzanine Card (FMC) carrier with single High Pin-Count connector hosting the KIT KALYPSO detector.

The solution presented in the paper is probably one of the world fastest line cameras. Thanks to its custom architecture it is capable of capturing at least 10 times more frames per second than fastest comparable commercially available devices.

### Minioral

Yes

### Description

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