iFDAQ for the COMPASS experiment

Bodlák Martin, Frolov Vladimir, Huber Stefan, Jarý Vladimír, Konorov Igor, Květoň Antonín, Nový Josef, <u>Steffen Dominik</u>, Šubrt Ondřej, Tomsa Jan, Virius Miroslav

Sponsored by:



Bundesministerium für Bildung und Forschung







Contents



- 1. Motivation and Concept of Hardware Event Building
- 2. Design of the intelligent FPGA-based DAQ
 - System
 - Hardware
 - (Firmware)
 - (Software)
- 3. iFDAQ integration and performance in COMPASS
 - Setup of COMPASS spectrometer
 - iFDAQ Performance and Status in 2017/2018
- 4. Switching Network Topology
 - Required Hardware Developments
 - Software Developments
- 5. Outlook and Conclusion

1. Motivation and Concept of Hardware Event Building

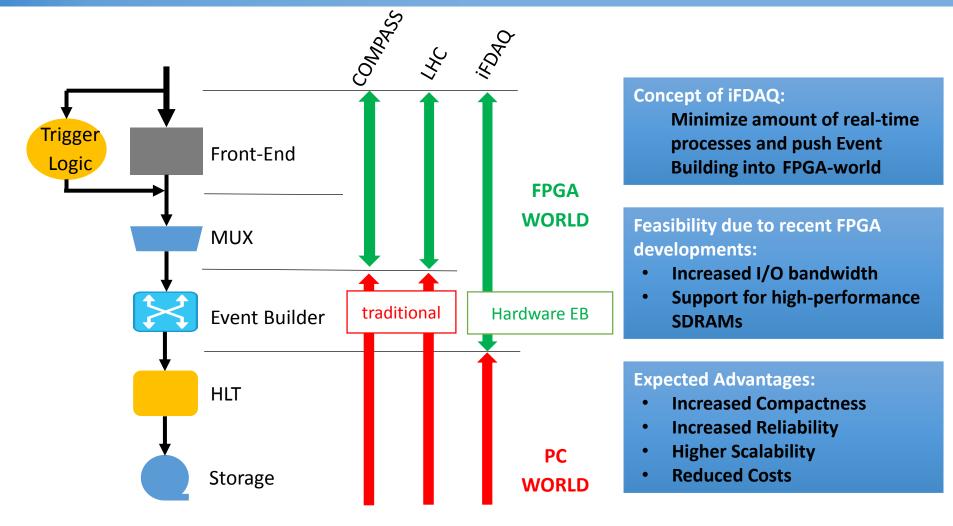
- 2. Design of the intelligent FPGA-based DAQ
 - System
 - Hardware
 - (Firmware)
 - (Software)
- 3. iFDAQ integration and performance in COMPASS
 - Setup of COMPASS spectrometer
 - iFDAQ Performance and Status in 2017
- 4. Switching Network Topology
 - Required Hardware Developments
 - Software Developments
- 5. Outlook and Conclusion

Switching Network Topology

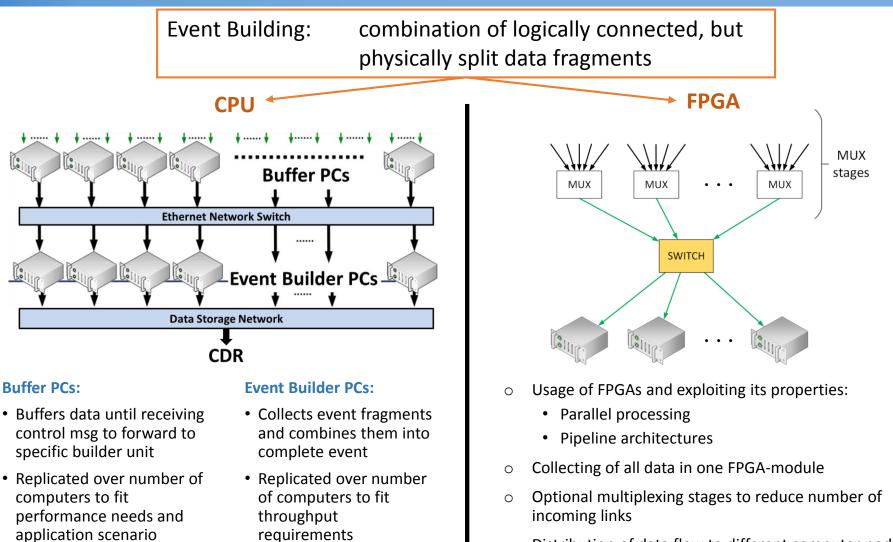
Conclusion

Different DAQ Systems





Event Builder – CPU vs. FPGA



• Distribution of data flow to different computer nodes

MUX

SWITCH

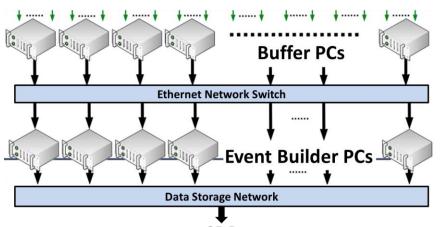
MUX

stages

Event Builder – CPU vs. FPGA



MUX



CPU (sequential)

CĎR

Disadvantages:

- Throughput limited by EB-network
- Performance of sequential execution strongly depends on algorithm complexity
- Recovery of hanging processes takes significant time

Advantages

- Easy integration of redundancy elements
- Uses mass-produced components
- Knowledge and templates available

Advantages:

****↓≠

MUX

- Continuation of the pipeline architecture in FEE
- Only FPGA allows to build real real-time systems
- High scalability
- High reliability
- Reduced costs

Disadvantages:

• Long development

But: Progress in higher-level tools (System Verilog, OSVVM)

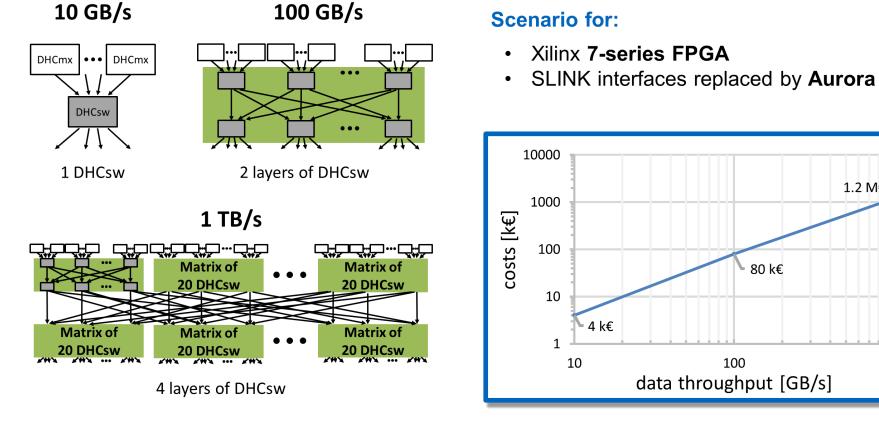
- \Rightarrow Motivation for
 - Minimizing real-time processes
 - Development of highly automatized and reliable DAQ

1.2 M€

Scaling Possibility of Hardware EB







1000

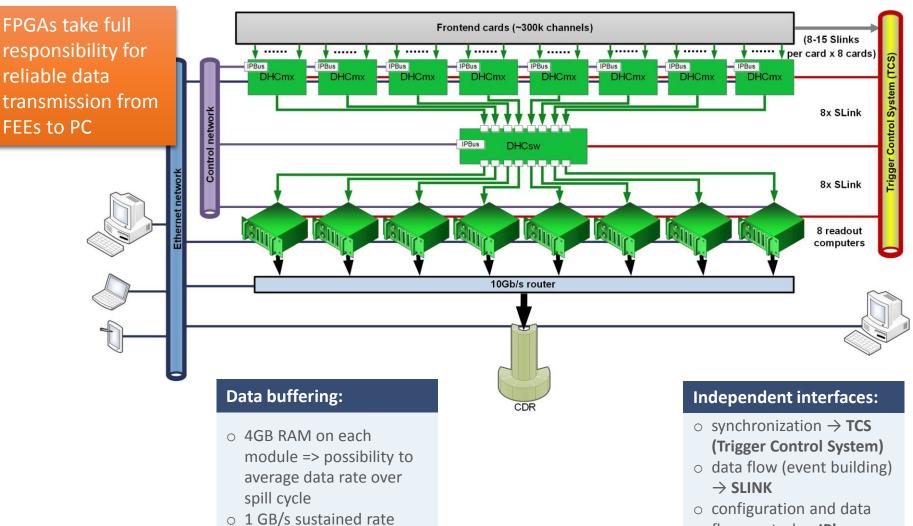
- 1. Motivation and Concept of Hardware Event Building
- 2. Design of the intelligent FPGA-based DAQ
 - System
 - Hardware
 - (Firmware)
 - (Software)
- 3. iFDAQ integration and performance in COMPASS
 - Setup of COMPASS spectrometer
 - iFDAQ Performance and Status in 2017
- 4. Switching Network Topology
 - Required Hardware Developments
 - Software Developments
- 5. Outlook and Conclusion

Switching Network Topology

Conclusion

ERI

iFDAQ – System Design



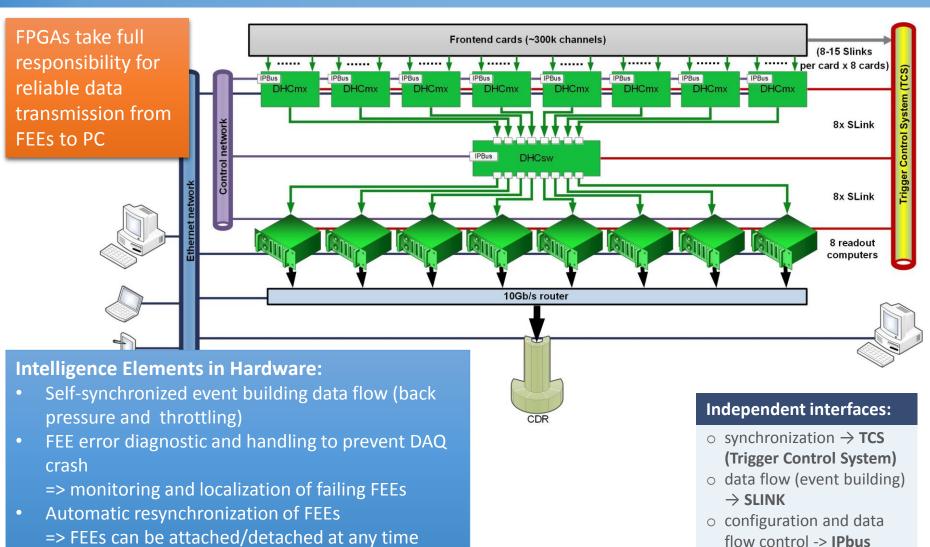
flow control -> IPbus

Switching Network Topology

Conclusion

iFDAQ – System Design





Switching Network Topology

Conclusion

Data Handling Card (DHC)

AMC module

• form factor: AMC standard	
• FPGA: Virtex6 XC6VLX130T	
• memory: 4 GB DDR3 SDRAM	
 • DHCmx 12:1 multiplexer [1] • DHCsw 8x8-switch 	
O data rate: 3500 Absolute limit 3000 2500 2500 2000 2000 2000 2000 2000 2000 1500 1000 100 1000 100 1000 100 1000	0000

VME carrier card

 $\circ\,$ form factor:

6 U VME

- o interfaces:
- TCS (Trigger Control System) receiver
- 1 Gb Ethernet for control network (IPbus)
- 16 serial data links (SLINK)
- JTAG for backup programming of FLASH



- 1. Motivation and Concept of Hardware Event Building
- 2. Design of the intelligent FPGA-based DAQ
 - System
 - Hardware
 - (Firmware)
 - (Software)
- 3. iFDAQ integration and performance in COMPASS
 - Setup of COMPASS spectrometer
 - iFDAQ Performance and Status in 2017 and 2018
- 4. Switching Network Topology
 - Required Hardware Developments
 - Software Developments
- 5. Outlook and Conclusion

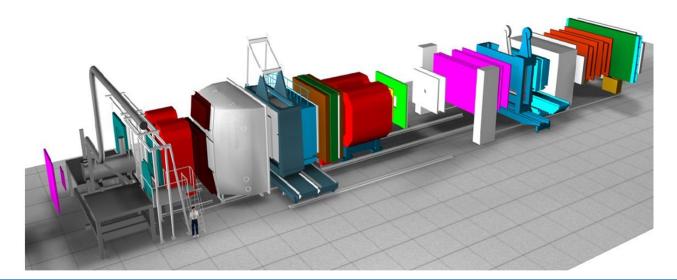
Switching Network Topology



COmmon Muon Proton Apparatus for Structure and Spectroscopy

COMPASS – Overview

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
- High intensity beams: $4 \cdot 10^7 \frac{\mu}{s}$; $2 \cdot 10^7 \frac{\text{hadrons}}{s}$
- Multi-purpose experiment
- Start of data-taking: 2001
- Since 2014: New DAQ with hardware event builder (iFDAQ)

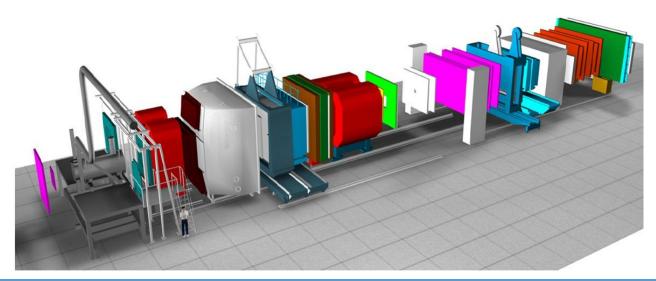


COMPASS – Spectrometer Setup

	spectrometer fa	icts
٠	Length:	60m
•	Amount of channels:	300.000
٠	Trigger rate:	30 kHz
٠	On-spill data rate:	1.5 GB/s
٠	Event size:	20-50 kB

Source [2]

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
- High intensity beams: $4 \cdot 10^7 \frac{\mu}{s}$; $2 \cdot 10^7 \frac{\text{hadrons}}{s}$
- Multi-purpose experiment
- Start of data-taking: 2001
- Since 2014: New DAQ with hardware event builder (iFDAQ)



iFDAQ in COMPASS – Hardware Parts

- Very compact: 30 online PC in former DAQ
 Now: 1 VME crate (6-U) + one rack (8 computers)
- Highly flexible: Easily adaptable to different spectrometer setups (e.g. DVCS 2017 vs. Drell Yan 2018)

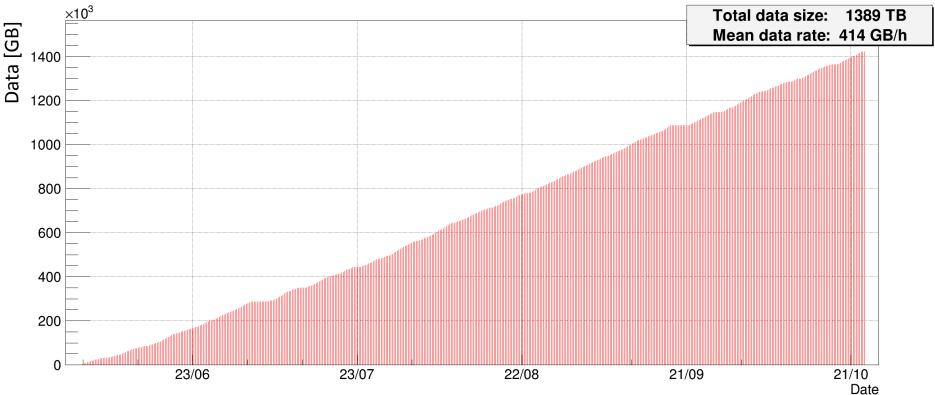






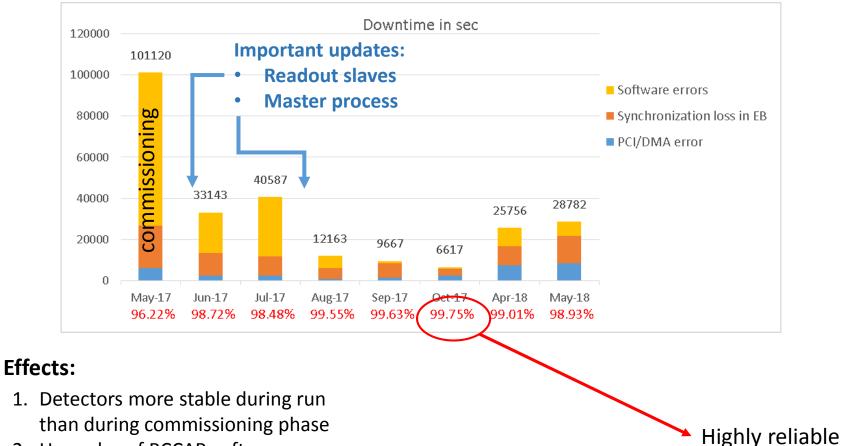
Performance – Accumulated Data 2017





CERN

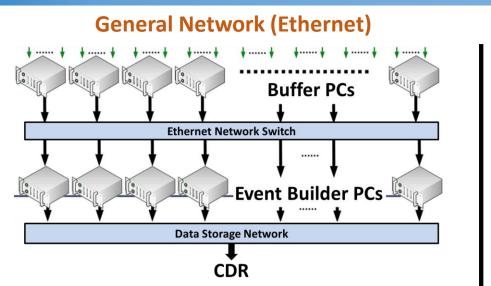
Performance – Uptime in 2017



2. Upgrades of RCCAR software

- 1. Motivation and Concept of Hardware Event Building
- 2. Design of the intelligent FPGA-based DAQ
 - System
 - Hardware
 - (Firmware)
 - (Software)
- 3. iFDAQ integration and performance in COMPASS
 - Setup of COMPASS spectrometer
 - iFDAQ Performance and Status in 2017
- 4. Switching Network Topology
 - Required Hardware Developments
 - Software Developments
- 5. Outlook and Conclusion

General Network vs. Point-to-Point



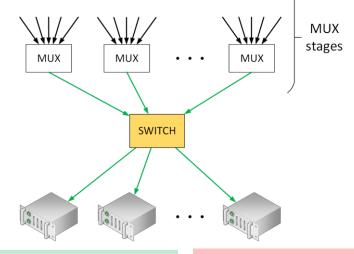
Advantages

- Easy integration of redundancy elements (traffic shaping according to load on nodes)
- Usage of massproduced components and standards

Disadvantages:

- Throughput limited by EB-network switch
- Inefficient usage of max. bandwith due to:
 - Improper comm. pattern (N senders -> 1 receiver) => network congestion
 - Data overhead due to addressing etc.

Point-to-Point



Advantages:

- Independence of network switch
- Efficient usage of link bandwidth (no addressing etc.)
- High reliability

Disadvantages:

- Strong dependence on reliability of network nodes (no rerouting possibility in case of hardware failure)
- No possibility for dynamic network optimization (e.g. load balancing)

CERN

Crosspoint Switch - Integration

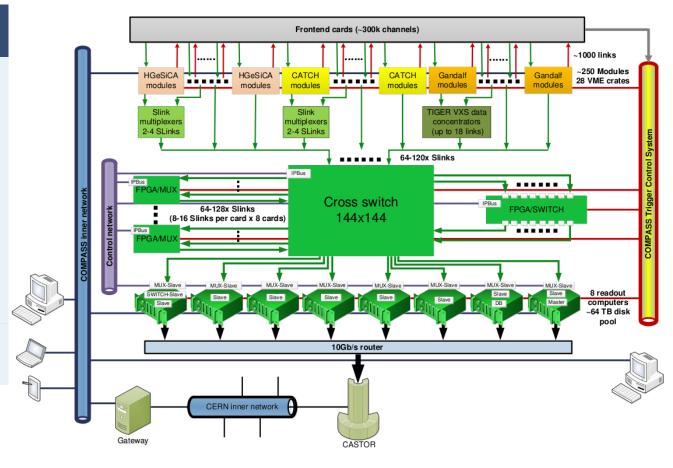
Crosspoint Switch

\circ connects:

- FE electronics
- DHCmx modules
- DHCsw module
- Spillbuffers

o purpose:

- Ease of load balancing
- System redundancy to compensate hardware failures
- ⇒ provides fully customizable network topology



Crosspoint Switch – Hardware Design



Crosspoint Switch Components

○ interfaces:

- 12 x 12 channel CXP transceiver (MPO fiber connectors)
- Ethernet for IPbus
- JTAG
- TCS (Trigger Control System) receiver

• Switching and Control:

- Vitesse VSC3144-02 fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
- Xilinx Artix-7 FPGA for switch control and monitoring



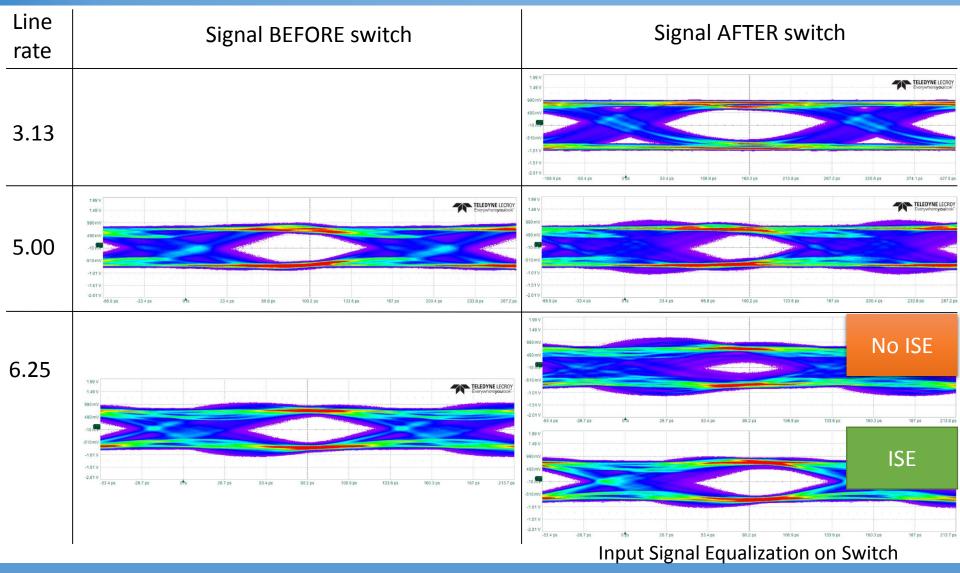


Interface FPGA – Crosswitch:

- 90 MHz, 11-bit parallel data bus
- Multiple program assignments can be queued and issued simultaneously \Rightarrow fast programming (<< 1us)

Crosspoint Switch – Hardware Test





- 1. Motivation and Concept of Hardware Event Building
- 2. Design of the intelligent FPGA-based DAQ
 - System
 - Hardware
 - (Firmware)
 - (Software)
- 3. iFDAQ integration and performance in COMPASS
 - Setup of COMPASS spectrometer
 - iFDAQ Performance and Status in 2017
- 4. Switching Network Topology
 - Required Hardware Developments
 - Software Developments
- 5. Outlook and Conclusion



Ongoing development:

- Integration of crosspoint switch
 - -> test of crosspoint switch successful and promising
 - -> integration of the hardware for the crosspoint switch (results to be expected soon)
 - -> upgrade of Software for automatic identification of malfunctioning hardware parts

Ideas for the Future:

- upgrade of TCS to bidirectional PON (passive optical network) with use of Universal Communication Framework (UCF) developed at TUM for on-the-fly reconfiguration of interconnections
- Minimizing of real-time processes
 - -> direct writing of data onto SSD

Conclusion



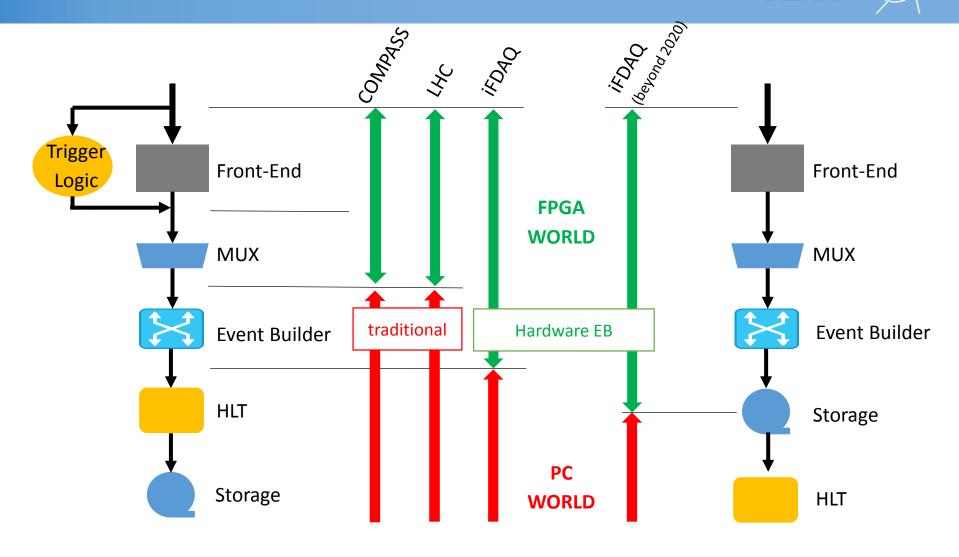
- \circ Improvements since commissioning of iFDAQ in 2014:
 - Increased reliability (Uptime around 99%)
 - Extended intelligence elements in software:
 - -> Automatic safe stop of the run for self-recovery
 - -> Continuously running
 - No event size limit due to upgrades in firmwares
- Performance in 2017:
 - Data rate: 91.7 MB/s (average)
 250 MB/s (in stable beam conditions)
 380 MB/s (peak sustained rate)
 - On-spill data rate: 1.5 GB/s
- o iFDAQ transferred to other HEP experiment (NA64)

Switching Network Topology

Conclusion

ERI

Possible DAQ Systems



THANK YOU for your Attention





- [1] Y. Bai et al., *New data acquisition system for the COMPASS experiment*, in proceedings of *Topical Workshop on Electronics for Particle Physics (TWEPP)*, Lisbon Portugal September 2015
- [2] COMPASS collaboration, P. Abbon et al., *The COMPASS experiment at CERN, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip., 577(3):455-518, 2007.*

Backup slides

DHC – Data error handling in firmware

Data Consistency Check:

- Transmission errors detected by S-Link
- Truncation, i.e. mismatch between real and declared data block size
- $\circ\,$ Inconsistency of event label
- Missing data -> timeout



Error handling

- o Discarding/throttling of wrong data
- o Adding of specific header for empty frame
- Setting error flag in local register (diagnostics of FEE errors)



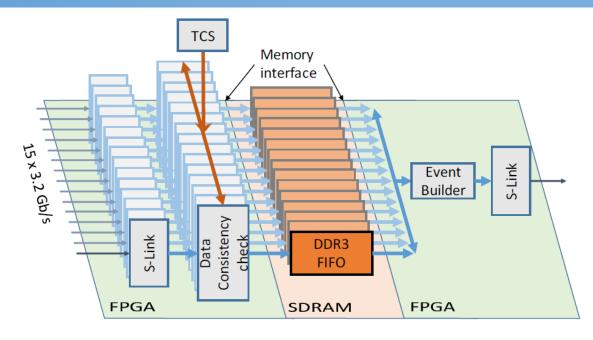
iFDAQ in **COMPASS**

Redundancy Logic

Conclusion



Firmware – DHCmx

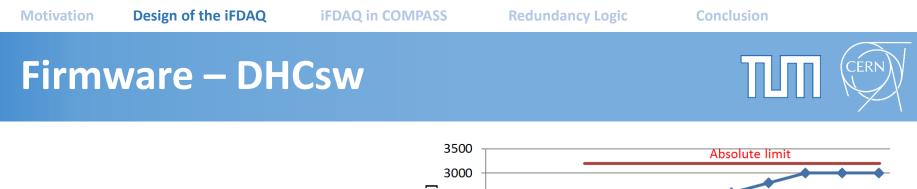


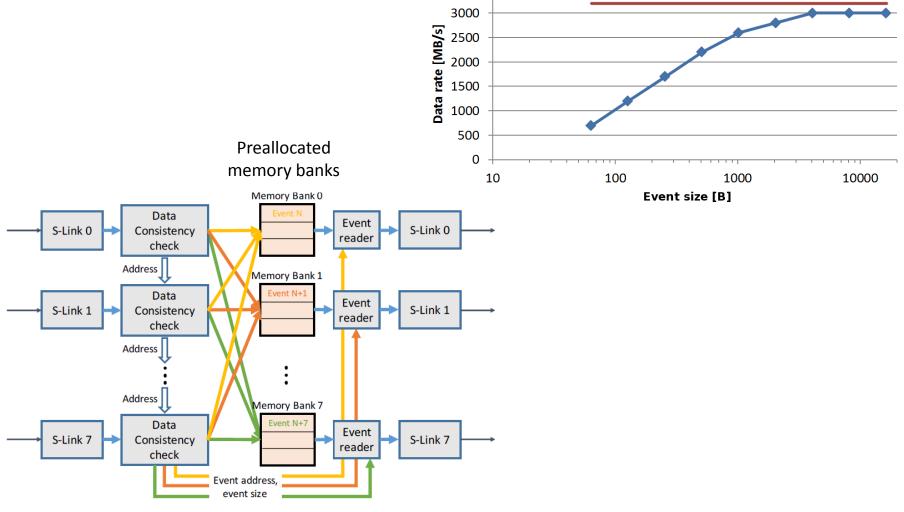
Data Consistency Check:

- $\,\circ\,$ Transmission errors detected by S-Link
- Truncation, i.e. mismatch between real and declared data block size
- Inconsistency of event label
- Missing data -> timeout

Error detected

- Discarding/throttling of wrong data
- Adding of specific header
- Setting error flag in local register





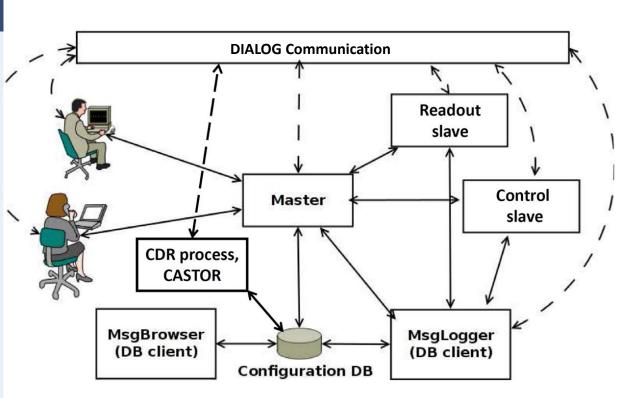
RCCAR software

Run Control, Configuration, And Readout Software (RCCARS):

- o Multilayer system around master process
 - master: Middleman between GUI, DB, all other processes
 - GUIs

display overall status of iFDAQ, control behavior of iFDAQ (when in Control mode)

- readout slaves (only real-time processes) readout of data, analysis of events, error check, transformation into DATE-format, distribution to monitoring tools, writing to HDD
- control slaves
 monitoring and control of hardware nodes
- message logger collection of msgs from processes, storing msgs in DB
- message browser display of msgs and support for advanced filtering
- Central Data Recording (CDR) transfer of raw data to CASTOR, disk cleaning for new data
- Inter-process communication via DIALOG library (Custom-developed server/client communication)



ICHEP 2017 Paris

RCCAR software

Run Control, Configuration, And Readout Software (RCCARS):

- Multilayer system around master process
 - master: Middleman between GUI, DB, all other processes
 - GUIs

•

•

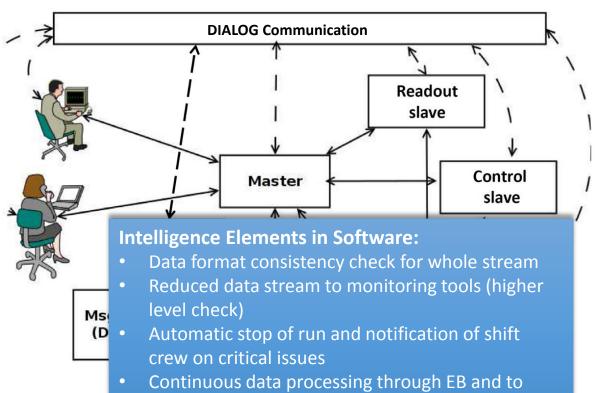
display overall status of iFDAQ, control behavior of iFDAQ (when in Control mode)

 readout slaves (only real-time processes) readout of data, analysis of events, error check, transformation into DATE-format, distribution to monitoring tools, writing to HDD

control slaves monitoring and control of hardware nodes

 message logger collection of msgs from processes, storing msgs in DB

- message browser display of msgs and support for advanced filtering
- Central Data Recording (CDR) transfer of raw data to CASTOR, disk cleaning for new data
- Inter-process communication via DIALOG library (Custom-developed server/client communication)



monitoring tools (Start of run just enables data writing to disk)

Motivation

Redundancy Logic

Conclusion



Run Control & Node Status GUI

Note: were were were were were were were we			Link	status			×
2 3 6 7 7 0 0 0 1 2 3 4 5 6 7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	hanges not enabled Enable changes Disable changes						
2 3 6 7 7 0 0 0 1 2 3 4 5 6 7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	MUX01 - source id 945	MUX02 - s	purce id 946	MUX03 - sr	purce id 947	MUXC	04 - source id 948
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15						
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	2 978 977 976 16 17 606 607 608 609 997 996 460 1008 1007	100€ 145 961 1012 144 980 381 3	82 257 999 998 989 988 987 986	1000 1009 250 740 739 738 737 6	24 625 626 627 628 <mark>258 256</mark> 983	981 380 979 984 1010 982 1	146 501 991 990 960 1004 1003 1011 1002
1 Deta accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number:	err	err err err err err err	err err err err err err err	err err err err err err e	err err err err err <mark>err err</mark> err	err err err err err	err err err err err err err err
1 Deta accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number:	OAD LOAD LOAD LOAD LOAD LOAD LOAD LOAD L	LOAD LOAD LOAD LOAD LOAD LOAD LOAD LOAD	DAD LOAD LOAD LOAD LOAD LOAD LOAD	LOAD LOAD LOAD LOAD LOAD LOAD LOAD	DAD LOADLOADLOADLOAD LOAD LOAD	LOAD LOAD LOAD LOAD LOAD LOAD LOAD L	OAD LOAD LOAD LOAD LOAD LOAD LOAD LOAD
1 Deta accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number: 53 Data accepted C5: 1050300 Data detail Self number:							
trumber: 9927 Data accepted PS: 141745374 Data decide PS: 10190714 Data accepted PS: 1250374 Data accepted PS: 1250374 <thdata 1250374<="" accepted="" ps:="" th=""> Data accepted</thdata>	0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0	0% 0% 0% 0% 0% 0% 0% 0	0% 0% 0% 0% 0% 0% 0% 0%	0% 0% 0% 0% 0% 0% 0% 0	0% 0% 0% 0% 0% 0% 0% 0%	0% 0% 0% 0% 0% 0%	0% 0% 0% 0% 0% 0% 0% 0%
trumber: 9927 Data accepted PS: 141745374 Data decide PS: 10190714 Data accepted PS: 1250374 Data accepted PS: 1250374 <thdata 1250374<="" accepted="" ps:="" th=""> Data accepted</thdata>	Enill number: 52 Data acconted CS: 110502600 Data detail	Enill number: 52 Data a	contod CS: 119600254 Data datail	Enill number: 52	conted CS: 65033620 Data detail	Enill number: E3	ata accepted CEL 07464205 Data detail
Outgoing pert UP Outgoing pert UP <th< th=""><th></th><th></th><th>·</th><th></th><th></th><th></th><th></th></th<>			·				
HUX05 HUX05 <th< th=""><th> · · ·</th><th></th><th>·</th><th></th><th>·</th><th></th><th></th></th<>	· · ·		·		·		
2 3 6 7 9 10 11 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 9 12 12 3 4 5 6 7 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6					g port. or		comp porce of
All or all of		MU		MU			
arr a		1 2 3 4 5 6 7	8 9 10 11 12 13 14 15	1 2 3 4 5 6 7	8 9 10 11 12 13 14 15	1 2 3 4 5 6	7 8 9 10 11 12 13 14 15
a b b b b b b b b b b b b b b b b b b b			<u> </u>				
number: 53 Data accepted C5: 41793595 Data accepted C5: 0 Data accepted C5: 0 <td>en en e</td> <td>en en en en en en er er</td> <td>an en en en en en en en</td> <td></td> <td>en en en en en en en err</td> <td>en en en en err err</td> <td>en en en en en en en en en</td>	en e	en en en en en en er er	an en en en en en en en		en en en en en en en err	en en en en err err	en en en en en en en en en
number: 53 Data accepted C5: 41793595 Data accepted C5: 0 Data accepted C5: 0 <th></th> <th></th> <th>JAULOAULOAULOAULOAULOAULOAULOAU</th> <th></th> <th>JAULOAULOAULOAULOAULOAULOAULOAULOAU</th> <th></th> <th>OADLOADLOADLOADLOADLOADLOADLOAD</th>			JAULOAULOAULOAULOAULOAULOAULOAU		JAULOAULOAULOAULOAULOAULOAULOAULOAU		OADLOADLOADLOADLOADLOADLOADLOAD
Data accepted P5: 53973120 Data defail Data accepted P5: 0 Data accepted P5: 0 </th <th>0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0</th> <th>24% 24% 24% 24% 24% 24% 24% 24% 2</th> <th>4% 24% 24% 24% 24% 24% 24% 24%</th> <th>24% 24% 24% 24% 24% 24% 24% 24%</th> <th>4% 24% 24% 24% 24% 24% 24% 24%</th> <th>24% 24% 24% 24% 24% 24% 24%</th> <th>24% 24% 24% 24% 24% 24% 24% 24% 24%</th>	0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0% 0	24% 24% 24% 24% 24% 24% 24% 24% 2	4% 24% 24% 24% 24% 24% 24% 24%	24% 24% 24% 24% 24% 24% 24% 24%	4% 24% 24% 24% 24% 24% 24% 24%	24% 24% 24% 24% 24% 24% 24%	24% 24% 24% 24% 24% 24% 24% 24% 24%
Data accepted P5: 53973120 Data defail Data accepted P5: 0 Data accepted P5: 0 </th <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>							
Outgoing part: UP No info No info No info ct 0 + MUX01 - source id: 947 Port 3 - MUX03 - source id: 947 Port 3 - MUX04 - source id: 948 Port 4 - MUX05 - source id: 948 Port 5 - MUX07 Port 7 - MUX08 errors	Spill number: 53 Data accepted CS: 41793505 Data detail	Spill number: x Data ad		Spill number: x Data ad		Spill number: x Di	
tt 0 - MUX01 - Source id: 945 Port 2 - MUX03 - source id: 947 Port 3 - MUX04 - Source id: 949 Port 5 - MUX06 Port 6 - MUX07 Port 7 - MUX08 errors err	Event number: 93884 Data accepted PS: 53973129 Data detail	Event number: x Data ar		Event number: x Data ad		Event number: x Da	
errors Data accepted PS: S44712032 Data detail Data accepted PS: S44712032 Data detail Port 8 - PCCORE11 Port 9 - PCCORE12 Port 10 - PCCORE13 Port 11 - PCCORE14 Port 12 - PCCORE15 Port 13 - PCCORE16 Port 14 - PCCORE17 Port 13 - PCCORE18 errors <	Outgoing port: UP	No	info	No	info	1	No info
errors Data accepted PS: S44712032 Data detail Data accepted PS: S44712032 Data detail Port 8 - PCCORE11 Port 9 - PCCORE12 Port 10 - PCCORE13 Port 11 - PCCORE14 Port 12 - PCCORE15 Port 13 - PCCORE16 Port 14 - PCCORE17 Port 13 - PCCORE18 errors <	Port 0 MUV01 course id: 045 Port 1 MUV02 course id: 046	Port 2 MUV02 course id: 0.47	Port 2 MUX04 course id: 049	Port 4 MUXOE course id: 040	Dort 5 MUV06	Doct 6 MUV07	Port 7 MUV00
18% 19% 11% 16% 7% 0% 0% 0% 0% 0%			+		1012 5 - 1107.000	1010 0 - 100007	TOTE 7 - MOXOO
Switch - source id: 944 number: 53 Event number: 95063 Data accepted CS: 429524189 Data detail Data accepted PS: 544712032 Data detail Port 8 - PCCORE11 Port 9 - PCCORE12 Port 10 - PCCORE13 Port 11 - PCCORE14 Port 12 - PCCORE15 Port 13 - PCCORE16 Port 14 - PCCORE17 Port 15 - PCCORE18 errors er							
protest 53 Event number: 95063 Data accepted CS: 429524189 Data detail Data accepted PS: 544712032 Data detail Port 8 - PCCORE11 Port 9 - PCCORE12 Port 10 - PCCORE13 Port 11 - PCCORE14 Port 12 - PCCORE15 Port 13 - PCCORE16 Port 14 - PCCORE17 Port 15 - PCCORE18 errors	18% 19%	11%	16%	7%	0%	0%	0%
Port 8 - PCCORE11 Port 9 - PCCORE12 Port 10 - PCCORE13 Port 11 - PCCORE14 Port 12 - PCCORE15 Port 13 - PCCORE16 Port 14 - PCCORE17 Port 15 - PCCORE18 errors errors <td></td> <td></td> <td>Switch - so</td> <td>ource id: 944</td> <td></td> <td></td> <td></td>			Switch - so	ource id: 944			
errors	Spill number: 53 Event number	er: 95063	Data accepted CS:	429524189	Data detail Data accepte	ed PS: 544712032	Data detail
pccore11 pccore12 pccore13 pccore14 pccore15 pccore16 pccore16 <th< th=""><th>Port 8 - PCCORE11 Port 9 - PCCORE12</th><th>Port 10 - PCCORE13</th><th>Port 11 - PCCORE14</th><th>Port 12 - PCCORE15</th><th>Port 13 - PCCORE16</th><th>Port 14 - PCCORE17</th><th>Port 15 - PCCORE18</th></th<>	Port 8 - PCCORE11 Port 9 - PCCORE12	Port 10 - PCCORE13	Port 11 - PCCORE14	Port 12 - PCCORE15	Port 13 - PCCORE16	Port 14 - PCCORE17	Port 15 - PCCORE18
pccore11 pccore12 pccore13 pccore14 pccore15 pccore16 pccore16 <th< td=""><td>errors errors</td><td>errors</td><td>errors</td><td>errors</td><td>errors</td><td>errors</td><td>errors</td></th<>	errors errors	errors	errors	errors	errors	errors	errors
errors)					
errors							
number: 94696 Fill level: 0% fill level: 0% fill level: 0% fill level: 24%	pccorel1 pccorel2	pccore13	pccore14	pccore15	pccorel6		nde Status GLII
3% CPU: 3% CPU: 5% CPU: 2% CPU: 24% CPU: 24% CPU: 24% CPU: 24% CPU: 24% Memory: 24% Memory:<			·		pccore16		ode Status GUI:
ry: 7% Memory: 7% Memory: 7% Memory: 7% Memory: 7% Memory: 9% Memory: 24% Memo	errors errors	errors	errors	errors	errors	error	ode Status GUI:
71% HDD: 69% HDD: 73% HDD: 71% HDD: 24% HDD: 24% HDD: Data accepted CS: 000000000000000000000000000000000000	errors errors ill level: 0% Fill level: 0%	errors Fill level: 0%	errors Fill level: 0%	errors Fill level: 24%	errors Fill level: 24%	Eill level:	
71% HDD: 69% HDD: 73% HDD: 71% HDD: 24% HDD: 24	errors errors II level: 0% Fill level: 0% PU: 3% CPU: 3%	errors Fill level: 0% CPU: 5%	errors Fill level: 0% CPU: 2%	errors Fill level: 24% CPU: 24%	errors Fill level: 24% CPU: 24%	Fill level:	System overview: s
accepted PS: 0 Data accept	errors errors iil level: 0% Fill level: 0% .PU: 3% CPU: 3% temory: 7% Memory: 7%	errors Fill level: 0% CPU: 5% Memory: 7%	errors Fill level: 0% CPU: 2% Memory: 9%	errors Fill level: 24% CPU: 24% Memory: 24%	errors Fill level: 24% CPU: 24% Memory: 24%	error Fill level:	System overview: s
umber: 53 number: 94696 Spill number: 53 Event number: 94987 Spill number: 53 Event number: 94402 Spill number: 53 Event number: 94111 Spill number: 0 O Control of front-end	errors errors II level: 0% Fill level: 0% PU: 3% CPU: 3% lemory: 7% Memory: 7% DD: 71% HDD: 69%	errors Fill level: 0% CPU: 5% Memory: 7% HDD: 73%	errors Fill level: 0% CPU: 2% Memory: 9% HDD: 71%	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24%	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24%	erro: Fill level:	System overview: s all nodes of hardwa
number: 94696 Event number: 94987 Event number: 94402 Event number: 94111 Event number: 0 Event number: 0 Event number: 0	errors errors ill level: 0% Fill level: 0% IPU: 3% CPU: 3% temory: 7% Memory: 7% IDD: 71.% HDD: 69% abta accepted CS: 372354 Data accepted CS: 62953	errors Fill level: 0% CPU: 5% Memory: 7% HDD: 73% Data accepted CS: 97974	errors Fill level: 0% CPU: 2% Memory: 9% HDD: 71% Data accepted CS: 826360	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted C5: 0	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted C5: 0	erro Fill level:	System overview: s all nodes of hardwa
	errors errors ill level: 0% Fill level: 0% iPU: 3% CPU: 3% temory: 7% Memory: 7% IDD: 71% HDD: 69% acate accepted CS: 372354 Data accepted PS: 0 bata accepted PS: 0 Data accepted PS: 0	errors Fill level: 0% CPU: 5% Memory: 7% HDD: 73% Data accepted CS: 97974 Data accepted PS: 4453	errors Fill level: 0% CPU: 2% Memory: 9% HDD: 71% Data accepted CS: 826360 Data accepted PS: 6954	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0	erro Fill level:	System overview: s all nodes of hardwa builder
	errors errors ill level: 0% Fill level: 0% IPU: 3% CPU: 3% temory: 7% Memory: 7% DDD: 71% HDD: 69% bata accepted CS: 372354 Data accepted CS: 629953 Data accepted CS: 629953 pata accepted PS: 0 Dpl number: 53 Spill number: 53	errors Fill level: 0% CPU: 5% Memory: 7% HDD: 73% Data accepted CS: 97974 Data accepted PS: 4453 Spill number: 53	errors Fill level: 0% CPU: 2% Memory: 9% HOD: 71% Data accepted CS: 826360 Data accepted PS: 6954 Spill number: 53	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0 Spill number: 0	erro Fill level:	System overview: s all nodes of hardwa builder
ange monitoring prescaling Change monitoring prescaling Change monitoring prescaling Change monitoring prescaling Change monitoring prescaling	errors errors ill level: 0% Fill level: 0% IPU: 3% CPU: 3% temory: 7% Memory: 7% DDD: 71% HDD: 69% bata accepted CS: 372354 Data accepted CS: 629953 Data accepted CS: 629953 pata accepted PS: 0 Dpl number: 53 Spill number: 53	errors Fill level: 0% CPU: 5% Memory: 7% HDD: 73% Data accepted CS: 97974 Data accepted PS: 4453 Spill number: 53	errors Fill level: 0% CPU: 2% Memory: 9% HOD: 71% Data accepted CS: 826360 Data accepted PS: 6954 Spill number: 53	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0 Spill number: 0	erro Fill level:	System overview: s all nodes of hardwa builder Control of front-en
excluding of front-e	errors errors II level: 0% Fill level: 0% PU: 3% CPU: 3% emory: 7% Memory: 7% DD: 71% HDD: 69% at a accepted CS: 372354 Data accepted CS: 62953 at a accepted PS: 0 Spill number: 53 event number: 94696 Event number: 94987 onitoring prescaler 100 0 \$	errors Fill level: 0% CPU: 5% Memory: 7% HDD: 73% Data accepted CS: 97974 Data accepted PS: 4453 Spill number: 53 Event number: 94402 Monitoring prescaler 100	errors Fill level: 0% CPU: 2% Memory: 9% HDD: 71% Data accepted C5: 826360 Data accepted P5: 6954 Spill number: 53 Event number: 9111 Monitoring prescaler 100 100	errors Fill level: 24% CPU: 24% HDD: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0 Spill number: 0 Event number: 0 Monitoring prescaler 0	errors Fill level: 24% CPU: 24% Memory: 24% HDD: 24% Data accepted CS: 0 Data accepted PS: 0 Spill number: 0 Event number: 0 Monitoring prescaler: 0	erro Fill level: CPU: Memory: HDD: Data accepted CS: Data accepted CS: Data accepted PS: Spill number: Spill number: Change monitod	System overview: s all nodes of hardwa builder Control of front-en allows easy online

Dominik Steffen | Real Time – Williamsburg | 14/06/2018

into DAQ and reloading of front-

end modules

Switching Network Topology

Hardware: Vitesse VSC3144

- 144 x 144 strictly non-blocking cross-point switch
- Up to 6.5 Gbps bandwidth per port
- No registers used in data path i.e. asynchronous data path => no restrictions on the phase, frequency, or signal pattern of any input (protocol independent)
- 45mm x 45mm 1072-pin BGA package
- Core programming on port-by-port basis OR simultaneous issuing of multiple queued assignments

