Final design of the readout system for Triple-GEM detectors for the CMS forward muon upgrade

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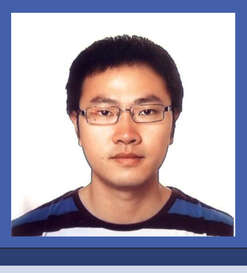
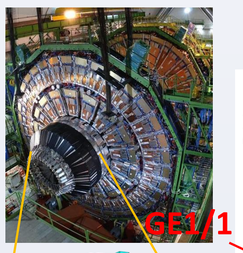
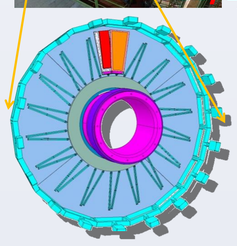
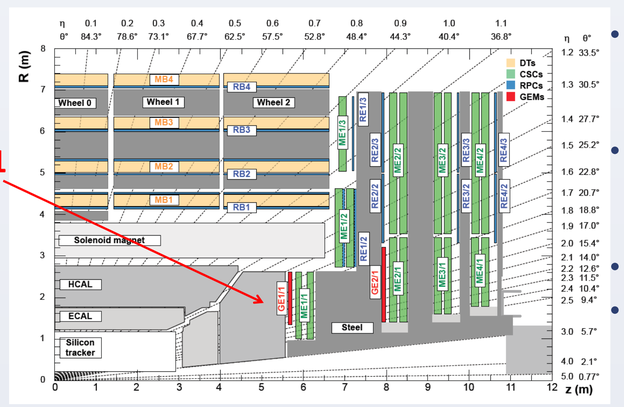


Introduction

The CMS Collaboration will install trapezoidal Triple-GEM detectors, with dimensions (990x440-220) mm^2 in the forward region, $|\eta| > 1.6$, of the CMS muon spectrometer. Triple-GEM detectors can provide precision tracking and fast trigger information, contributing on one hand to provide missing redundancy in the high-η region and on the other hand to the improvement of the CMS muon trigger.



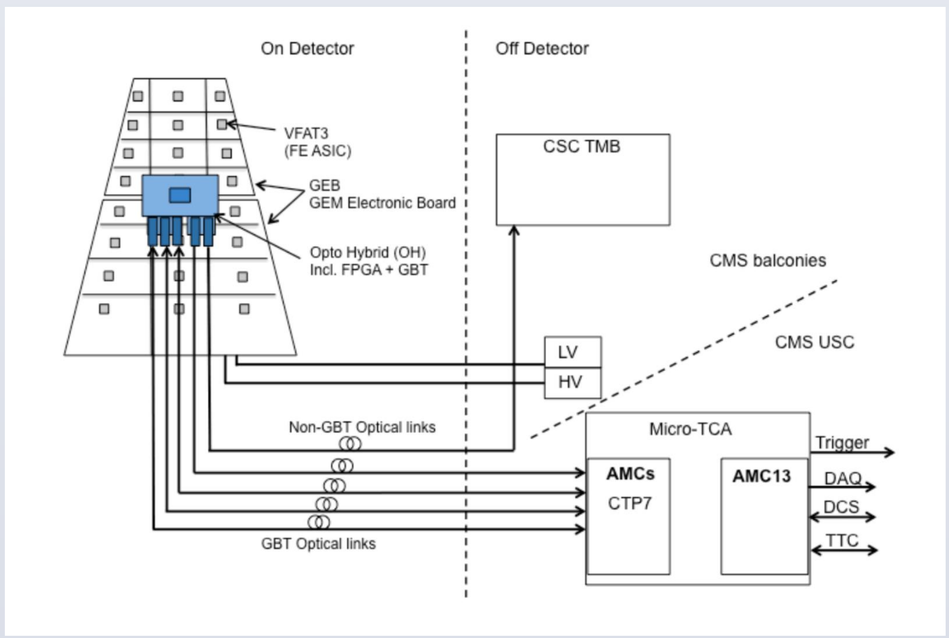




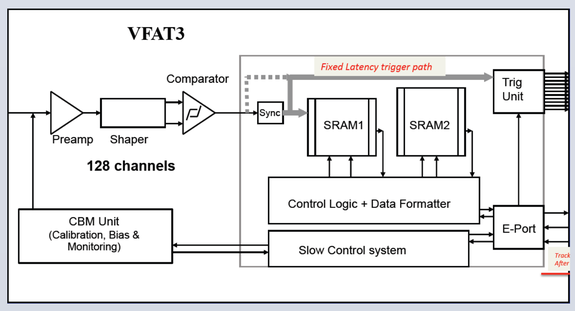
- Restore redundancy in μ system for robust tracking & triggering
- Improve L1 & HLT muon momentum resolution
- Reduce global μ rate
- Ensure ~100% trigger efficiency with high pile Up

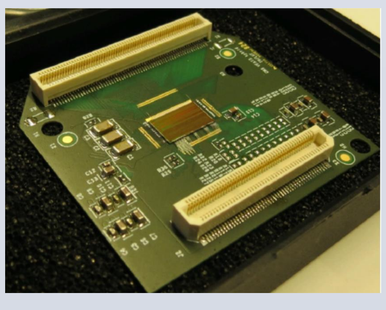
DAQ system architecture

The CMS Triple-GEM detectors are composed of 8 segments in η and 3 columns in φ. Each segment will be readout out with the new Front-End electronics VFAT3 [1]. This binary chip counts 128 channels. It can provide fast "trigger" signals at LHC clock frequency, 40 MHz, as well as "tracking data" upon the CMS Level1 trigger signal. The "trigger" data consists of a fast 'OR' of 2 strips while the "tracking data" corresponds to the the full granularity of the detector. Trigger and tracking data are sent to the μTCA off-detector electronics located in the CMS service cavern through the CERN Versatile Link. The trigger data are also sent to the Cathode Strip Chamber (CSC) Trigger Mother Board (TMB) to improve the Level-1 trigger efficiency of the CSCs.



The VFAT3 chip





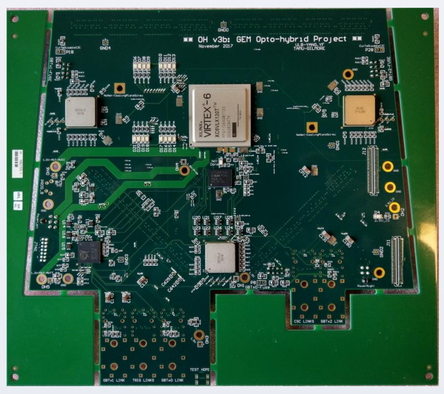
- Binary chip
- Programmable shaping time : 25, 50, 100, 250, 500 ns
- Internal calibration
- Direct interface to GBT @ 320 Mbps
- 8 Sbits to FPGA @ 320 Mbps
- Designed for rate up to 10 kHz/cm^2
- L1 latency up to 20 μs

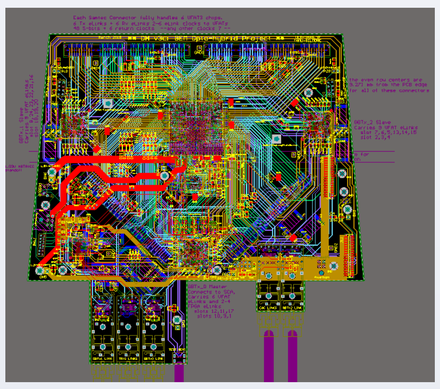
The GEB

The GEM Electronics Board (GEB) is a 8-layer PCB which plugs onto the detector and allows the 24 VFAT3s to communicate with a mezzanine, the Opto-Hybrid, which is equipped with an FPGA and GBT chipsets.

The Opto-Hybrid (OH)

An FPGA will be placed on the detector Opto-Hybrid (OH) to concentrate the trigger signals from the 24 VFAT3s, to perform zero-suppression and transmit the data to the CSC as well as to the μTCA off-detector electronics. About 216 differential pairs are required to connect the FPGA to the 24 VFAT3 chips. To avoid cables along the detector the signals are transmitted through 4 160-pins samtec® connectors installed on both GEB and OH. All components are powered through FEAST ASICs [3].





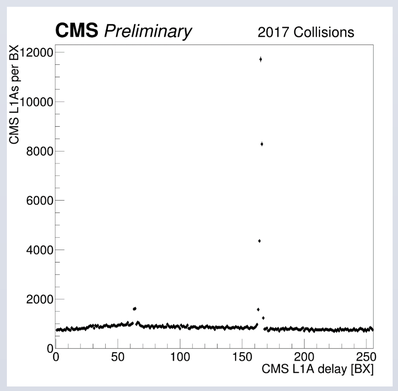
The μTCA back-end electronics

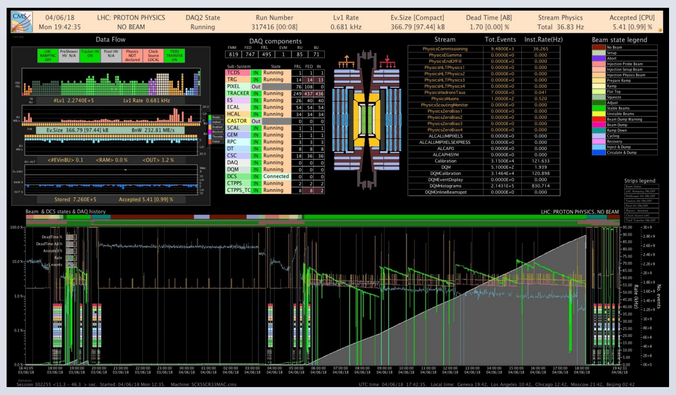
The μTCA standard will be used for the back-end electronics. The CTP7 AMC [4], designed for the CMS Calorimeter Trigger upgrade is used to receive the trigger and tracking data from the Triple-GEM detectors, provide local triggering and interface the CMS DAQ. Given the number of optical links available, 12 CTP7 and 1 μTCA crate are enough to read-out the entire GE1/1 system. The CMS AMC13 board [5] is used to interface the GEM readout system to the CMS DAQ.

- Virtex-7 690T FPGA + ZYNQ SoC FPGA with dual ARM Cortex-A9 CPU
- 80 RX and 61 TX GTH I/O links, multi-rate, LHC-synchronous or asynchronous link operation
- Embedded Linux Operating System running on the ZYNQ

GE1/1 planning and Slice Test

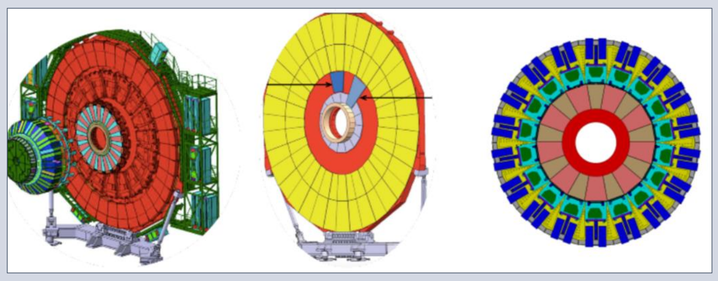
Before the installation of the final system during LHC Long Shutdown 2 (2019-2020), 10 detectors equipped with the VFAT2 chip [6] (predecessor of VFAT3) have been installed in CMS during the 2017 winter. This prototype step is called Slice Test. End of 2017, these detectors have been fully integrated in the DAQ and DCS (Detector Control System) of CMS. During winter 2018, two detectors have been replaced by detectors equipped with the final electronics version, including the VFAT3.





GE2/1 and ME0 upgrades

Beyond GE1/1, CMS plans to install additional layers of Triple-GEM detectors: GE2/1 and ME0. GE2/1 is on the second endcap disk of CMS while ME0 is an extra layer, closer to the beam pipe, that will be installed behind the new High Granularity Calorimeter.



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[1] Low-noise and low-power binary front-end in 130nm CMOS for triple-GEM detectors supporting wide range of detector capacitances with gain and peaking time programmability, P. Aspell et al., IEEE-NSS 2017 Proc. [2] Development of GEM Electronics Board (GEB), J. Talvitie et al., TWEPP2014, JINST 9 (2014) 12, C12030 [3] DC-DC converters in 0.35um CMOS technology, S.Michelis et al., JINST 7 (2012) C01072 [4] The Calorimeter Trigger Processor Card: the next generation of high speed algorithmic data processing at CMS, A. Svetek et al., JINST 11 (2016) C02011 [5] The AMC13XG: a new generation clock/timing/DAQ module for CMS MicroTCA, E. Hazen et al., TWEPP 2013, JINST (2013) 8 C12036. [6] VFAT2: A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors, P. Aspell et al., TWEPP 2007 Proc. ISBN 978-92-9083-304-8e