The uTCA Fast Control board for generic control and data acquisition applications for HEP experiments

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1. Motivation

The uTCA Fast Control board (uFC) is an FPGA-based μTCA compatible Advanced Mezzanine Card (AMC) for generic control and data acquisition applications in high energy physics (HEP) experiments. Built around the Xilinx Kintex-7 FPGA, the uFC provides users with a platform which has access to onboard FPGA Mezzanine Card (FMC) sockets with a large array of configurable I/O and high-speed links up to 10 Gbps. This poster presents test results from the first set of pre-production prototypes and reports on applications in High Energy Photon Source in China.

2. Implementation

Designed as a full size, double width AMC, the uFC is suitable for μTCA-based scalable systems, as well as for bench-top prototyping.
- Xilinx Kintex-7 XC7K325T-2FFG900I FPGA - capable of supporting link rate up to 10 Gbps
- Memory
  - Up to 8GB DDR3 SODIMM, capable of memory transfer rates of up to 64Gbps at 500MHz
  - 32MB Flash Memory
  - 2KiB iIC EEpROM with EUI-48™ Node Identity
- Communication & Networking
  - Card edge AMC connector - provides high-speed connectivity on up to 8 ports
  - Two SFP / SFP+ cage
  - UART To USB Bridge
- Expansion Connectors
  - Two FMC-HPC (Partial Population) connector, each has 4 GTX Transceivers, 116 single-ended or 58 differential user-defined signals (34 LA & 24 HA)
- ARM Cortex-M7 microcontroller - implements Module Management Controller (MMC) and clock controller via FreeRTOS lwIP
- Clocking - offers a large selection of input clock sources
- Control & I/O
  - 8X DIP Switches
  - AMS FAN Header (2 I/O)
  - LEMO input/output
- Power -12V wall adapter for bench-top prototyping
  - Voltage and Current measurement and management capability of 2.5V, 1.5V, and 1.2V, 1.0V supplies
- Configuration
  - JTAG header provided for use with Xilinx download cables such as the Platform Cable USB II or Digilent USB cable
  - 32MB (256Mb) Quad SPI Flash
  - AMC backboard JTAG

3. Preliminary Result

We adopted the uFC in the second generation hybrid pixel detector system (HEPS-BPIX) with single photon counting mode for the High Energy Photon Source (HEPS) in China. The prototype system was assembled with sixteen modules including 1M pixels in total, covering an area of 16.32 cm x 18.3 cm. The data acquisition is provided by a single server through four 10 Gigabit Ethernet (10 GbE), achieving a data rate of 1.15 GB/s at 8 bit, 1.2 kHz frame rate.

The uFC fan-outs clock and trigger to front-end modules and forward packets between front-end module and DAQ via 10G Ethernet.

The uFC to NAT-MCH- PHYS80 backplane communication test on Port 0 and Port 4-7 in the NATIVE-R9-WR μTCA Crate with a xTCA-based extender card (NAMC-EXT-RTM-FPS).