# The uTCA Fast Control board for generic control and data acquisition applications for HEP experiments


Jie Zhang, Hangxu Li, Jingzi Gu, Xiaoshan Jiang

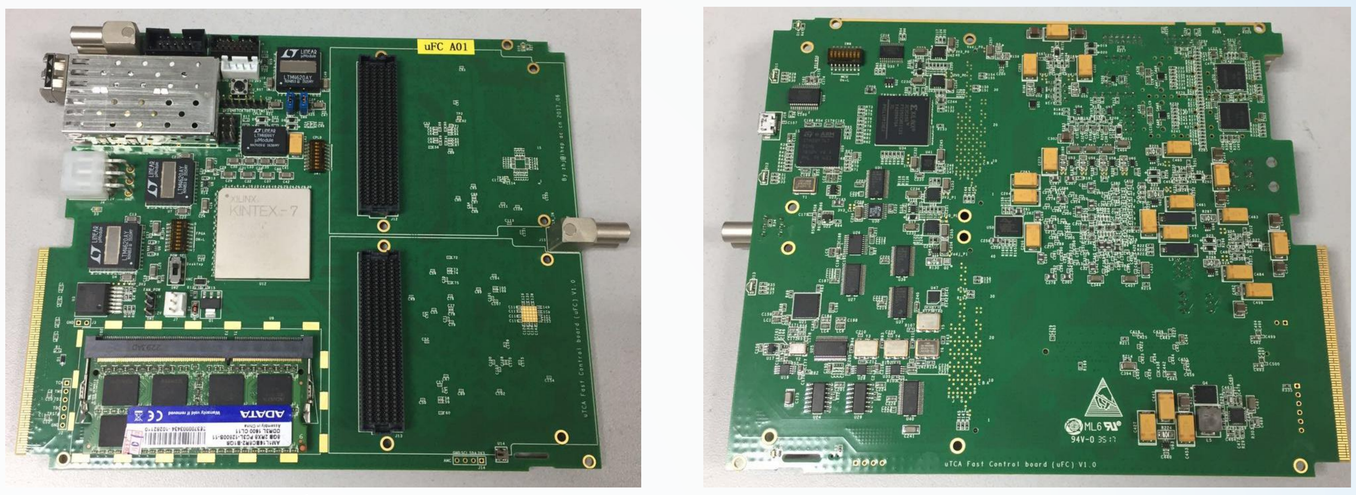
The State Key Laboratory of Particle Detection and Electronics,

Institute of High Energy Physics, CAS, China

E-mail: zhj@ihep.ac.cn


## 1·Motivation

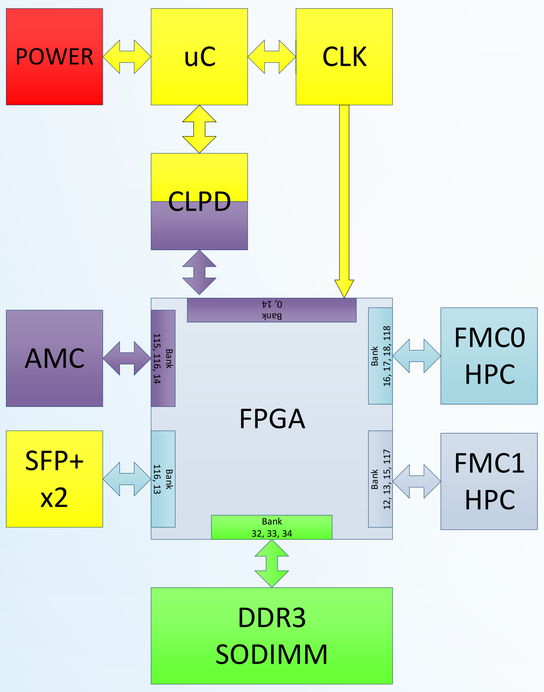
The uTCA Fast Control board (uFC) is an FPGA-based µTCA compatible Advanced Mezzanine Card (AMC) for generic control and data acquisition applications in high energy physics (HEP) experiments. Built around the Xilinx Kintex-7 FPGA, the uFC provides users with a platform which has access to on-board FPGA Mezzanine Card (FMC) sockets with a large array of configurable I/O and high-speed links up to 10 Gbps. This poster presents test results from the first set of pre-production prototypes and reports on applications in High Energy Photon Source in China.



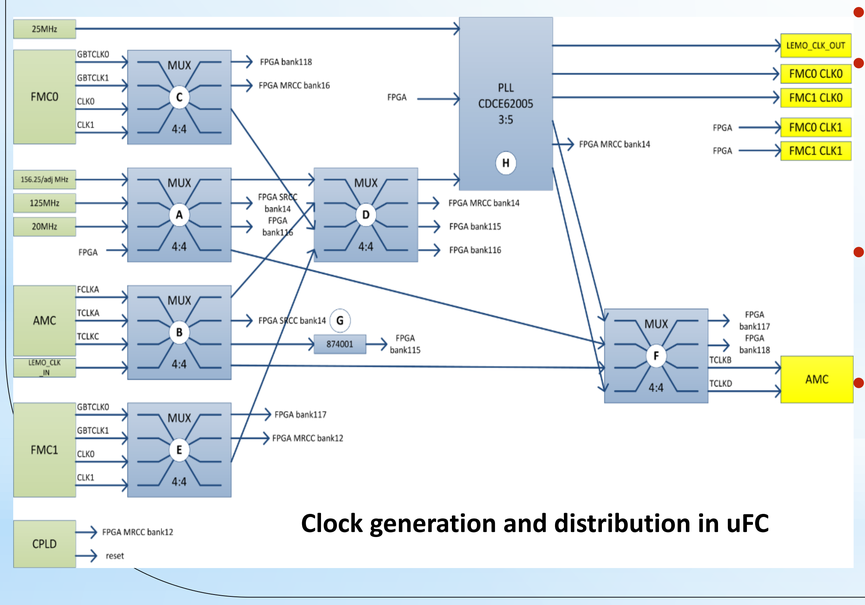
Top view Bottom view

**Photo of the pre-production uFC, highlighting the two high-pin count (HPC) FMC Mezzanine Card (FMC) sockets and 8GB DDR3 SODIMM module.**

## 2· IMPLEMENTATION



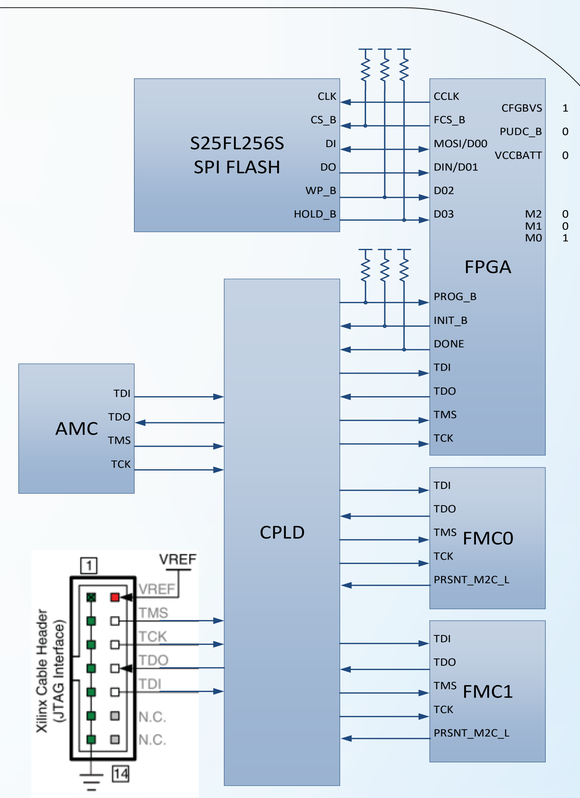

**Block diagram of uFC**




**Clock generation and distribution in uFC**

Designed as a full size, double width AMC, the uFC is suitable for µTCA-based scalable system, as well as for bench-top prototyping.

- Xilinx **Kintex-7** XC7K325T-2FFG900I FPGA - capable of supporting link rate up to 10 Gbps
- **Memory**
  - Up to 8GB DDR3 SODIMM, capable of memory transfer rates of up to 64Gbps at 500MHz
  - 32MB Flash Memory
  - 2Kbit IIC EEPROM with EUI-48™ Node Identity
- **Communication & Networking**
  - Card edge AMC connector - provides high-speed connectivity on up to 8 ports
  - Two SFP / SFP+ cage
  - UART To USB Bridge
- **Expansion Connectors**
  - Two FMC-HPC (Partial Population) connector, each has 4 GTX Transceivers, 116 single-ended or 58 differential user defined signals (34 LA & 24 HA)
  - Vadj can support 1.8V, 2.5V, or 3.3V
- **ARM Cortex-M7 microcontroller** - implements Module Management Controller (MMC) and clock controller via FreeRTOS lwIP
- **Clocking** - offers a large selection of input clock sources
- **Control & I/O**
  - 8X DIP Switches
  - AMS FAN Header (2 I/O)
  - LEMO input/output
- **Power** -12V wall adapter for bench-top prototyping
  - Voltage and Current measurement and management capability of 2.5V, 1.5V, and 1.2V, 1.0V supplies
- **Configuration**
  - JTAG header provided for use with Xilinx download cables such as the Platform Cable USB II or Digilent USB cable
  - 32MB (256Mb) Quad SPI Flash
  - AMC backboard JTAG



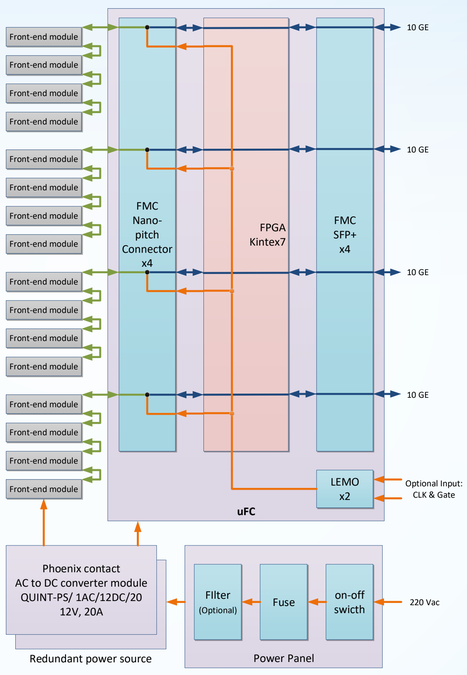

Xilinx allows configuring and debugging the FPGA through JTAG. The CPLD in the uFC acts as a bridge between FPGA, FMC0/1, AMC backboard and JTAG connector. Users can access to the FPGA through the uTCA crate or JTAG connector.

When an FMC card is attached to the uFC board, it is automatically added to the JTAG chain through CPLD. CPLD adds an attached FMC mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection via a device or bypass jumper for the JTAG chain to be completed to the FPGA.

## 3· PRELIMINARY RESULT

uFC to NAT-MCH-PHYS80 backplane communication test on Port 0 and Port 4-7 in the NATIVE-R9-WR µTCA Crate with a xTCA-based extender card (NAMC-EXT-RTM-F-PS).

We adopted the uFC in the second generation hybrid pixel detector system (HEPS-BPIX) with single photon counting mode for the High Energy Photon Source (HEPS) in China. The prototype system was assembled with sixteen modules including 1M pixels in total, covering an area of 16.32 cm x 18.3 cm. The data acquisition is provided by a single server through four 10 Gigabit Ethernet (10 GbE), achieving a data rate of 1.15 GB/s at 8 bit, 1.2 kHz frame rate.




The uFC fan-outs clock and trigger to front-end modules and forward packets between front-end module and DAQ via 10G Ethernet.

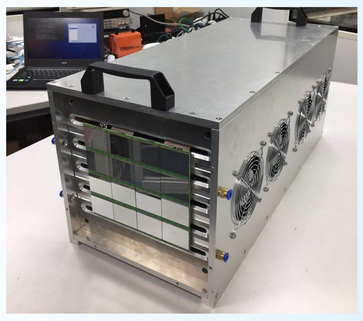
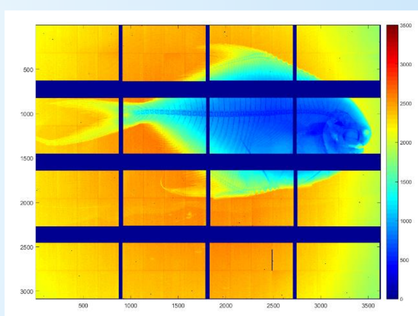


**Photo of the second generation HEPS-BPIX detector.**



**X-Ray images**