Lifetime Study of COTS ADC for SBND LAr TPC Readout Electronics
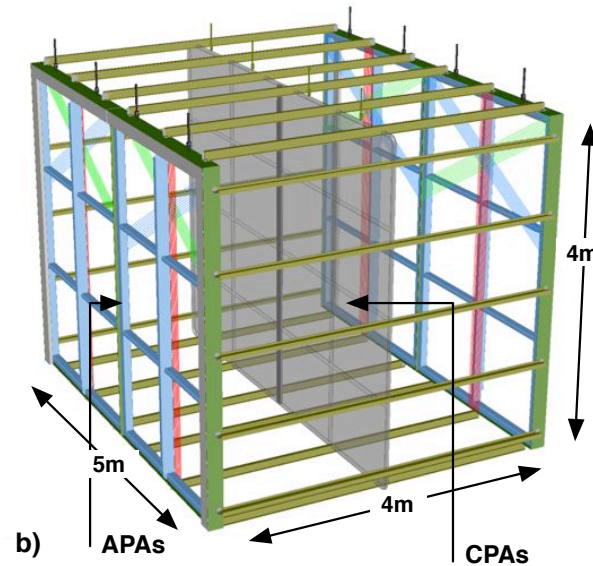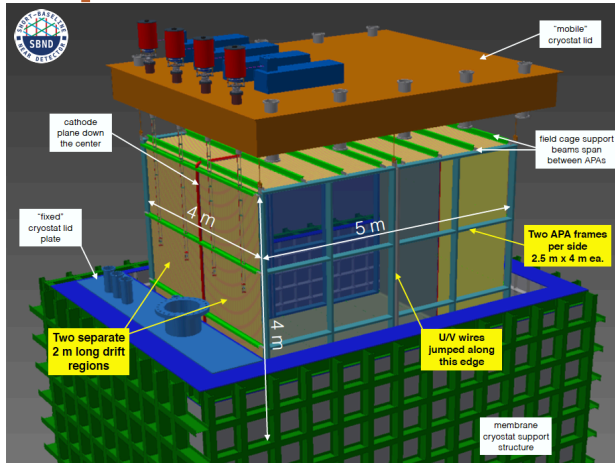
Shanshan Gao on behalf of the SBND Cold Electronics Team

Brookhaven National Laboratory

6/15/2018

SBND Experiment

- SBN (Short Baseline Neutrino) program
  - Using Booster Neutrino Beam for sterile neutrino search
  - 3 detectors: MicroBooNE, ICARUS, and SBND
  - SBND is expected to be in operation in 2020

- SBND is a 260 ton LAr TPC as near detector in SBN
  - Central cathode plane assembly (CPA), 2 anode plane assemblies (APA) on either side w/ 2m drift distance each
  - 11,264 sensing wires to be read out
  - **Cold electronics makes possible an optimum balance** among various design and performance requirements for such large sized detectors

Motivation of Cold Electronics in Large LAr TPC

- **Much lower** noise

  – Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics

  – The noise is significantly less than at room temperature when CMOS FE ASICs are operating at cryogenic temperatures

    - Benefit from the charge carrier mobility in silicon increasing and thermal fluctuations decreasing with kT/e

- **Much less** cryostat penetrations

  – Signal digitization and multiplexing to high speed links inside the cryostat results in large reduction in the quantity of cables (less outgassing) and the number of feed-through penetrations, also giving the designers of both the TPC and the cryostat the freedom to choose the optimum configurations

- BNL has started cold electronics study since 2008

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SBND Cold ADC Option

- A cold ADC committee formed by SBND collaboration is to advise the development of cold readout electronics

  - Explore different options, including commercial ADC in cold, dual gain configuration with ASIC ADC, new ADC ASIC etc.

  - The COTS ADC work *benefits the future program*, which serves as a potential backup for DUNE far detector, cold qualification techniques are useful for future Dark Matter and Neutrino experiments

- BNL is leading the **COTS ADC** lifetime study in cold operation

  - COTS ADC candidates with 100% cold yield identified

    - ADI AD7274, TSMC 350nm CMOS

    - TI ADS7883, TI 180nm CMOS

    - TI ADS7049-Q1, TI 500nm CMOS

  - SBND collaborators from **Manchester University** join the lifetime study to collect data in parallel

  - **A qualified COTS ADC will minimize the engineering effort**

Evaluation Test for COTS ADC at Cold

- Cold characterization test
  - AD7274 and ADS7049-Q1
    - DNL/INL performance at LN2 is comparable with at RT
  - AD7883, missing codes are located

- **Accelerated lifetime test (ALT)**
  - Due to HCE aging, lifetime of COTS ADC at cryogenic temperature is a crucial concern along with performance
  - The COTS ADC lifetime study procedure is developed
    - Exploratory phase and validation phase
  - Preliminary projection of lifetime

- Cold electronics integration test
  - A necessary step to validate COTS ADC performance at cold
 - 40% APA integration test and the incoming SBND VST

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CMOS Lifetime at Cryogenic Temperatures

- Most of the major failure mechanisms are strongly temperature dependent and become negligible at cryogenic temperature
  - Such as electro-migration, stress migration, time-dependent dielectric breakdown and negative-bias temperature instability

- The degradation (aging) due to channel Hot Carrier Effects (HCE)
  - **The only remaining mechanism** that may affect the lifetime of CMOS devices at cryogenic temperature
  - Lifetime due to HCE aging
    - A limit defined by a chosen level of monotonic degradation
      - Drain current, transconductance, threshold voltage etc.
    - The aging mechanism does **not** result in **sudden device failure**
    - The device "fails" if a chosen parameter gets out of the specified circuit design range

- Reliability and aging are entirely different concepts

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Basic on HCE and ALT

Accelerated Lifetime Test

Hot Carrier Effect
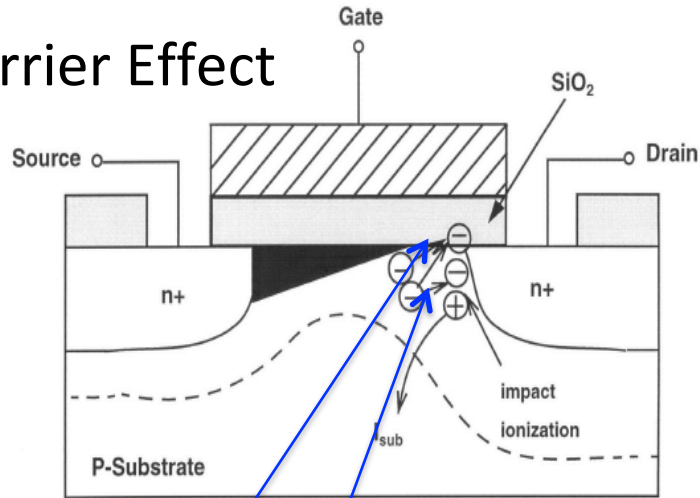
→Some hot electronics exceed the energy required to create an electron-hole pair, resulting in *impact ionization*

→ A very small fraction of hot electrons exceeds the energy required to create an *interface state* at the Si-SiO2 interface

→ Due to the generation of interface states, negative charges will accumulate causing the degradation

→ More severe at cold than at RT

CMOS in DC operation

→ ALT at any temperature (well-established by foundries) transistor is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation to a practically observable range.

→ ALT is widely used by industry
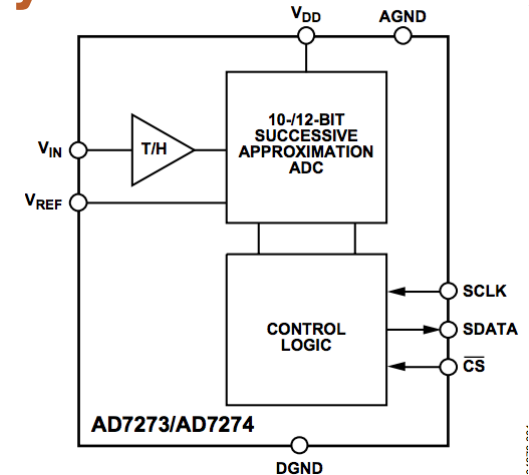
→ Lifetime is projected by empirical equation

$$log_{10}\tau \propto 1/V_{ds}$$

CMOS in AC operation

→ Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $4/(f_{clock}*t_{rise})$ compared to dc operation. This factor is large (>100) for deep submicron technology and clock frequency needed for TPC

AD7274 is the Main Focus of Lifetime Study

FUNCTIONAL BLOCK DIAGRAM

- ADI AD7274 commercial 12-bit SAR ADC
  - 350nm TSMC CMOS
  - V_{DD} of 2.35V to 3.6V
    - Absolute maximum of V_{DD} and V_{REF}: 6.0V
  - ~5mW at 2MSPS with 2.5V supplies
  - ENOB: ~11.2 bit (at RT)
  - No internal regulator
    - A stress test can be devised based on the technology node (V_{DS} = 3.6V)

- Tentative conclusions pre the stress test
  - Extensive evaluation of TSMC 180 nm node projects a lifetime in excess of 10^3 years at 77 K and nominal V_{DS} = 1.8V, under DC operation
  - Expected better lifetime for TSMC 350nm
    - Based on the lower peak electric field in the channel (and lower HCE)
    - In the "core" of the ADC, each transistor will be conducting current during a short fraction of the switching cycle, with an effective duty cycle of less than 1/100, providing some margin to the lifetime estimates
  - No details of the ADC circuits beyond the block diagram

Exploratory Phase (1)

- Preparation phase
  - Goal is to make test stand suitable for lifetime study
  - Parameters to be evaluated
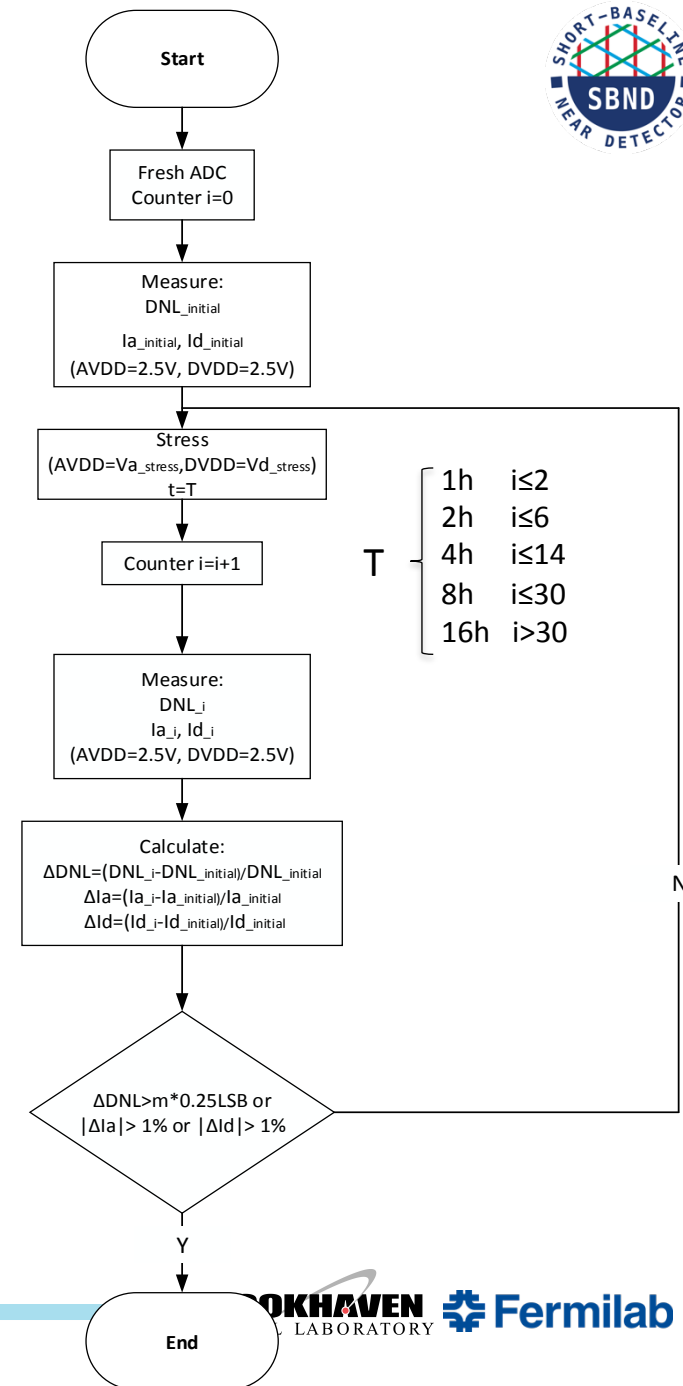   - Power consumption
    - Linearity: DNL/INL

DNL @ RT: ± 0.5 LSB
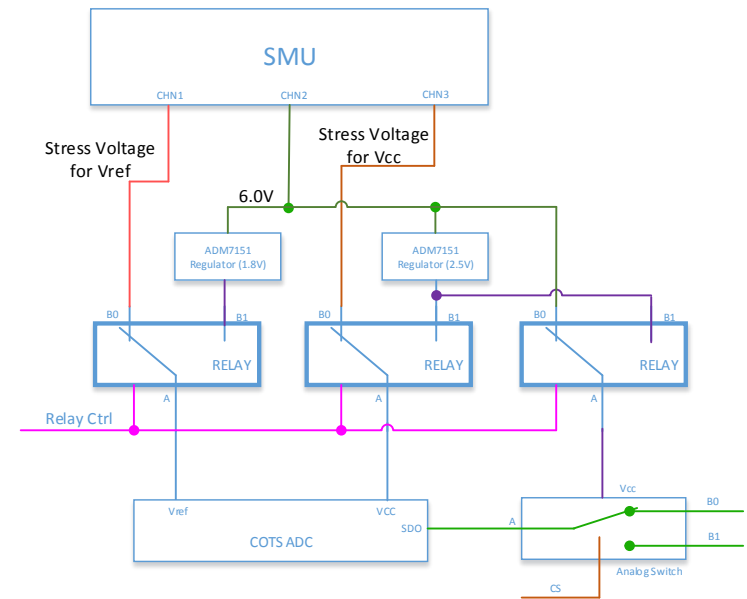
DNL @ LN2: ± 0.5 LSB
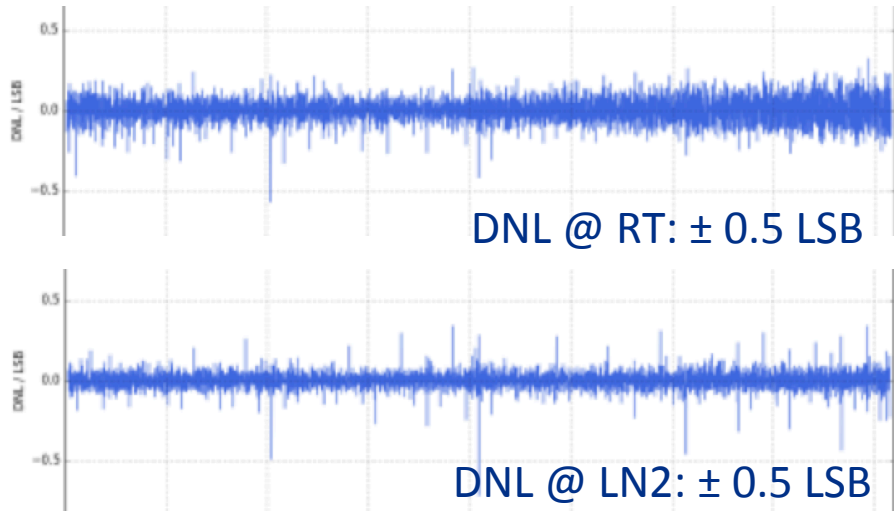
Test stand for cold screening test
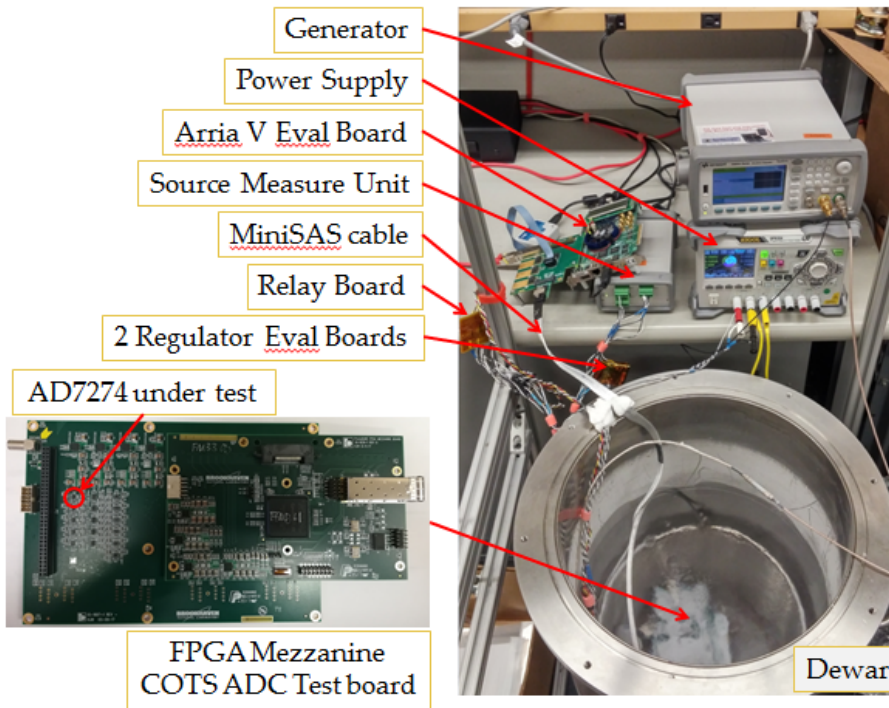
- Goal of exploratory phase is to define criteria of lifetime from the stress test
  - We will gain or lose confidence based on the test results in this phase
  - The ADC does not "fail"; the "lifetime" is a limit to specified performance

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Exploratory Phase (2)

- Operation limit of COTS ADC was identified
  - The limit could be the ones which cause the ADC malfunctioning

- Only **fresh device samples** will be stressed within the operation limit
  - **Continuous** current monitoring
  - **Periodical** performance characterization
    - DNL / INL

- Stress test results will be used to extrapolate the lifetime of the COTS ADC
  - The development of lifetime criteria will be an iterative process, tailored to ADC technology, based on the test data to be collected and analyzed

Start

Fresh ADC
Counter i=0

Measure:
$DNL_{initial}$
$Ia_{initial}$, $Id_{initial}$
(AVDD=2.5V, DVDD=2.5V)

Stress
(AVDD=Va_{stress}, DVDD=Vd_{stress})
t=T

Counter i=i+1

T		
1h	i≤2
2h	i≤6
4h	i≤14
8h	i≤30
16h	i>30

Measure:
DNL_i
Ia_i, Id_i
(AVDD=2.5V, DVDD=2.5V)

Calculate:
$\Delta DNL=(DNL_i-DNL_{initial})/DNL_{initial}$
$\Delta Ia=(Ia_i-Ia_{initial})/Ia_{initial}$
$\Delta Id=(Id_i-Id_{initial})/Id_{initial}$

$\Delta DNL>m*0.25LSB$ or
$|\Delta Ia|> 1\%$ or $|\Delta Id|> 1\%$

N

Y

End

ADC Stress Test Setup for the Exploratory Phase

Generator
Power Supply
Arria V Eval Board
Source Measure Unit
MiniSAS cable
Relay Board
2 Regulator Eval Boards
AD7274 under test
FPGA Mezzanine COTS ADC Test board
Dewar

- Challenges of the stress test at cold
  - Cryogenic (77K)
    - Cold qualified components
  - Long term
    - Non-stop running at cold up to a month
  - Sensitivity
    - Current monitoring with µA level
    - Sigma of DNL with 0.01 LSB level
   - Signal integrity

- ADC power scheme
  - Stress test
    - Precision current measurement
    - Powered by SMU directly
  - Performance characterization test
    - Lower noise gets right DNL/INL
    - Power from low noise regulator
  - Automatic switching for long term run

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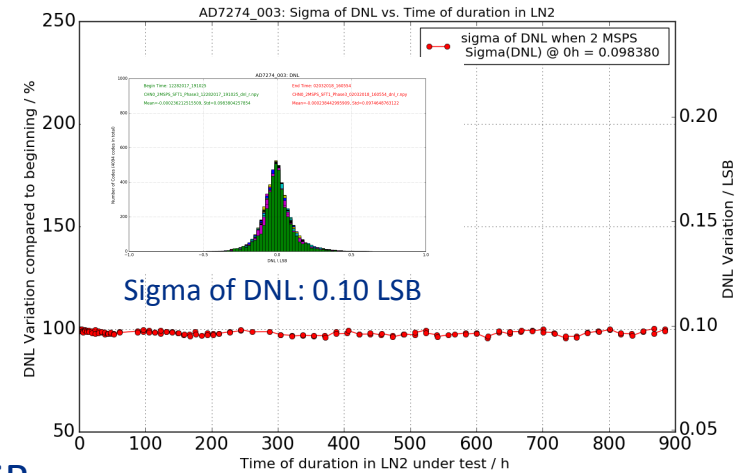# ADC with Nominal Operation Voltage

- An sample has run for 870 hours with nominal operation voltage
  - To verify if there is any significant change of current and DNL performance compared to the samples running with stress voltage as a crosscheck
  - V_{DD} = 2.5V, V_{REF} = 1.8V
    - Current or performance change is not significant
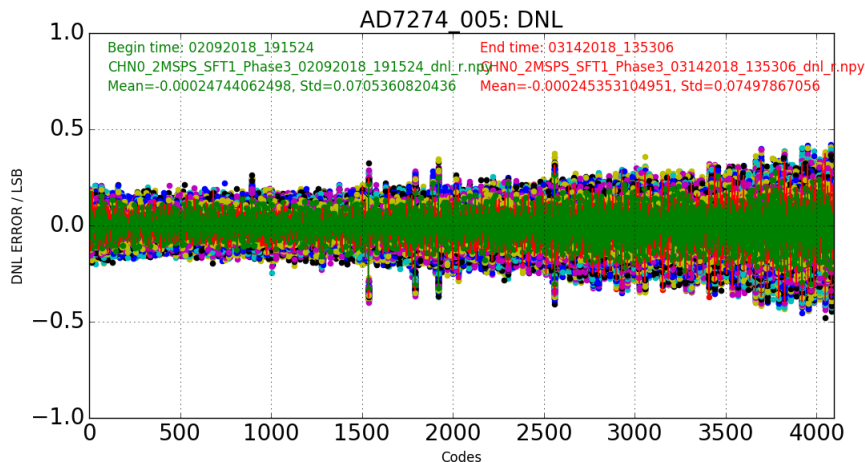   - Variation of < 1% requires sources with the resolution of µA
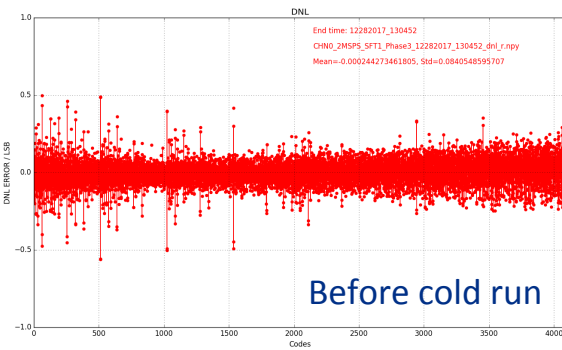
DNL @ RT: ± 0.5 LSB
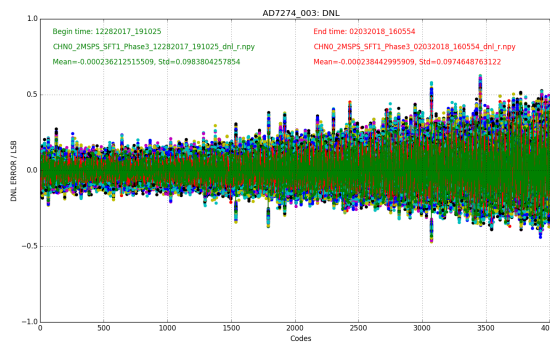
DNL overlap @ LN2: ± 0.5 LSB
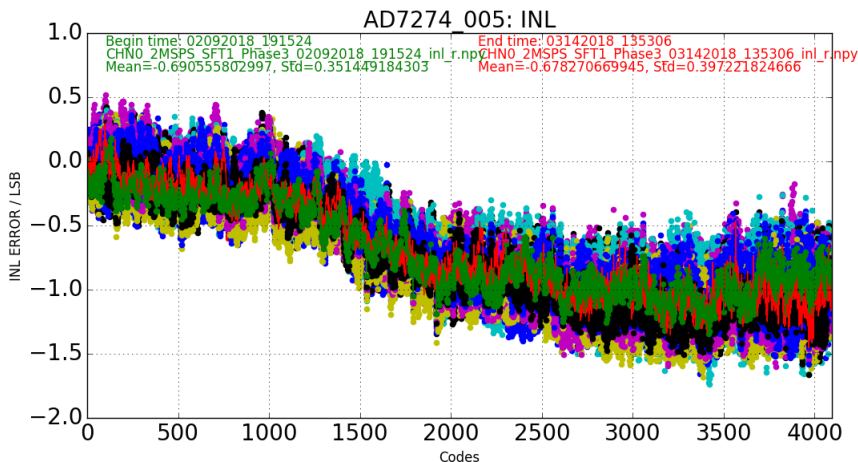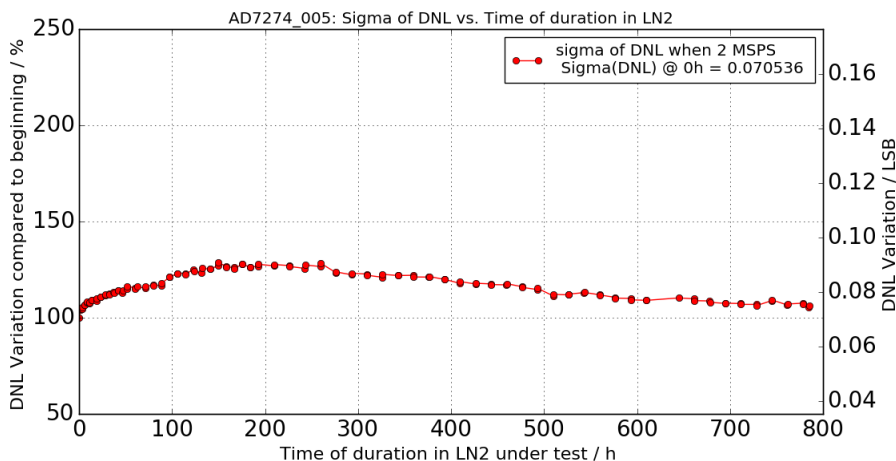
Sigma of DNL: 0.10 LSB

Sigma of DNL along the stress time

A Sample ADC Stressed at 5.25V at LN2 for 718 Hours

AD7274_005: DNL

Begin time: 02092018_191524
CHN0_2MSPS_SFT1_Phase3_02092018_191524_dnl_r.npy
Mean=-0.00024744062498, Std=0.0705360820436

End time: 03142018_135306
CHN0_2MSPS_SFT1_Phase3_03142018_135306_dnl_r.npy
Mean=-0.000245353104951, Std=0.07497867056

DNL ERROR / LSB vs Codes

DNL overlap @ LN2: ± 0.5 LSB

AD7274_005: INL

Begin time: 02092018_191524
CHN0_2MSPS_SFT1_Phase3_02092018_191524_inl_r.npy
Mean=-0.690555802997, Std=0.351449184303

End time: 03142018_135306
CHN0_2MSPS_SFT1_Phase3_03142018_135306_inl_r.npy
Mean=-0.678270669945, Std=0.397221824666

INL ERROR / LSB vs Codes

INL overlap @ LN2: 2 LSB

AD7274_005: Sigma of DNL vs. Time of duration in LN2

sigma of DNL when 2 MSPS
Sigma(DNL) @ 0h = 0.070536

DNL Variation compared to beginning / % and DNL Variation / LSB vs Time of duration in LN2 under test / h

Sigma of DNL smaller than 0.10 LSB

AD7274_005: Current vs. Time of duration in LN2

Stress Voltage
V(0) = 5.248V, I(0) = 4.917mA
718.3 Hours under Stress

Current Variation compared to beginning / % vs Time of duration in LN2 under test / h
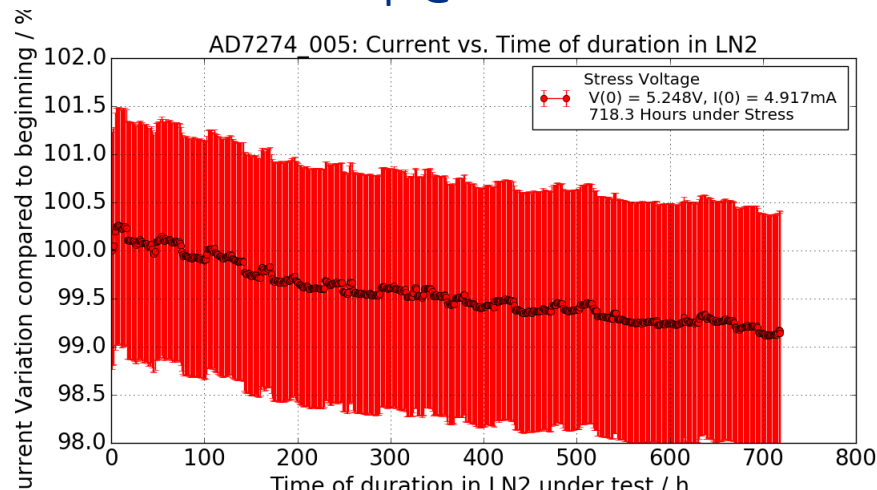
I_{VCC} decreases ~1%

Note: INL also includes the non-linearity of input triangle waveform

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The Criteria for Lifetime Study

- Li, S., Ma, J., De Geronimo, G., Chen, H., & Radeka, V. (2013). LAr TPC electronics CMOS lifetime at 300 K and 77 K and reliability under thermal cycling. IEEE Transactions on Nuclear Science, 60(6), 4737-4743.

  – The lifetime due to HCE at both the cryogenic temperature, as well as at room temperature, is limited by a predictable and a very gradual and monotonic degradation (aging) mechanism

  – Lifetime can be defined by any arbitrary but consistent criterion
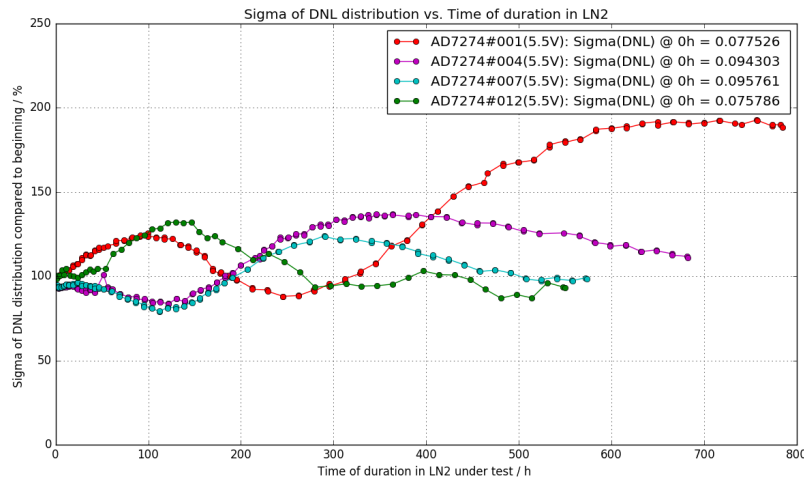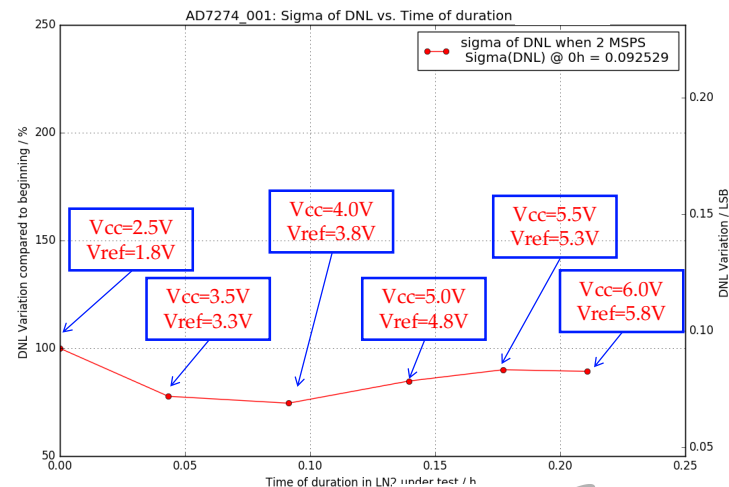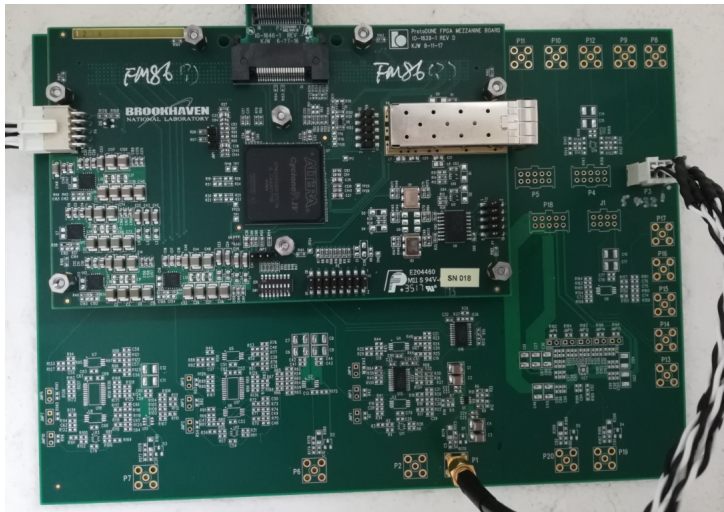

Sigma of DNL is less than 0.2 LSB
Non-monotonic change
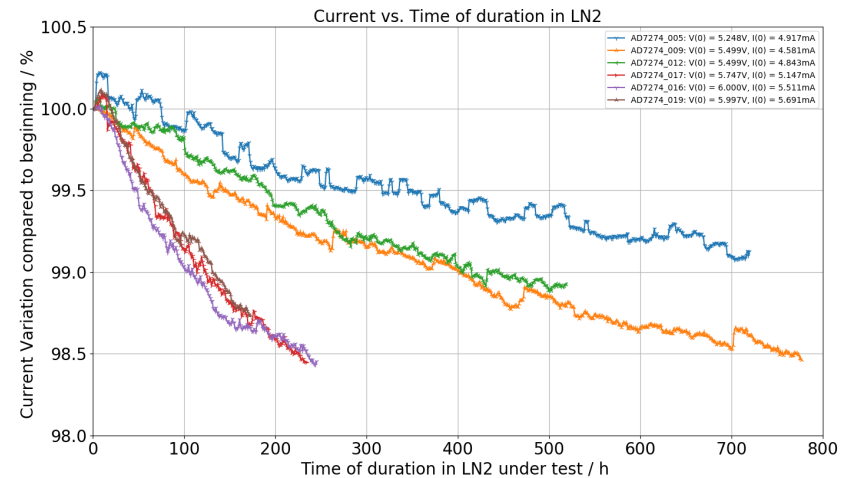
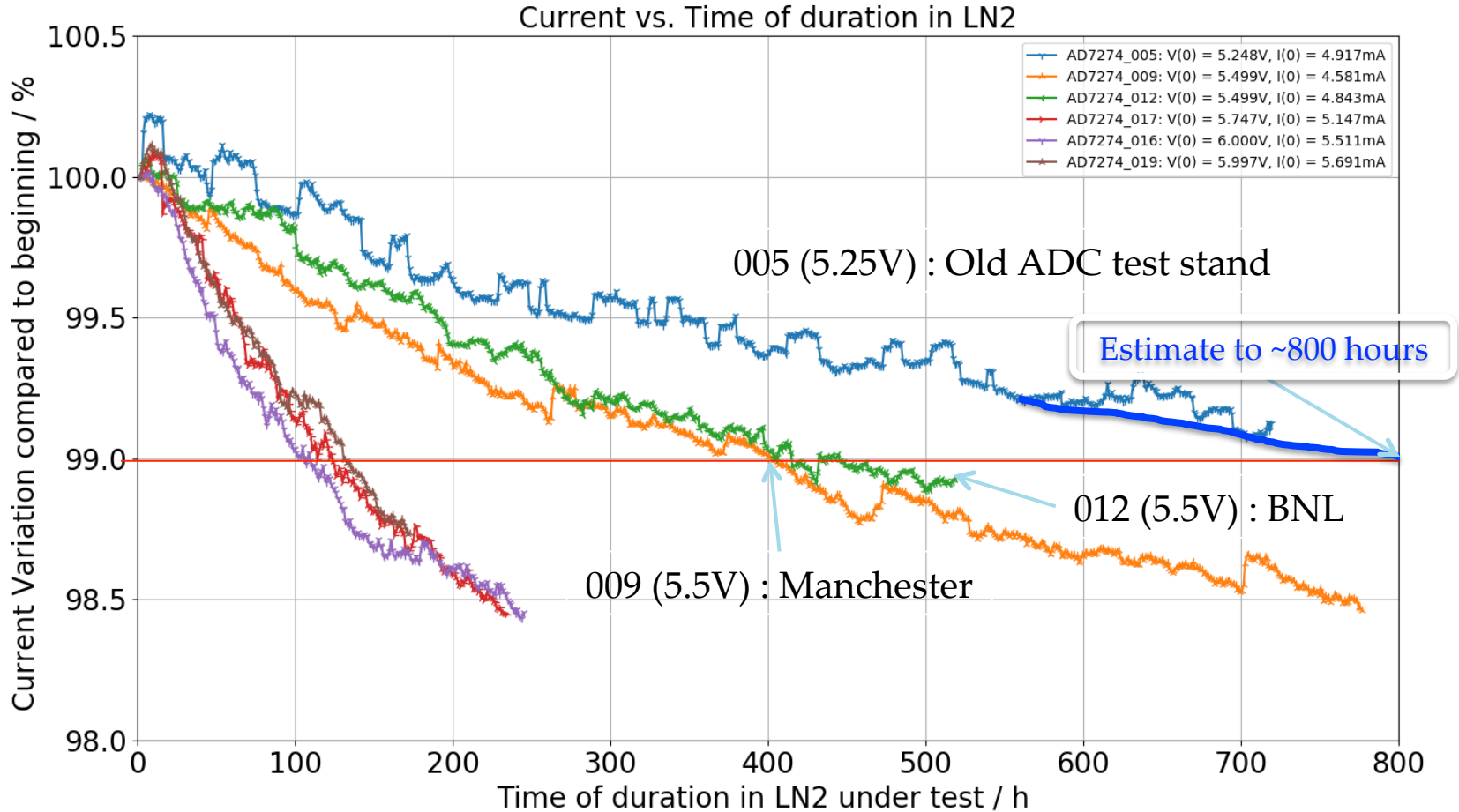Variation of I_{VCC} will be used to assess the lifetime of COTS ADC

Validation Phase

- Goal is to collect more data to validate what we had learned in the exploratory phase
  - Still ongoing

- Upgrade of the stress test stand
  - Support stress voltages up to 6V
    - The former one up to 5.5V
  - DNL/INL can be monitored as well as current with stress voltages
    - The former one can't monitor DNL/INL during the stress
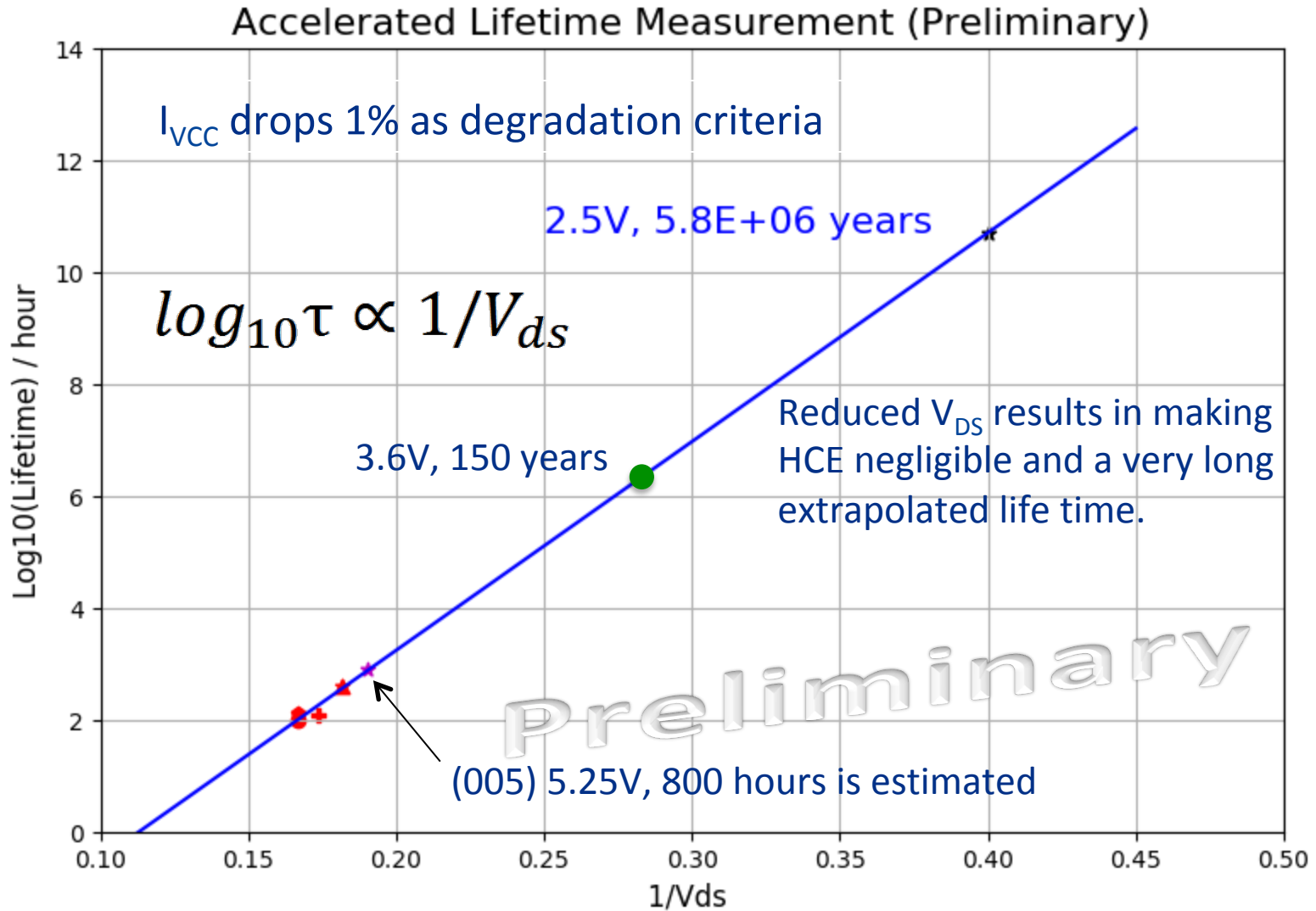 - Share with SBND collaborators from Manchester

AD7274_001: Sigma of DNL vs. Time of duration

sigma of DNL when 2 MSPS
Sigma(DNL) @ 0h = 0.092529

Vcc=2.5V Vref=1.8V
Vcc=3.5V Vref=3.3V
Vcc=4.0V Vref=3.8V
Vcc=5.0V Vref=4.8V
Vcc=5.5V Vref=5.3V
Vcc=6.0V Vref=5.8V

ADC Lifetime Study During Validation Phase

- Stress test result of 6 ADC chips
 - #009 (*Manchester*) and #012 (*BNL*) overlap quite well

Current vs. Time of duration in LN2

Legend:
- AD7274_005: V(0) = 5.248V, I(0) = 4.917mA
- AD7274_009: V(0) = 5.499V, I(0) = 4.581mA
- AD7274_012: V(0) = 5.499V, I(0) = 4.843mA
- AD7274_017: V(0) = 5.747V, I(0) = 5.147mA
- AD7274_016: V(0) = 6.000V, I(0) = 5.511mA
- AD7274_019: V(0) = 5.997V, I(0) = 5.691mA

005 (5.25V) : Old ADC test stand

Estimate to ~800 hours

012 (5.5V) : BNL

009 (5.5V) : Manchester

Y-axis: Current Variation compared to beginning / %
X-axis: Time of duration in LN2 under test / h

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ADC Lifetime Projection

Accelerated Lifetime Measurement (Preliminary)

I_{VCC} drops 1% as degradation criteria

2.5V, 5.8E+06 years

$log_{10}\tau \propto 1/V_{ds}$

3.6V, 150 years

Reduced V_{DS} results in making HCE negligible and a very long extrapolated life time.

(005) 5.25V, 800 hours is estimated

Preliminary

A Little More Explanation of CMOS HCE Lifetime (Aging)

- Reliability and aging are entirely different
  - The Reliability is dependent on the system design, choice of components, assembly techniques, and in general, by the QA/QC in the work place.
    - M. White and J.B. Bernstein, "*Microelectronics Reliability: Physics-of - Failure Based Modeling and Lifetime Evaluation*", JPL Publication 08-5 2/08

- HCE aging is given by the physical/chemical processes
  - It can be controlled only by the design and the operating conditions
  - It does not result in sudden failure
    - The device "fails" if a chosen parameter gets out of the specified circuit design range
  - It is uniform and reproducible

- **The cold electronics for LAr TPCs** should be designed for a lifetime one or more orders of magnitude longer than the required service life (e.g., > 300 years for DUNE), essentially to **remain outside of the region of HCE degradation**

Cold Electronics Performance with COTS ADC

- Front End Mother Board Assembly (FEMB)
  - 128 channels of digitized TPC wire readout,
    - 88 assemblies for 11,264 SBND TPC channels
  - Analog mother board 8x 16-chn FE ASIC and 128x AD7274 chips
 - FPGA mezzanine: multiplexing of digitized signals to 4x 1Gbps links
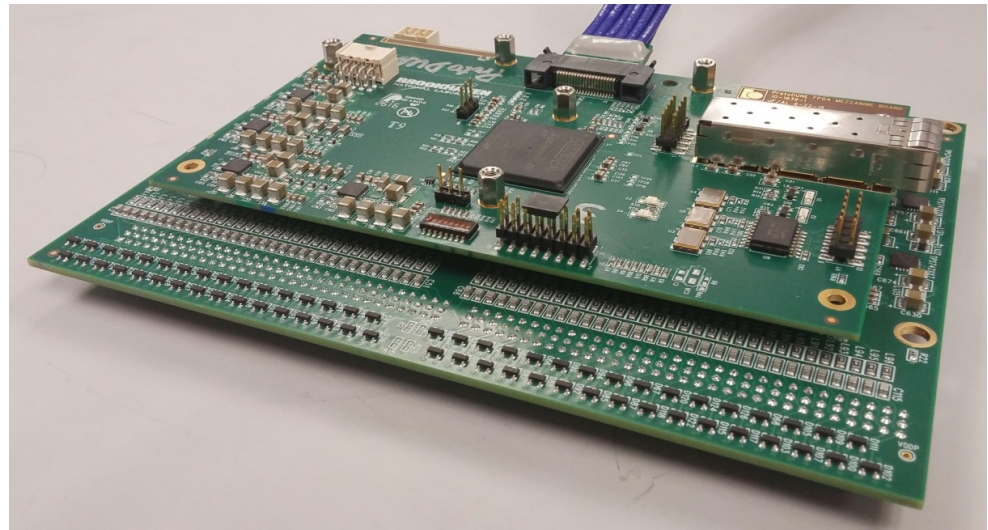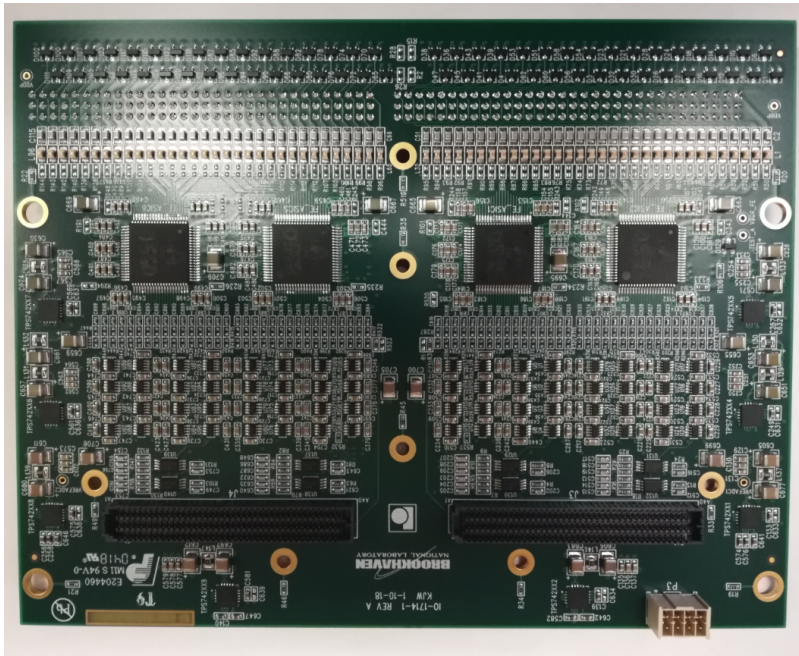
Integration Test at BNL

- A necessary (but not sufficient!) condition to achieve a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostic** and strict isolation and **grounding rules** will have to be followed

2.8m x 1.0m, 1024 sensing wires
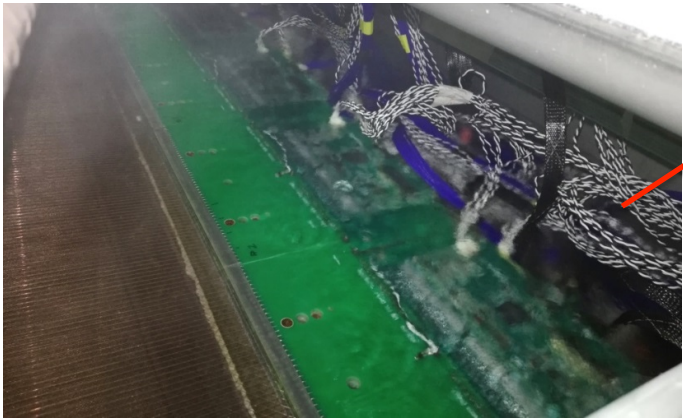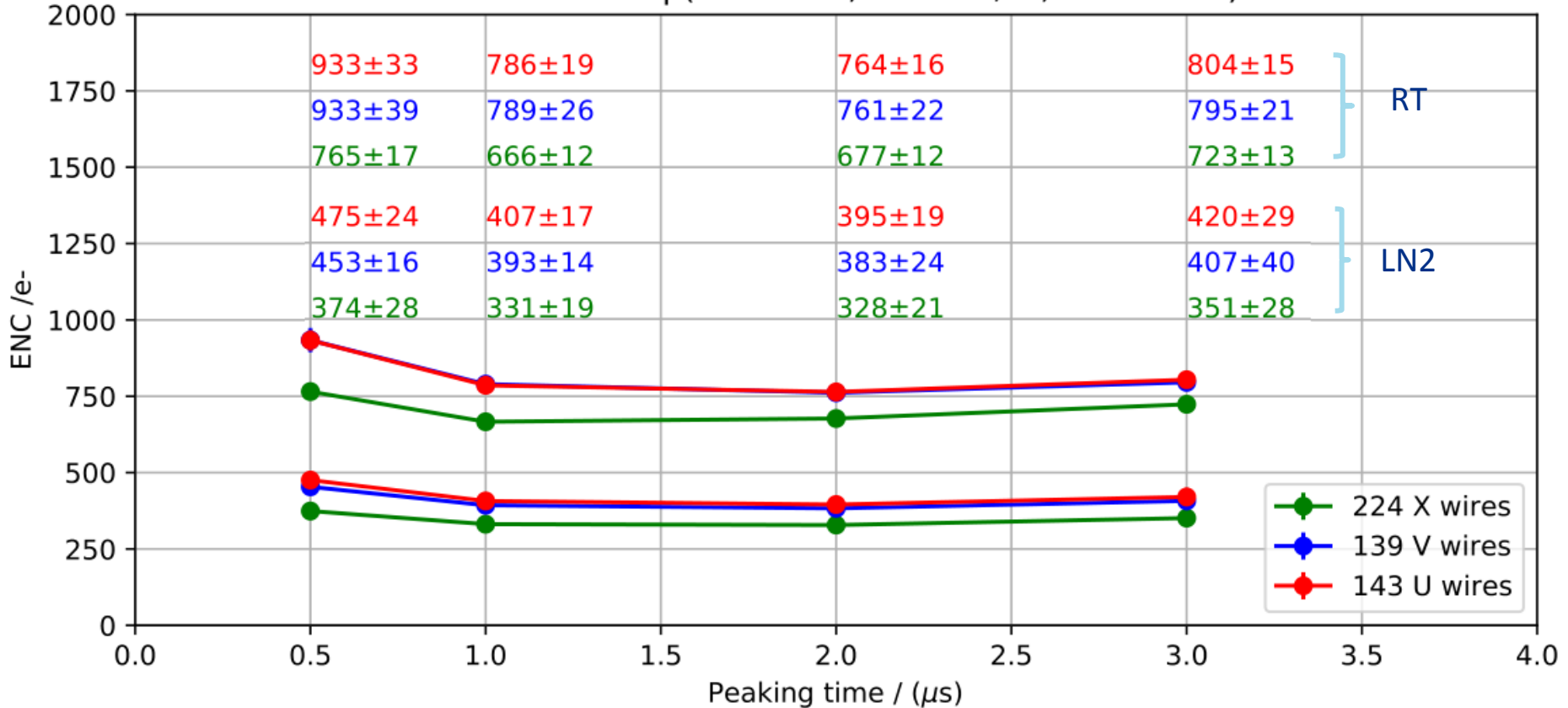
40% APA and 4 FEMBs fully submerged in LN2

Feed-through + WIEC

Cold box with 40% APA
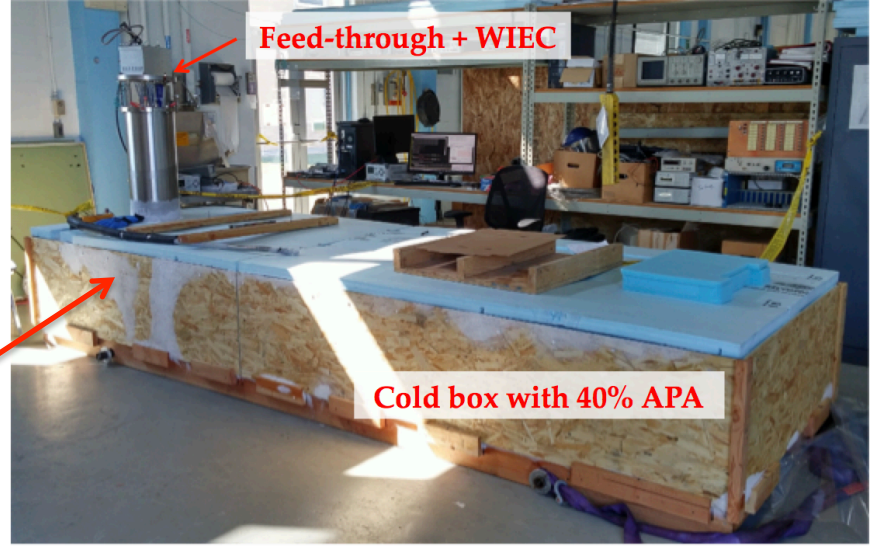
~400 Gallons (~1500L) LN2 was consumed

ENC Measurement of FEMB with 40% APA

40% APA with 4 FEMBs fully submerged in LN2

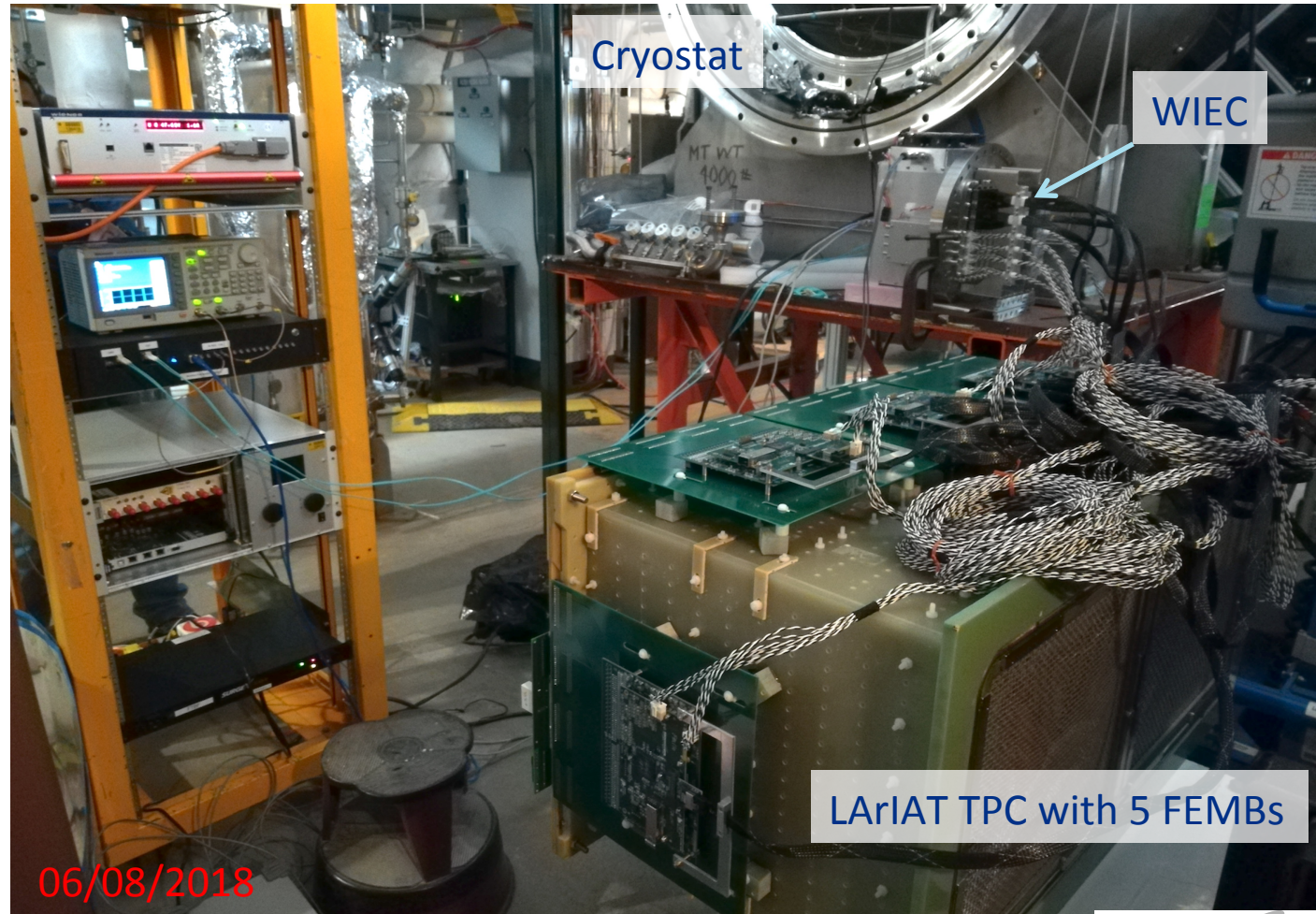APA ENC vs. Tp(Raw data, 25.0mV/fC, FPGA DAC)

Induction Planes (U/V = 4.0m) : ENC ~ 400 e^- @ t_p = 1us
Collection Plane (Y = 2.8m) : ENC ~ 330 e^- @ t_p = 1us

SBND Vertical Slice Test with LArIAT TPC

- 480 TPC wires, 5 FEMBs with AD7274 in use
- Aim for beam test at FTBF in coming weeks

Summary

- Readout electronics developed for low temperatures (77K-89K) is an enabling technology for noble liquid detectors for neutrino experiments

- SBND collaboration has been studying the COTS ADC option
  - Preliminary lifetime projection of AD7274 is ~5.8 x 10^6 years at 2.5V operation
    - The HCE (hot carrier effect) will be negligible for COTS ADC used in SBND (and DUNE), and *we'll be stay out of HCE during the detector operation*
    - Validation phase of AD7274 lifetime study is ongoing

- **SBND collaboration has made decision to use COTS ADC**
  - Integration test with 40% APA has been performed at BNL, with demonstration of satisfactory ENC performance
  - SBND Vertical Slice Test at Fermilab is being prepared, aim to take data in coming weeks
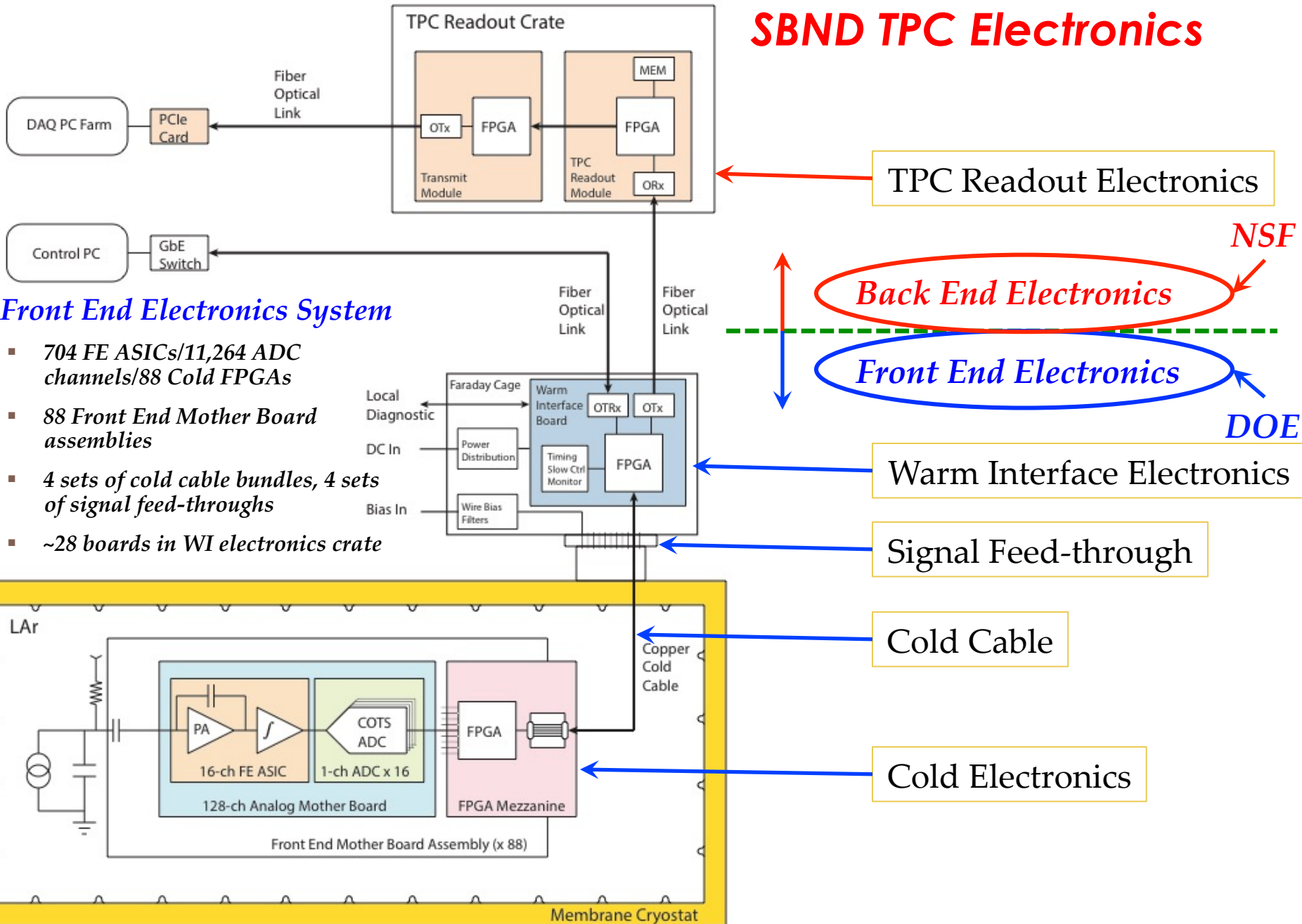
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Job Opening at BNL for Trigger & DAQ

- This job post is for multiple openings
- The successful candidate is expected to play an essential role in **FELIX** and **Global Trigger** development in the ATLAS upgrades and other *high-energy physics*, *nuclear physics* and *astronomy* experiments.
  - *Design, develop, prototype, and produce hardware and firmware for the ATLAS experiment*
  - *Evaluate hardware and firmware and characterize system performance*
  - *Participate in system integration of multiple combined systems*

- https://jobs.bnl.gov/job/upton/postdoctoral-research-associate/3437/8059129

Backup Slides

SBND TPC Electronics

TPC Readout Crate

Fiber Optical Link

DAQ PC Farm — PCIe Card

OTx — FPGA — Transmit Module

MEM — FPGA — TPC Readout Module — ORx

TPC Readout Electronics

Control PC — GbE Switch

Front End Electronics System

- 704 FE ASICs/11,264 ADC channels/88 Cold FPGAs
- 88 Front End Mother Board assemblies
- 4 sets of cold cable bundles, 4 sets of signal feed-throughs
- ~28 boards in WI electronics crate

NSF

Back End Electronics

Front End Electronics

DOE

Faraday Cage — Warm Interface Board — OTRx — OTx

Local Diagnostic

DC In — Power Distribution

Timing Slow Ctrl Monitor — FPGA

Bias In — Wire Bias Filters

Fiber Optical Link

Warm Interface Electronics

Signal Feed-through

Cold Cable

Cold Electronics

LAr

PA — ∫ — COTS ADC — FPGA

16-ch FE ASIC — 1-ch ADC x 16

128-ch Analog Mother Board — FPGA Mezzanine

Front End Mother Board Assembly (x 88)

Copper Cold Cable

Membrane Cryostat

Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length for CMOS at 300K and 89K

Signal for 3x3 and 5x5 mm Sense Wire Spacing

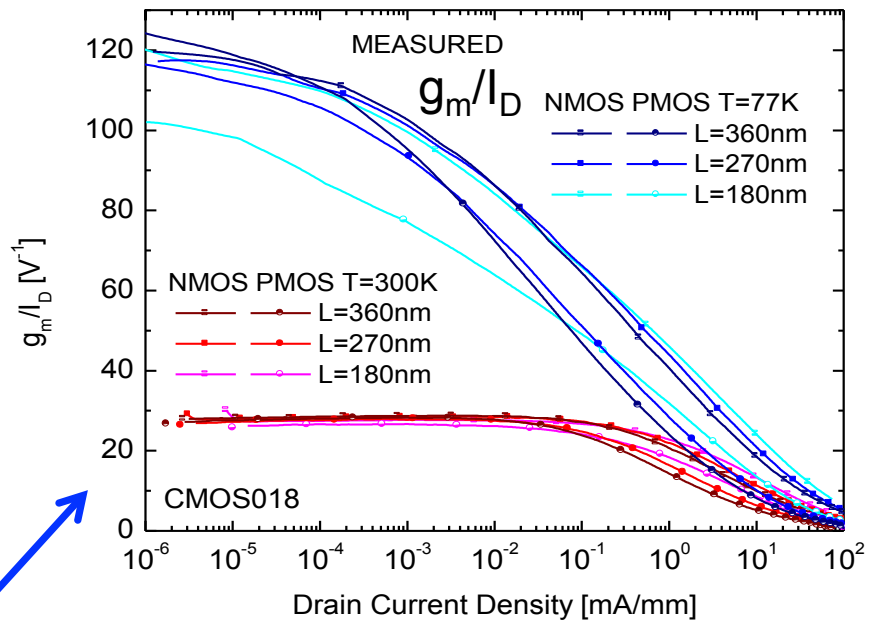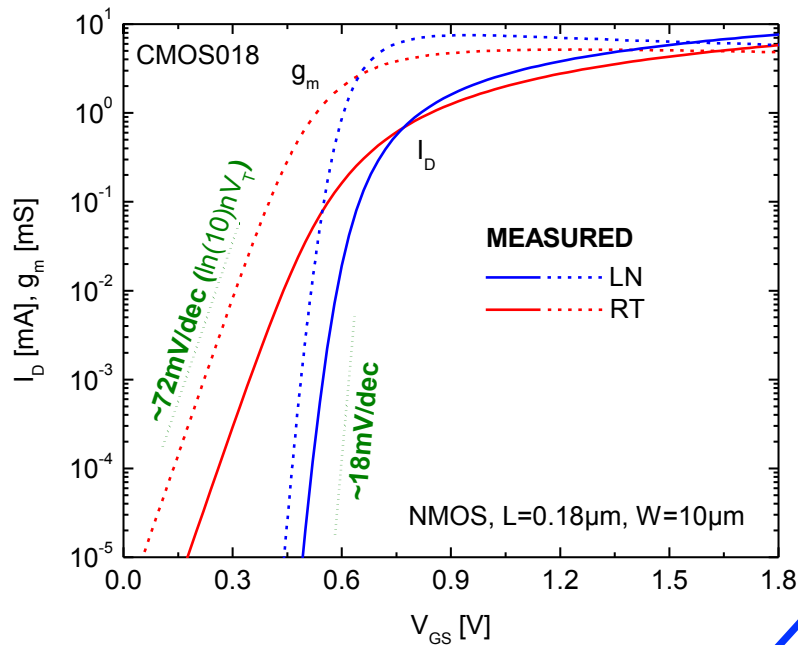**DUNE with warm electronics (300K) ENC~6×10^3 e rms**

Signal for (1/e drift)

3x3   5x5

$10^4 e$
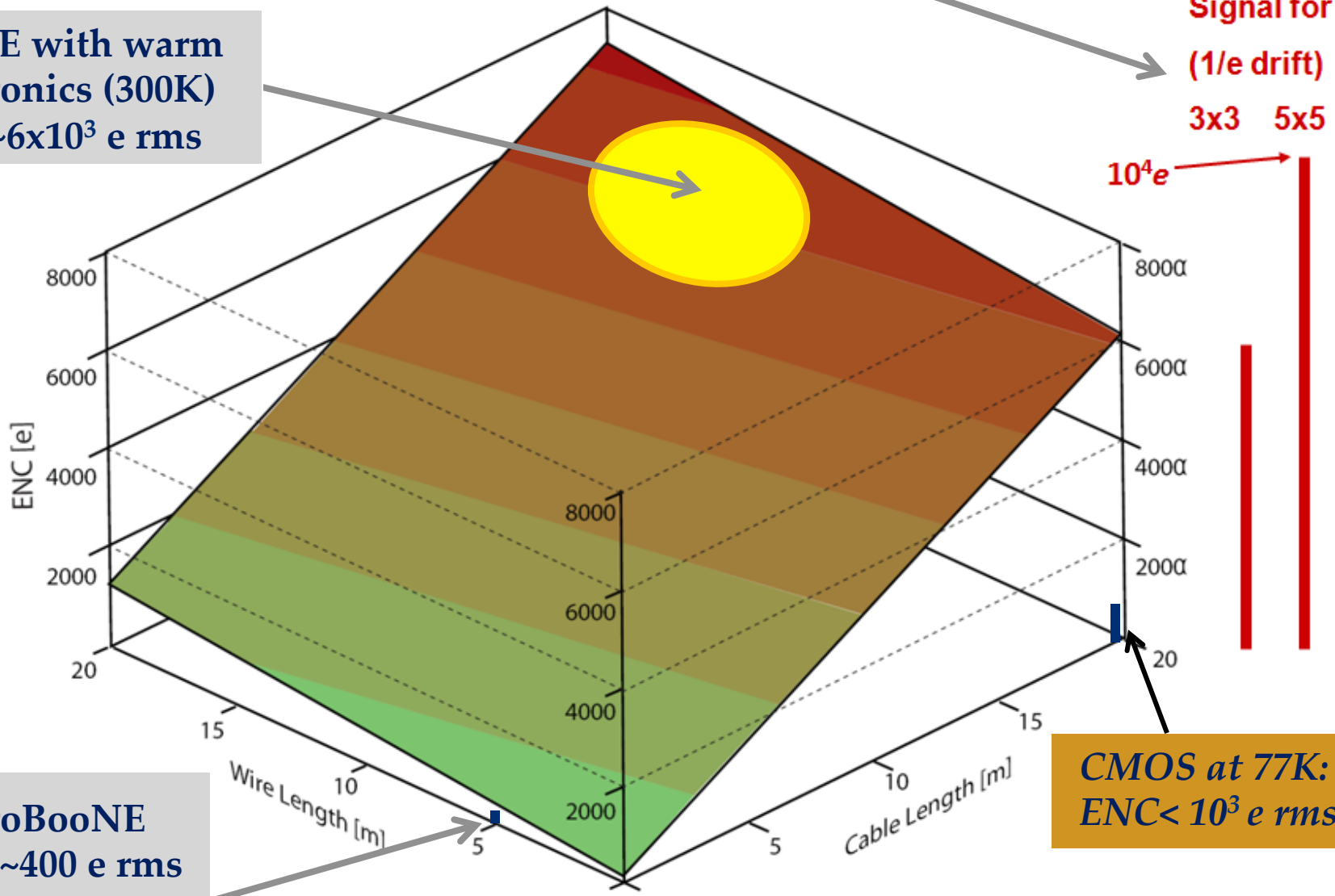
MicroBooNE ENC~400 e rms

CMOS at 77K: ENC< 10^3 e rms

CMOS Characteristics in LAr

$$\text{Transconductance/drain current} \quad \Longrightarrow \quad \frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 & at \ T = 300K \\ \sim 116 & at \ T = 77K \end{cases}$$

At 77-89K, charge carrier **mobility** in silicon _increases_ and **thermal fluctuations** _decrease_ with **kT/e**, resulting in a **higher gain**, **higher** g_m/I_D, **higher speed** and **lower noise**.

- In parallel, studies of **CMOS lifetime and reliability** at 77 K have been conducted
  - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*

CMOS Lifetime Study – Principle Findings

- A study of hot-electron effects on the device lifetime has been performed for the TSMC NMOS 180nm technology node at 300K and 77K. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (V_{ds}), and a separate measurement of the substrate current (I_{sub}) as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current, $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of V_{ds} *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and DUNE falls naturally into this domain, where hot-electron effects are negligible.*

- The slope of lifetime vs $1/V_{ds}$ is independent of the technology node (from 180, 130 to 65 nm) and of the foundry (TSMC, Global …). For all three nodes the lifetime is extended by an order of magnitude if V_{dd} (V_{ds}) is reduced by **~6%**. This may be related also to the two basic underlying parameters, *electron energy* for *impact ionization* and for *creation of an interface state*, as well as *their ratio.*

Basics on Hot-electron effects (HEC) and NMOS lifetime

- In deep submicron NMOS (L<0.25μm) electrons can become "hot" at any temperature, by attaining energy $E > kT$.

- Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \cong 1.3eV$ resulting in *impact ionization*. Electrons proceed to the drain. The *holes* drift to the substrate. The **substrate current**,

$$I_{sub} = C_1 I_{ds} e^{-\varphi_i/q\lambda E_m} \qquad (1)$$

- A very small fraction of hot electrons exceeds the energy required to create an **interface state** (e.g., an acceptor-like trap), in the Si-SiO$_2$ interface, $\varphi_{it} \geq 3.7eV$ for electrons (~4.6eV for holes). This causes a change in the transistor characteristics (transconductance, threshold, intrinsic gain).

- The time required to change any important parameter (the changes in different parameters are correlated) by a specified amount (e.g., g$_m$ by ~10%) is defined as the **device lifetime**. It can be calculated as,

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it}/q\lambda E_m} \qquad (2)$$
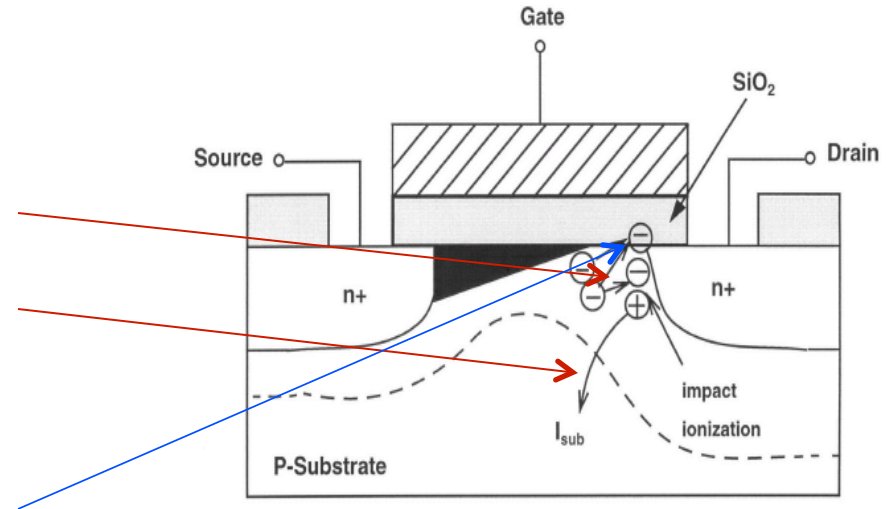
q = electron charge
λ = electron mean free path
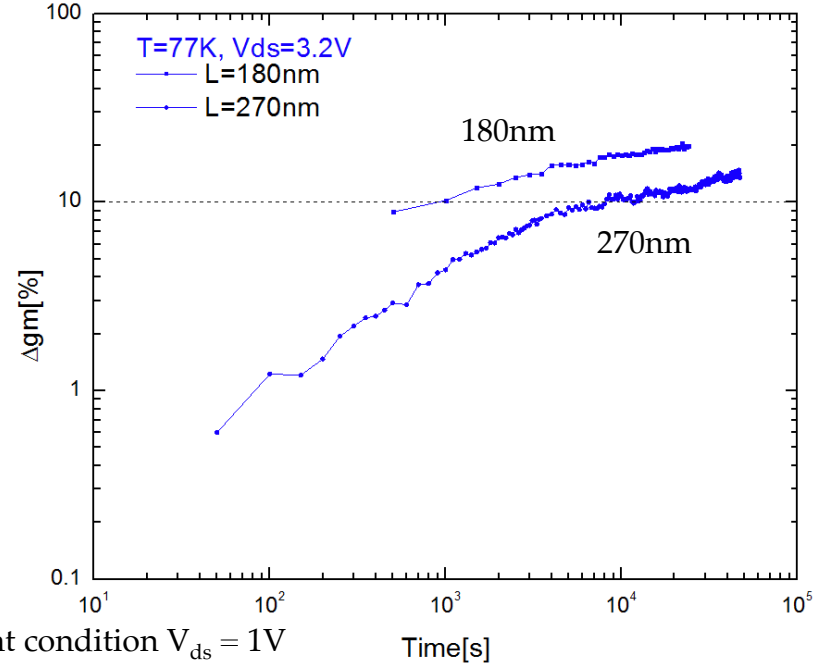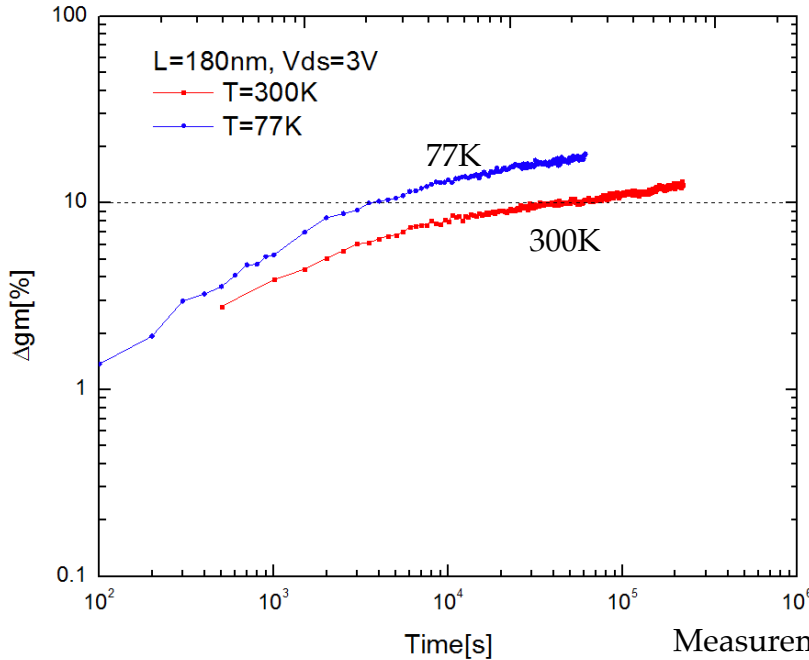E_m = *electric field*

I_{ds} = drain-source current
W = channel width

C_1, C_2 - constants

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it}/q\lambda E_m}$$

Different T: Lower T, higher λ, lower τ Different L: Shorter L, higher E_m, lower τ

Measurement condition $V_{ds} = 1V$

- Lifetime depends on the **drain current density** and the product of λE_m

- Devices at cryogenic temperature have shorter lifetime because **the phonon scattering decreases** at low temperature, resulting in **a longer mean free path** thus a higher λE_m, which means a higher amount of hot carriers, which leads to more severe HCE and shorter lifetime

- Devices with shorter length have shorter lifetime because the shorter length devices have **higher maximum electric field** under the same operating condition, thus a higher λE_m, which means a higher proportion of hot carriers, which leads to a more severe hot carrier effect and shorter lifetime. We use the **minimal length** device to represent the lifetime of the technology.
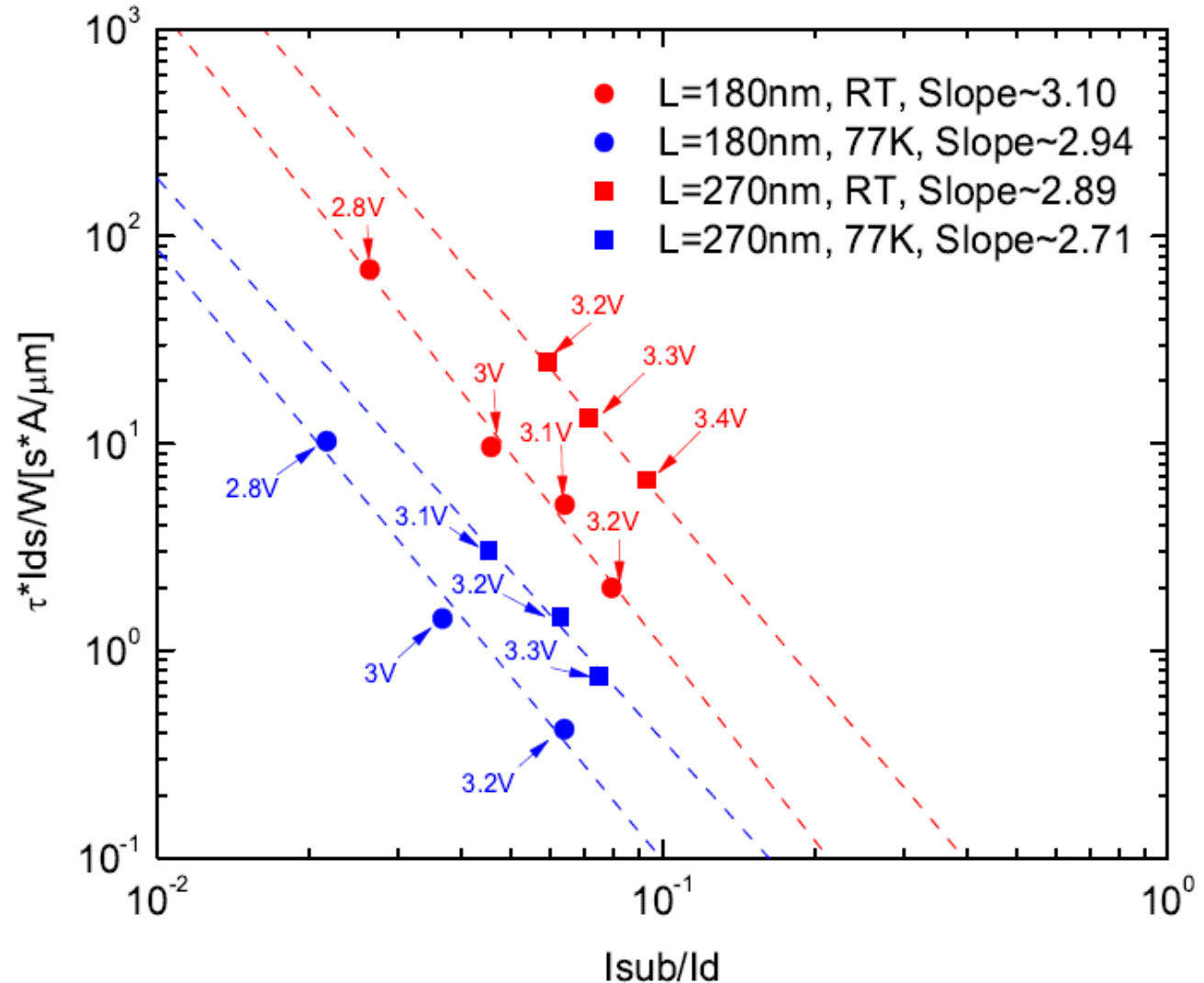
Lifetime vs substrate current (normalized to channel width and current): Slope $\alpha = \varphi_{it}/\varphi_i \approx 3$ test for TSMC L=180 and L=270 nm

$$\frac{\tau I_{ds}}{W} \propto \frac{I}{(I_{sub}/I_{ds})^{\alpha}}$$

The slope is largely independent of the channel length and temperature.

For constant I_{sub}/I_{ds}, the lifetime increases with channel length.

Each stress point is a new ("fresh") device sample (two different L devices, 13 samples in this plot).

CMOS in AC operation: Logic circuits and FPGAs

- It has been long established (1994) that *ac* and *dc* hot-carrier induced degradation is the same if the *effective stress time* is taken into account. This quasi-static model, confirmed recently (2006) considers the *ac stress as a series of short dc stresses strung together*

- The lifetime of a logic circuit driven at a clock frequency can be related to the lifetime of the NMOS transistor under continuous *ac* operation in terms of the ratio of the effective stress time during a change of state and the clock period. Thus the *Lifetime of digital circuits (ac operation) is extended by the inverse duty factor* $4/(f_{clock} t_{rise})$ *compared to dc operation.* This factor is large (>100) for deep submicron technology and clock frequencies needed for TPC readout.

- Design guidelines for digital circuits and FPGAs: *Keep the inverse duty factor high*. As an additional conservative measure, reduce V_{ds} by 10%, adding an order of magnitude margin to the lifetime.

# Effective Stress Time is a small fraction of the Clock Cycle:
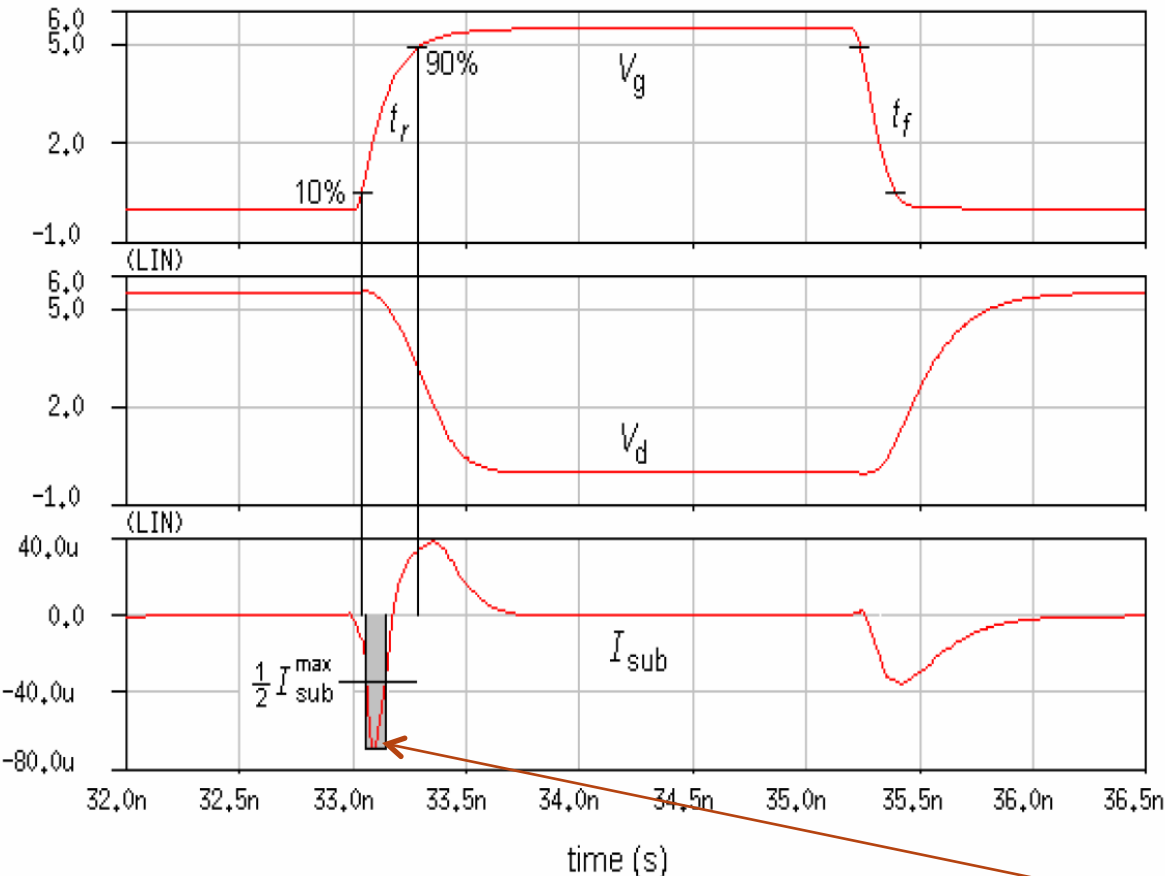
$$\left[\frac{ac\,stress\,time}{dc\,stress\,time}\right] \approx \left(f_{clock}\,t_{rise}\right)\Big/4$$

Lifetime of digital circuits (ac operation) is extended by the inverse duty factor compared to dc operation.
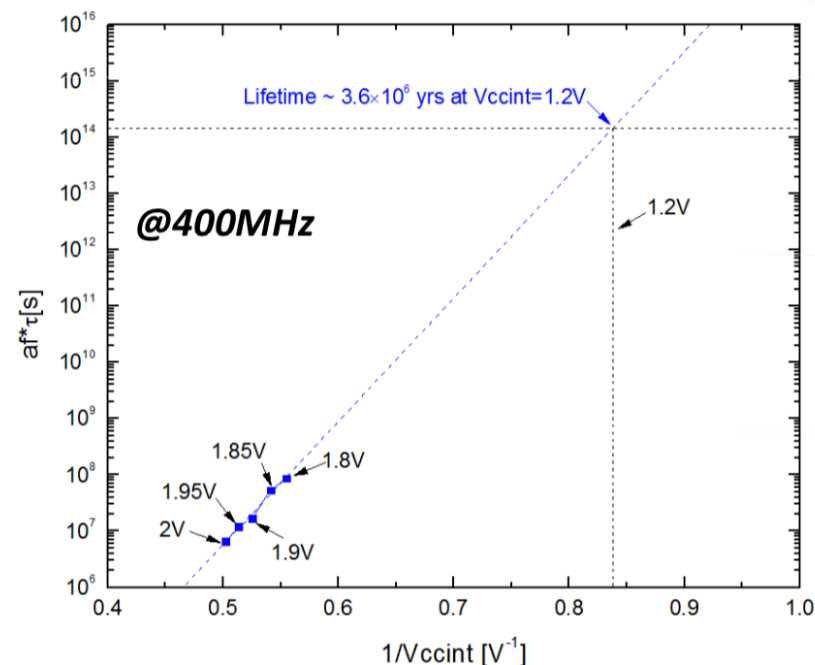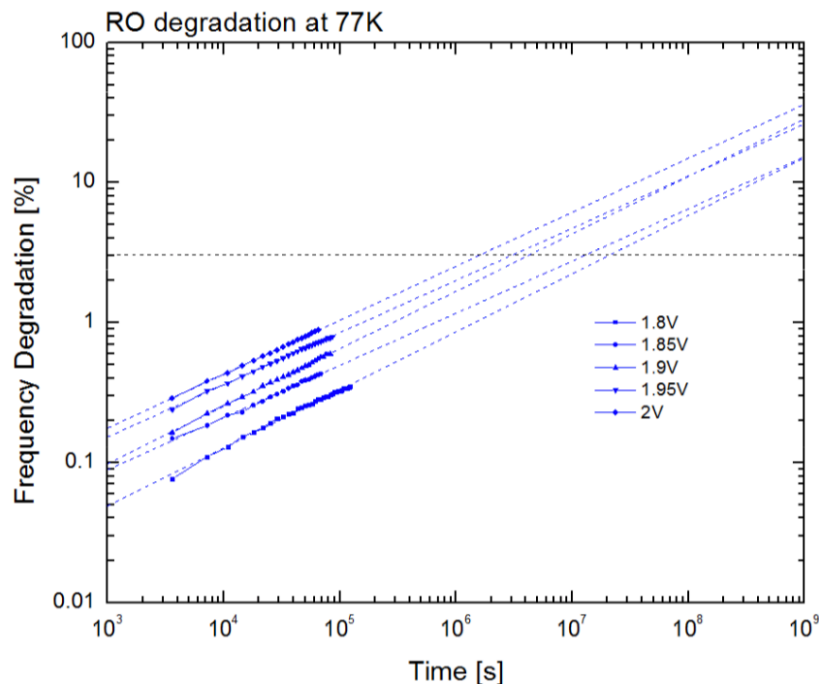This factor is large (>100) for COTS ADC with $f_{\text{clock}} >$ 32 MHz and $t_{\text{rise}} <$ 500 ps.

Hot-carrier induced degradation occurs only when the <u>substrate current</u> is high, i.e., nominal V_{ds} and high I_{ds}.

Accelerated Lifetime Measurement of 3.3 V node: very steep dependence on V_{ds}
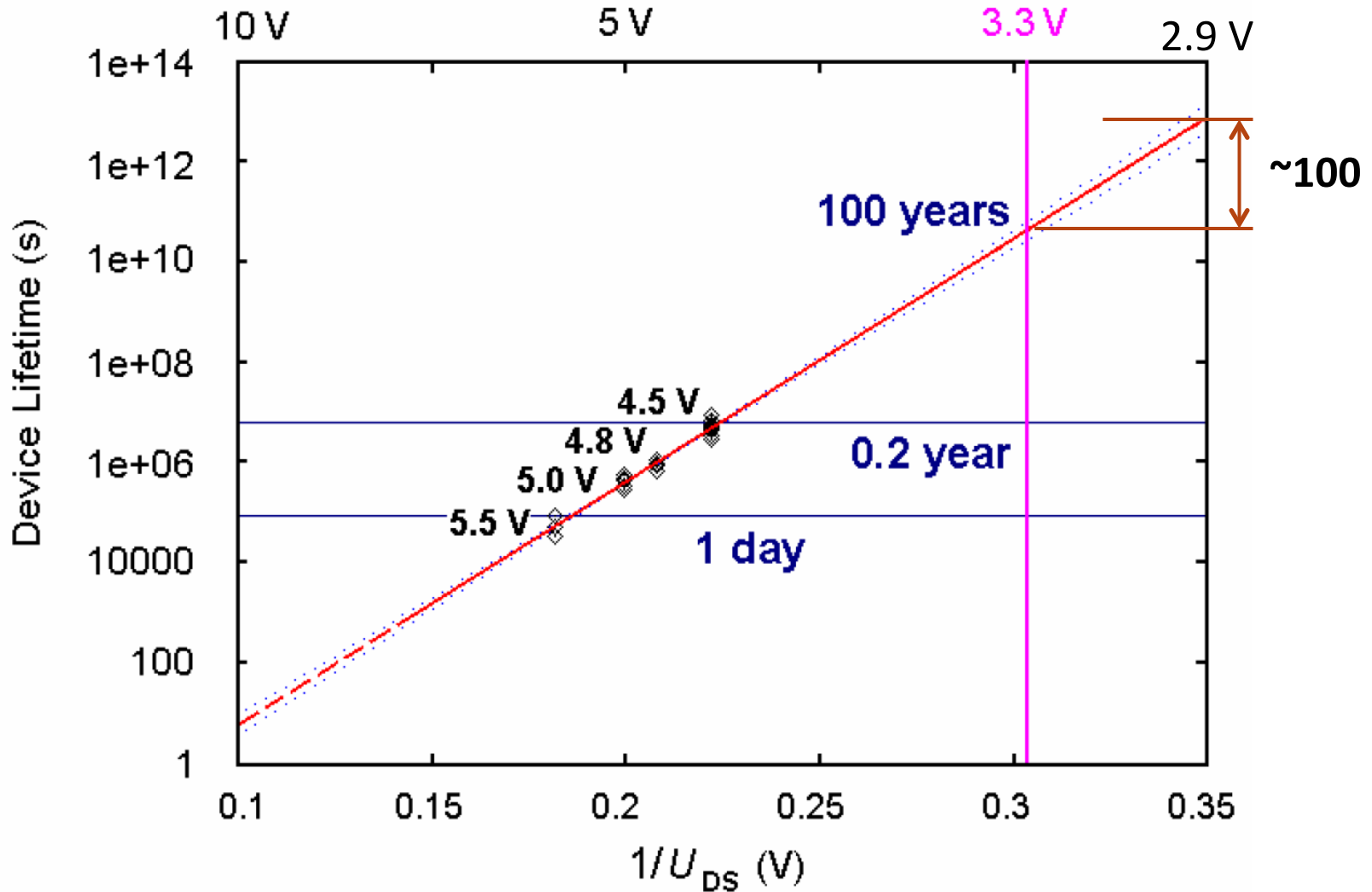
Lifetime Projection of FPGA

- Traditionally, lifetime is projected by empirical equation $log_{10}\tau \propto 1/V_{ds}$. The target operation frequency is 400MHz while the RO is stress under 1.7GHz. To include the effect of higher stress frequency, frequency acceleration factor α_f is introduced which is defined as $\alpha_f = \dfrac{f_{stress}}{f_{target}}$. The equation for lifetime projection is modified as:

$$log_{10}\alpha_f\tau \propto 1/V_{ds}$$

- Following the above equation, lifetime of FPGA at 77K is projected to be 3.6×10^6 years for 3% degradation criteria, giving a wide margin over the physical target (>20 years) .

Failure Rate and MTBF/MTTF*

- **MTBF** (Mean Time Between Failures) and Failure Rate λ=1/MTBF approach to Reliability, assumes a random process, where the failure rate is constant and the distribution of time intervals between failures is given by Poisson statistics.

- **Reliability** is defined as the probability that a component (transistor, circuit, subsystem, or entire system) will operate, as specified, over a given time without failure. In terms of Failure Rate, or MTBF, it is given by,

$$R = e^{-\lambda t} = e^{-t/MTBF}$$

- **Mission/Service Life** is useful life as limited by any mechanism, random failure, or **wear/aging,** uniform and understood for a given class of components.

- **MTBF (Reliability)** is a probability parameter for a random process. It can be controlled by the design, choice of components, and various quality control tools.

- **Wear/aging** is given by the physical/chemical processes, with all devices of the same type subject to the same process. It can be controlled only by the design and the operating conditions.

MTBF example (2)

- Setting R close to unity (probability of failure very low),

$$MTBF \geq \frac{t}{1-R}$$

- Assume R=0.999, i.e, probability of failure ~0.1%. It follows,

$$MTBF \geq 10^3 t$$

- For t=1 year →MTBF~1000 years

- For humans, a 25 year old has R (1 year)~0.999, or MTBF 1000 years, but it has a "service life" much shorter due to wear/aging.

- In most cases Service Life is shorter than MTBF