Trigger Merging Module for the J-PARC E16 Experiment

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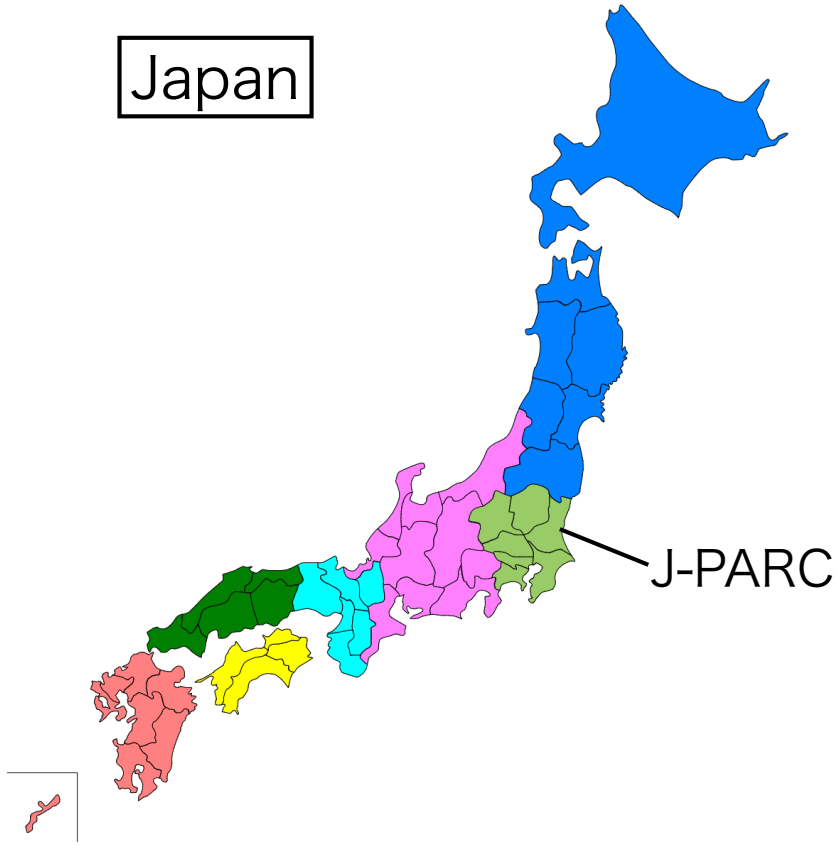
Outline

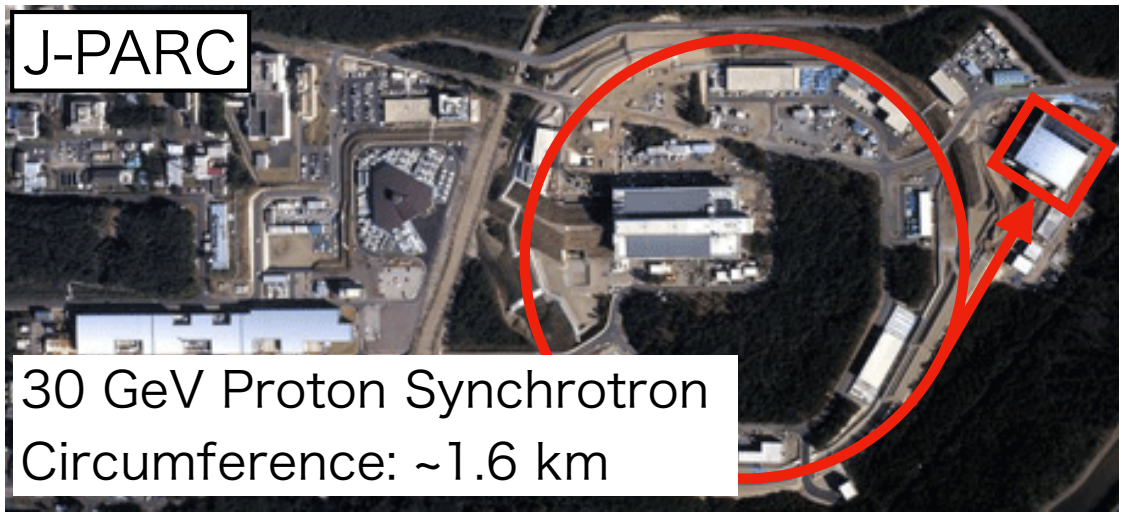
○J-PARC E16 Experiment
- Detectors
- Trigger System

○Trigger Merging Module(TRG-MRG)
- Hardware
- Firmware

○Performance Test
- Time Resolution
- Latency
- Transfer Efficiency

○Summary



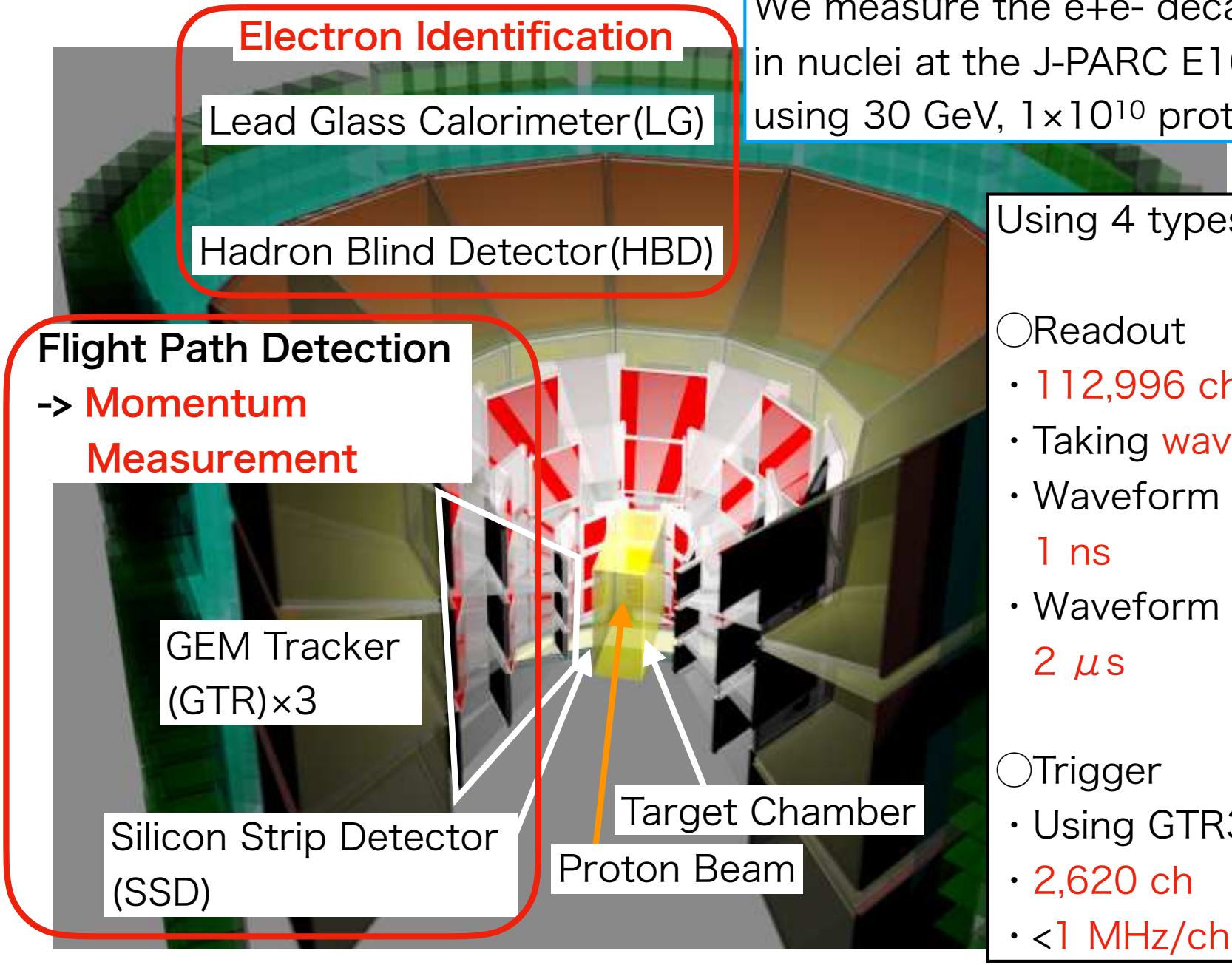


※The E16 experiment will start 2019

J-PARC E16 Experiment

Detectors

We measure the e+e- decays of ϕ mesons in nuclei at the J-PARC E16 experiment using 30 GeV, 1×10^{10} protons/pulse

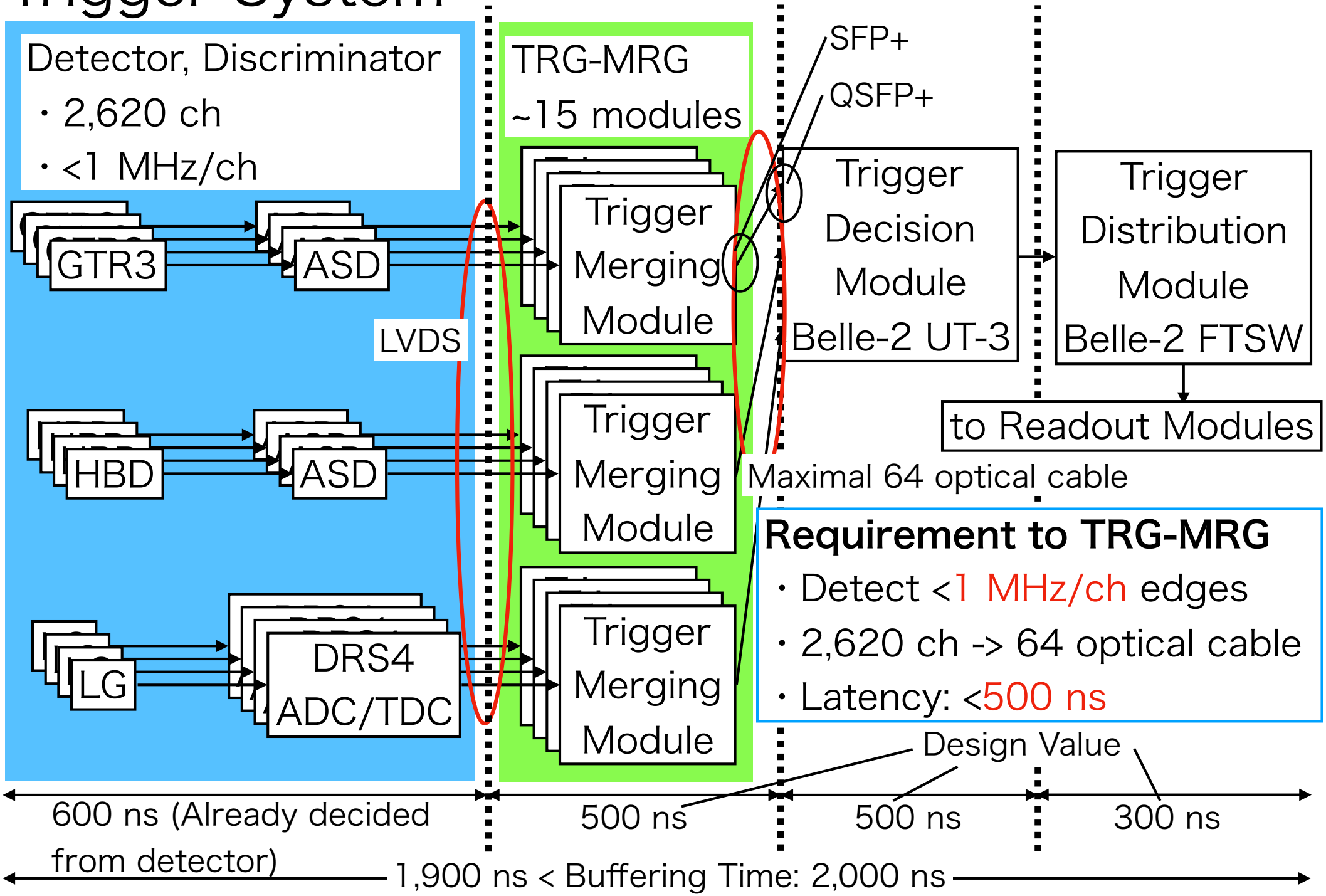


Using 4 types detectors

○Readout
- 112,996 ch
- Taking waveform data
- Waveform sampling time: 1 ns
- Waveform buffering time: 2 μs

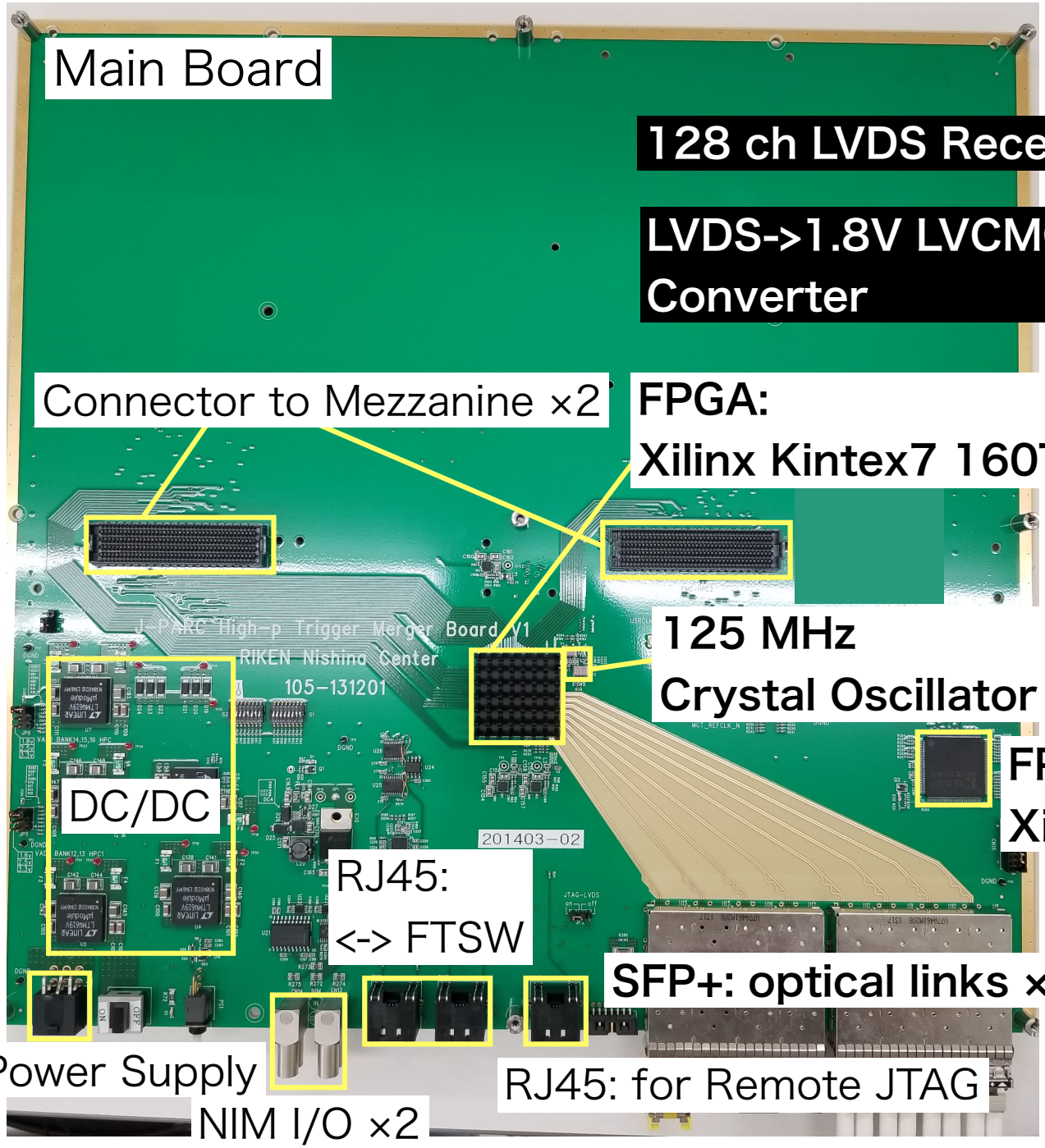
○Trigger
- Using GTR3, HBD, LG
- 2,620 ch
- <1 MHz/ch

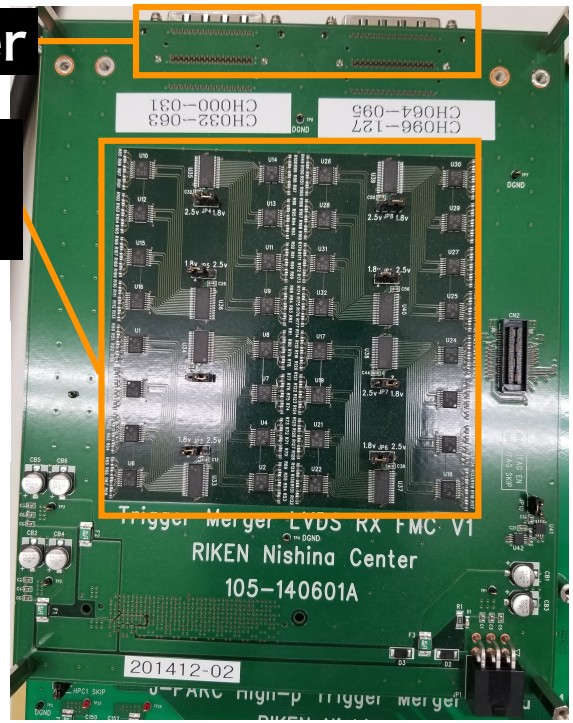
Trigger System



Trigger Merging Module (TRG-MRG)

TRG-MRG: Hardware



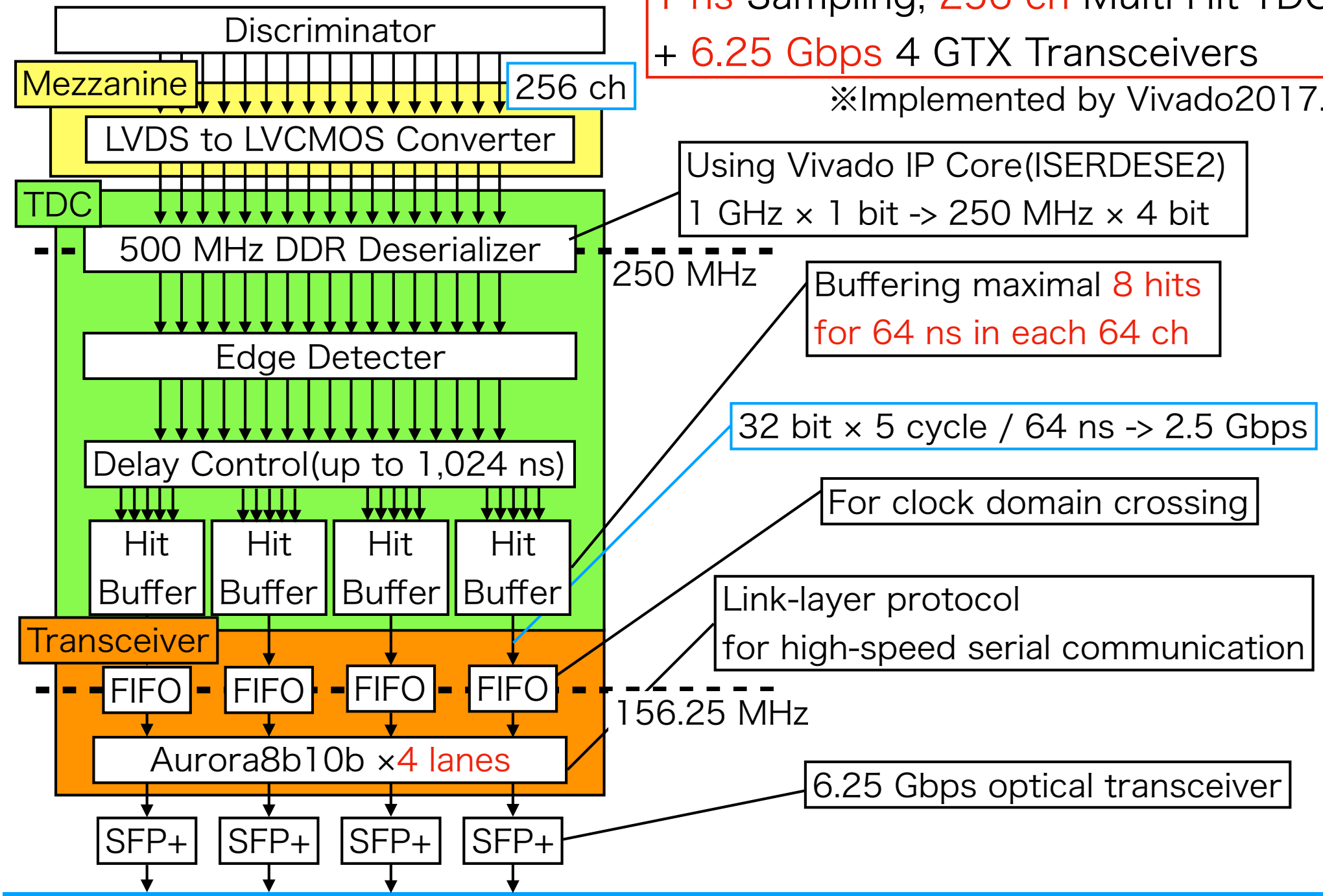


FPGA:
Xilinx Spartan3 50AN-4

TRG-MRG: Firmware

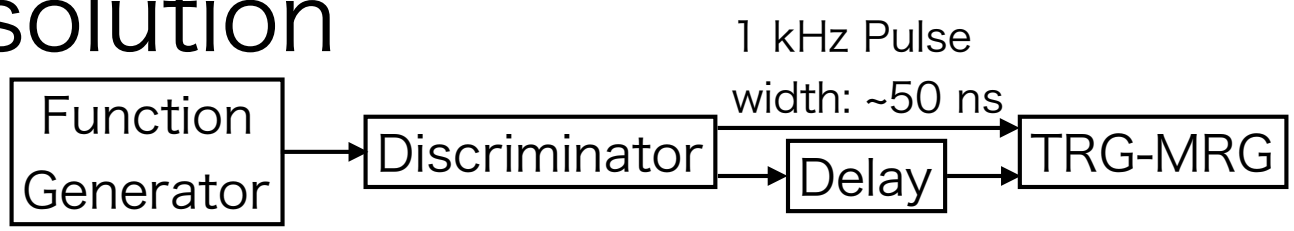
1 ns Sampling, 256 ch Multi Hit TDC
+ 6.25 Gbps 4 GTX Transceivers

※Implemented by Vivado2017.2

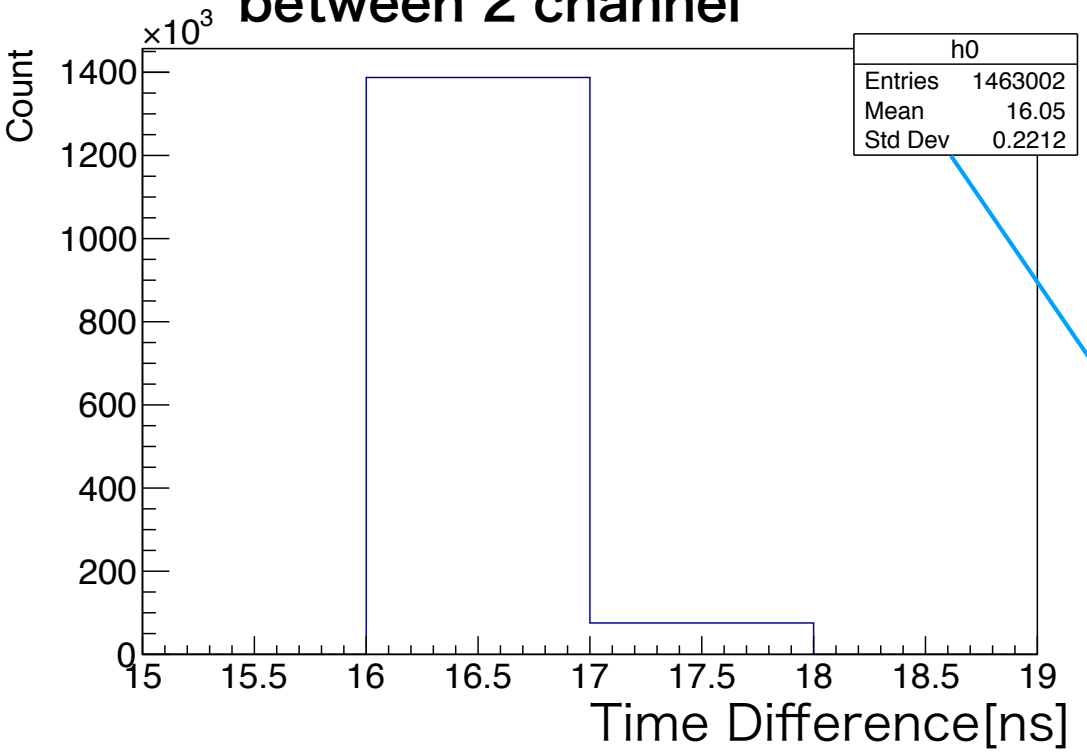


Performance Test

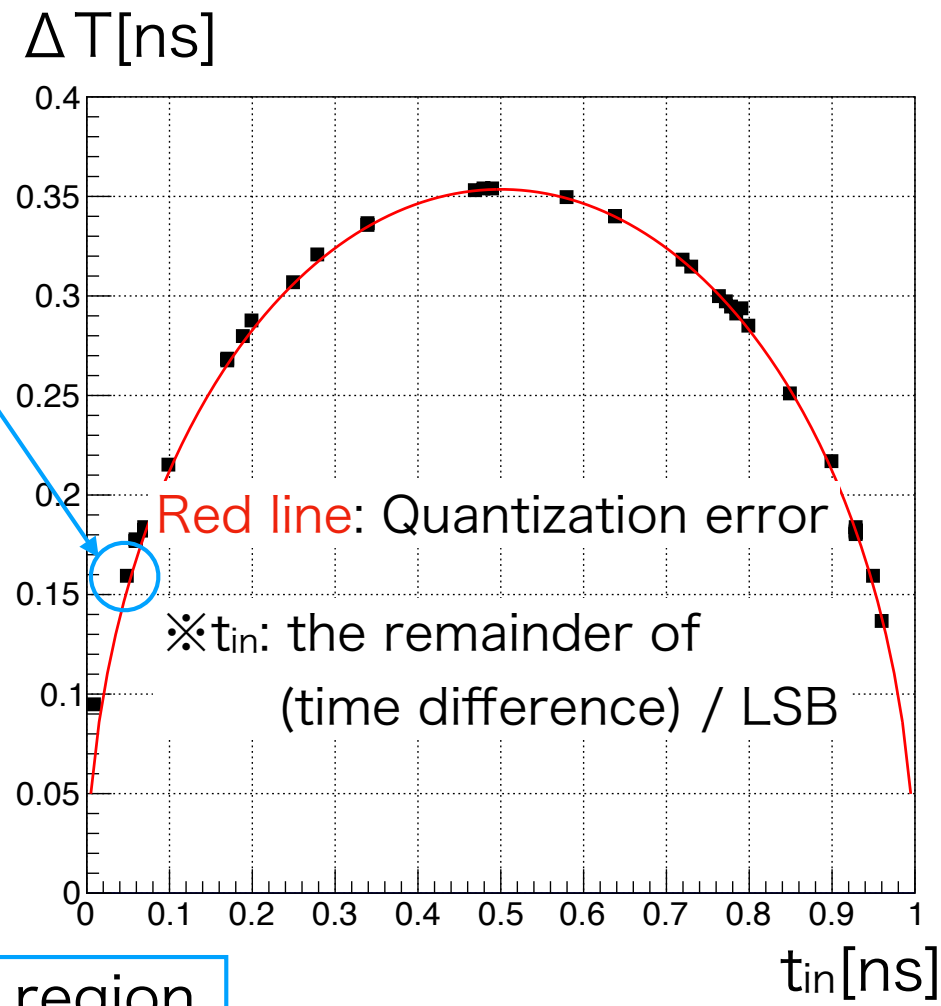
Time Resolution



Distribution of time difference between 2 channel



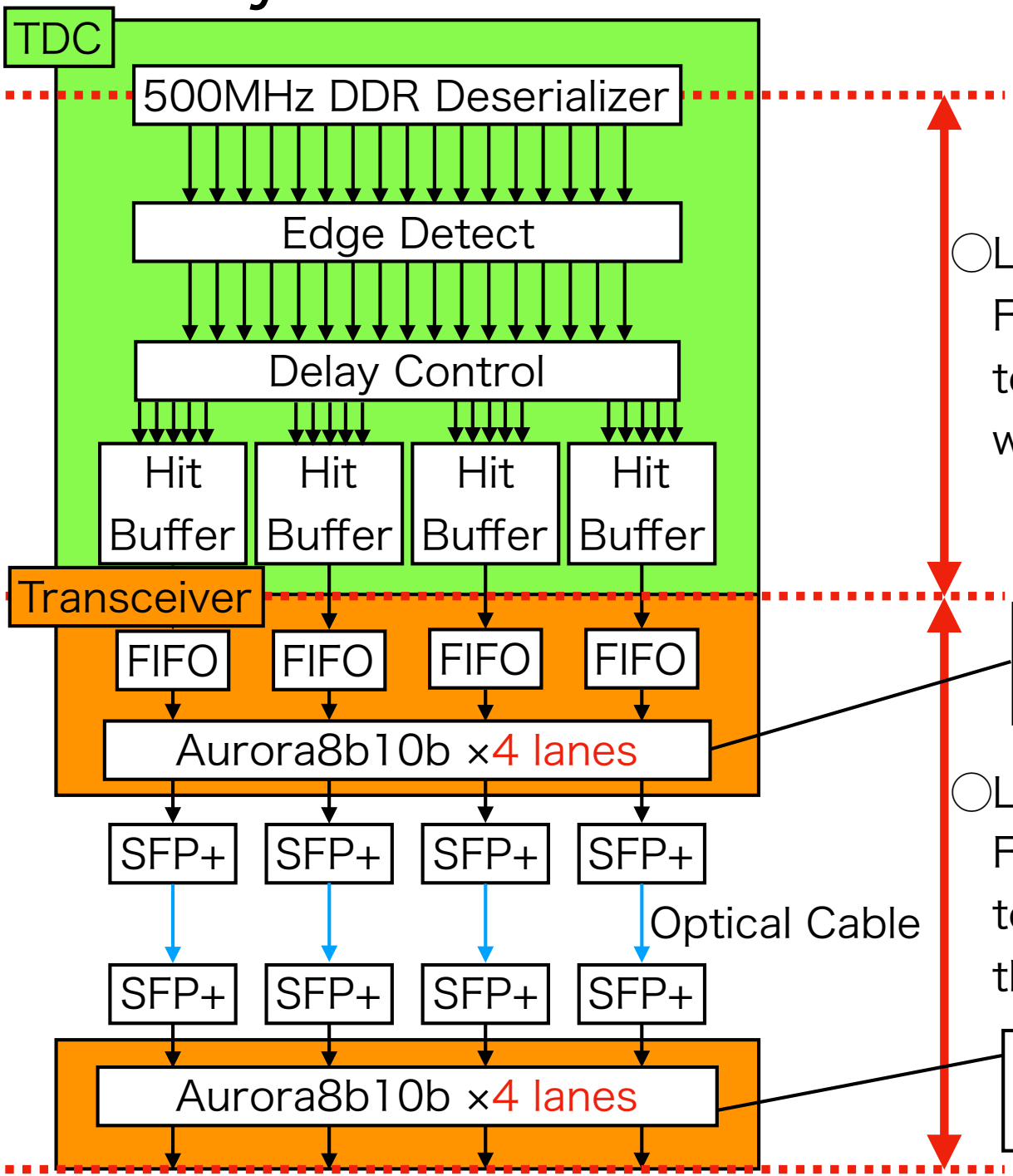
Distribution of time resolution



Time resolution < 0.35 ns in all t_{in} region

Good agreement with expected error

Latency



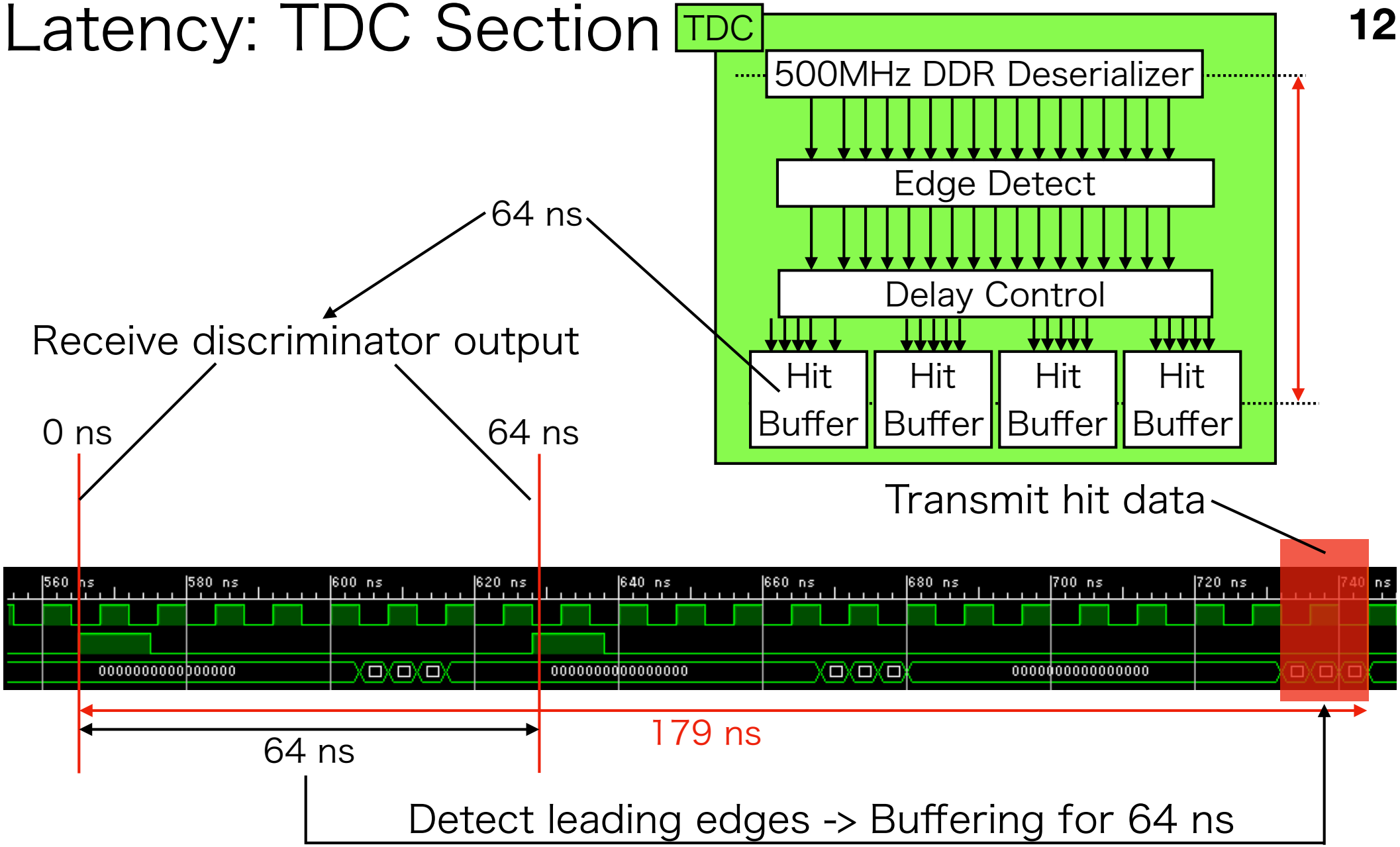
○Latency of TDC section
From deserializing LVDS signals
to transmitting data to transceivers
with no delay

Encode
Serialize

○Latency of transceiver section
From inputting data to FIFO
to outputting data from Aurora
through optical cable

Deserialize
Decode

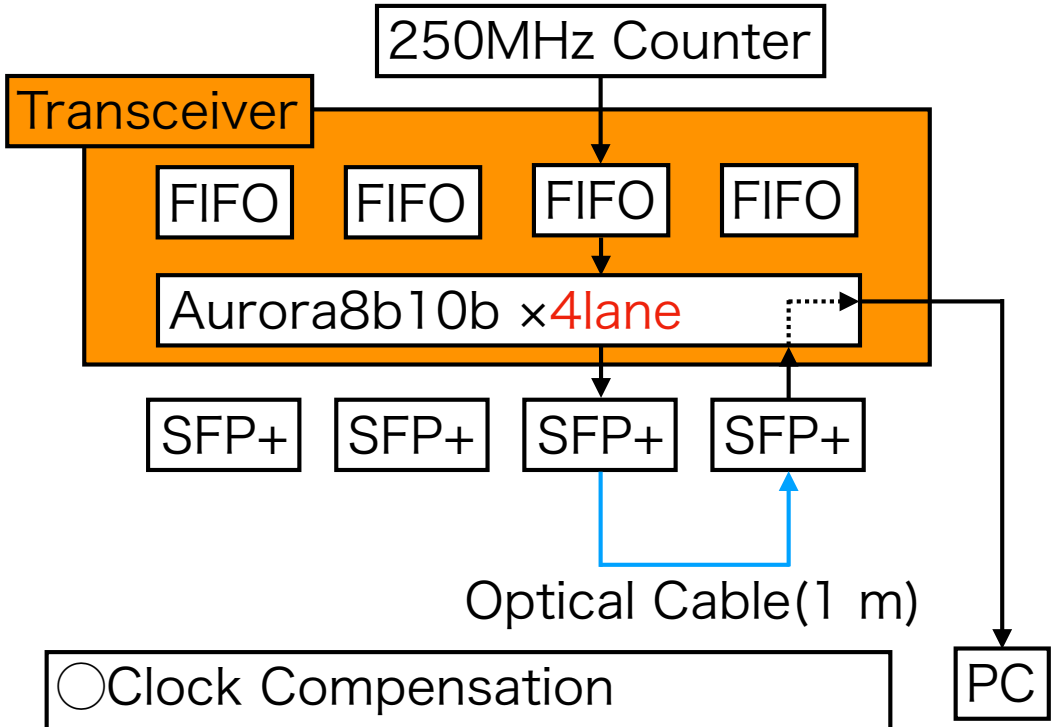
Latency: TDC Section



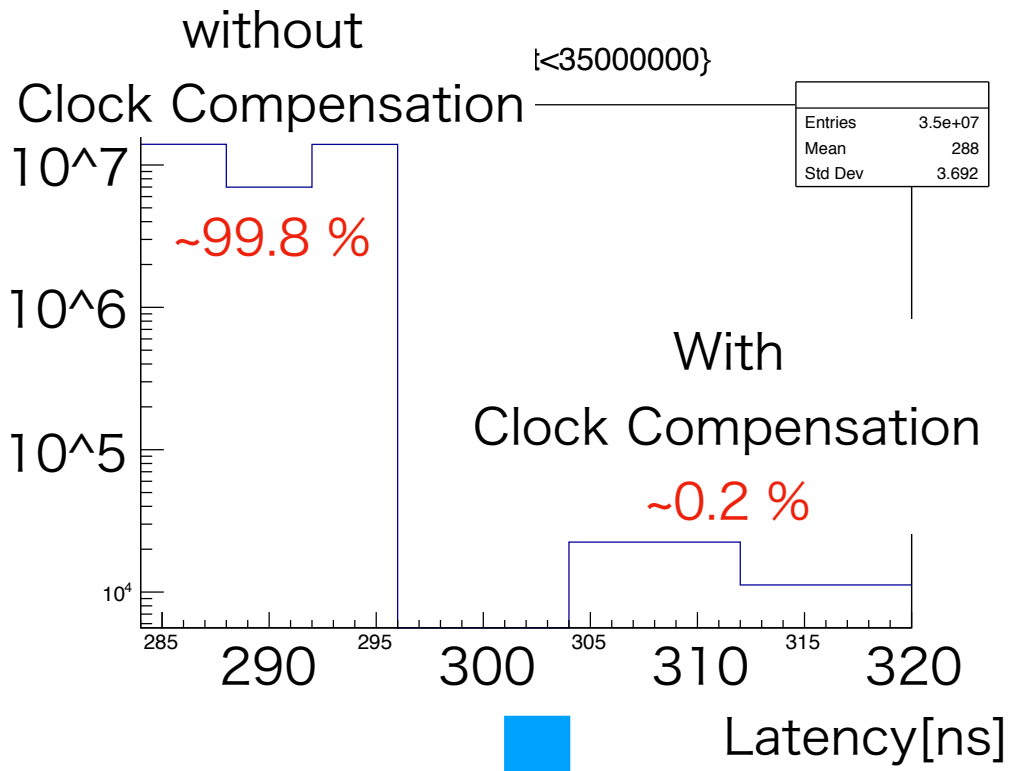
※Using circuit simulator in Vivado2017.2

Latency in TDC section is <179ns

Latency: Transceiver Section



Distribution of Latency



Latency(Transceiver) <320 ns

◯Clock Compensation

- Basic function of Aurora
- To synchronize between transmitting module and receiving module
- Output busy signal
  3 cycles in each 2,500 cycles

Total Latency: <179 ns + 320 ns = 499 ns
Satisfy the Requirement(500 ns)

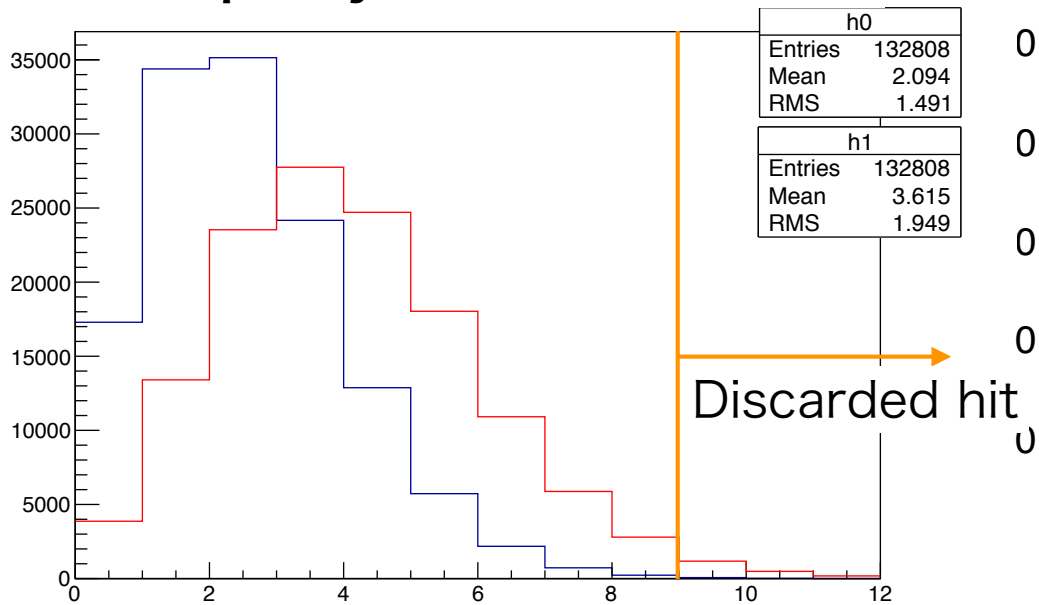
Transfer Efficiency of the Merging Criteria

Merging Criteria: Allow maximal 8 hits for 64 ns in 64 ch

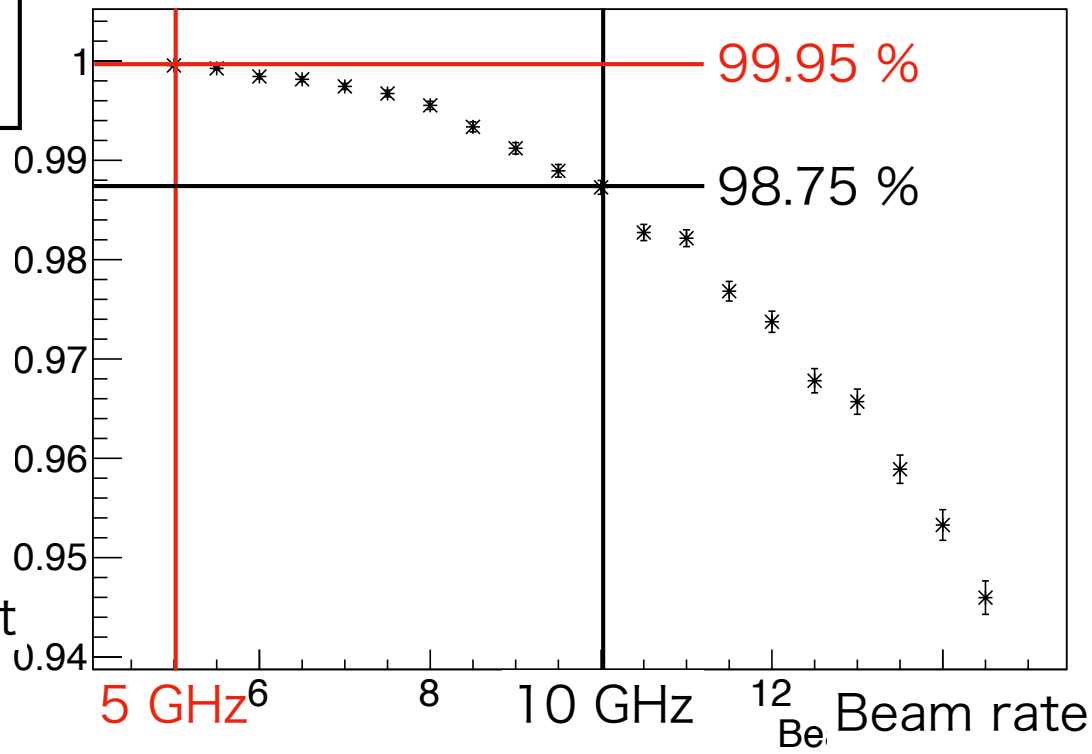
◯Simulate expected situation in the experiment with Geant4

- Beam Rate: 1×10^{10} /pulse (5 GHz)
- Single rate: <1 MHz/ch

Multiplicity for 64 ns in 64 ch



Beam intensity dependence of the transfer efficiency



Blue: Beam Rate = 5 GHz

Red: Beam Rate = 10 GHz

99.95% transfer efficiency in expected situation

Enough to use in the experiment

Summary

- Develop trigger merging module(TRG-MRG) for the J-PARC E16 Experiment

- Detect leading edges from discriminator output by FPGA
  and transmit serialized data to trigger decision module by SFP+

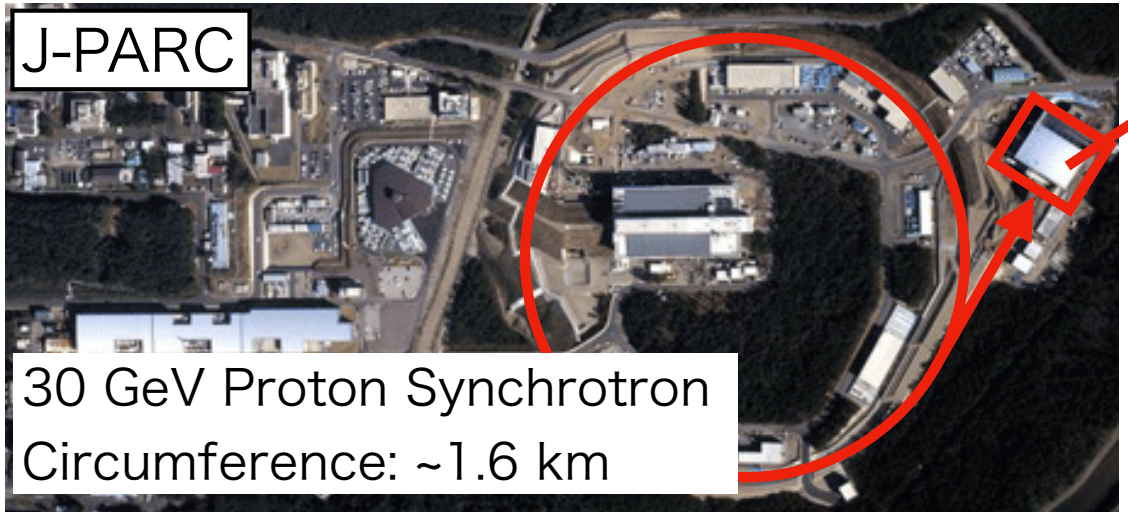
- 1 main board + 2 mezzanine cards
  - Mezzanine: Receive 128 ch/card LVDS signal + Convert LVDS to LVCMOS format
  - Main: 1 ns sampling, 256 ch Multi Hit TDC + 6.25 Gbps optical transceiver ×4

- Required performance is achieved
  - Time Resolution: <0.35 ns
  - Latency: <179 ns(TDC section) + 320 ns(Transceiver section) = 499 ns
  - Transfer Efficiency: 99.95 % in the expected situation in the experiment

TREG-MRG is Ready for the J-PARC E16 Experiment,
in Coming Autumn of 2019

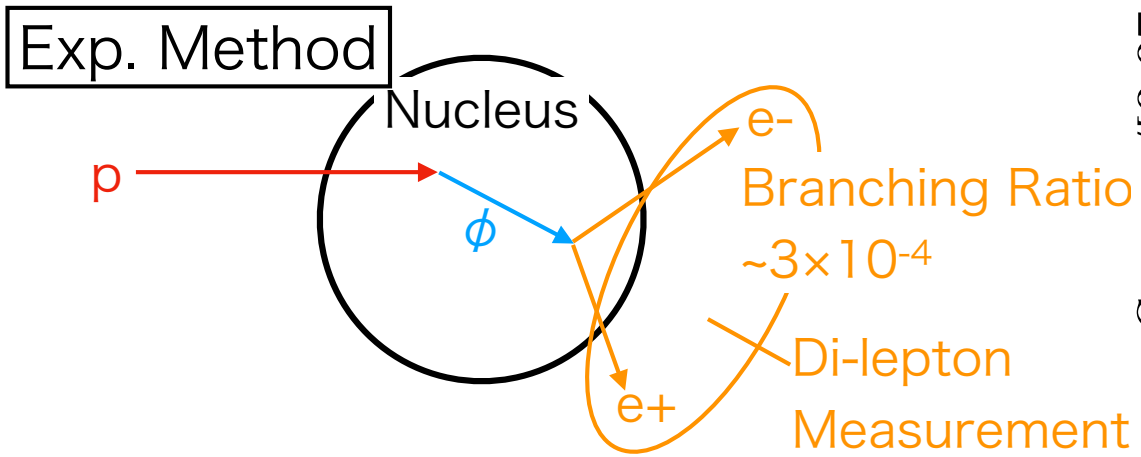
J-PARC E16 Experiment

Motivation: Restoration of chiral symmetry breaking under nuclear density
Method: Invariant mass spectroscopy of $\phi\,(\bar{s}s)$ in nuclear medium
Facility: Japan Proton Accelerator Research Complex(J-PARC)
High momentum(High-p) beam-line (Completed by FY2019)
Beam: 30 GeV proton, ~1×10^10 /pulse(~2 s)

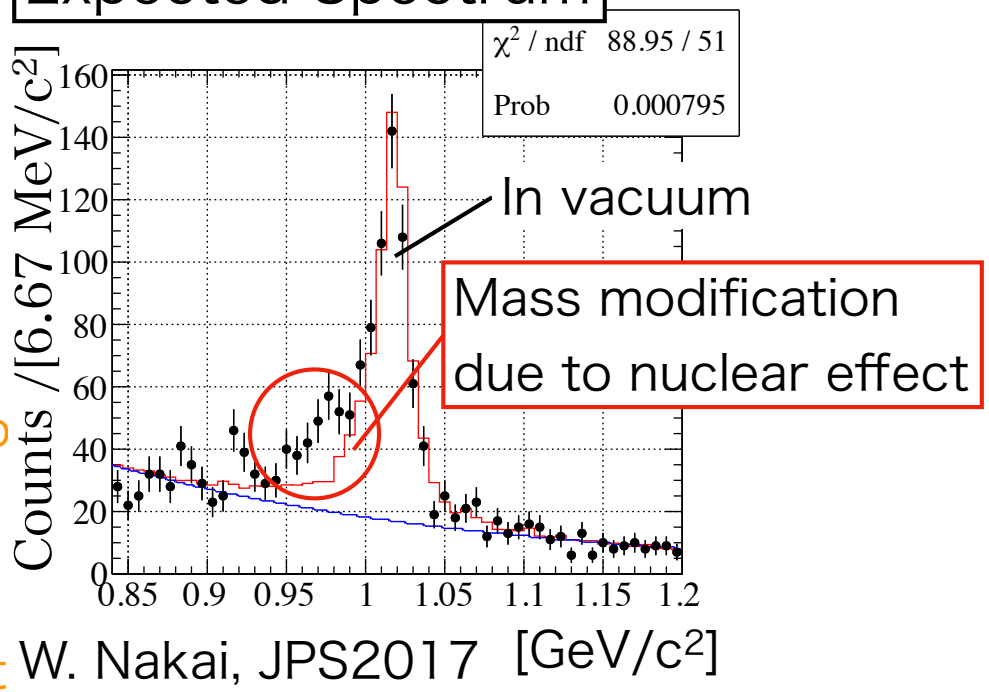


High-p beam-line

Exp. Method



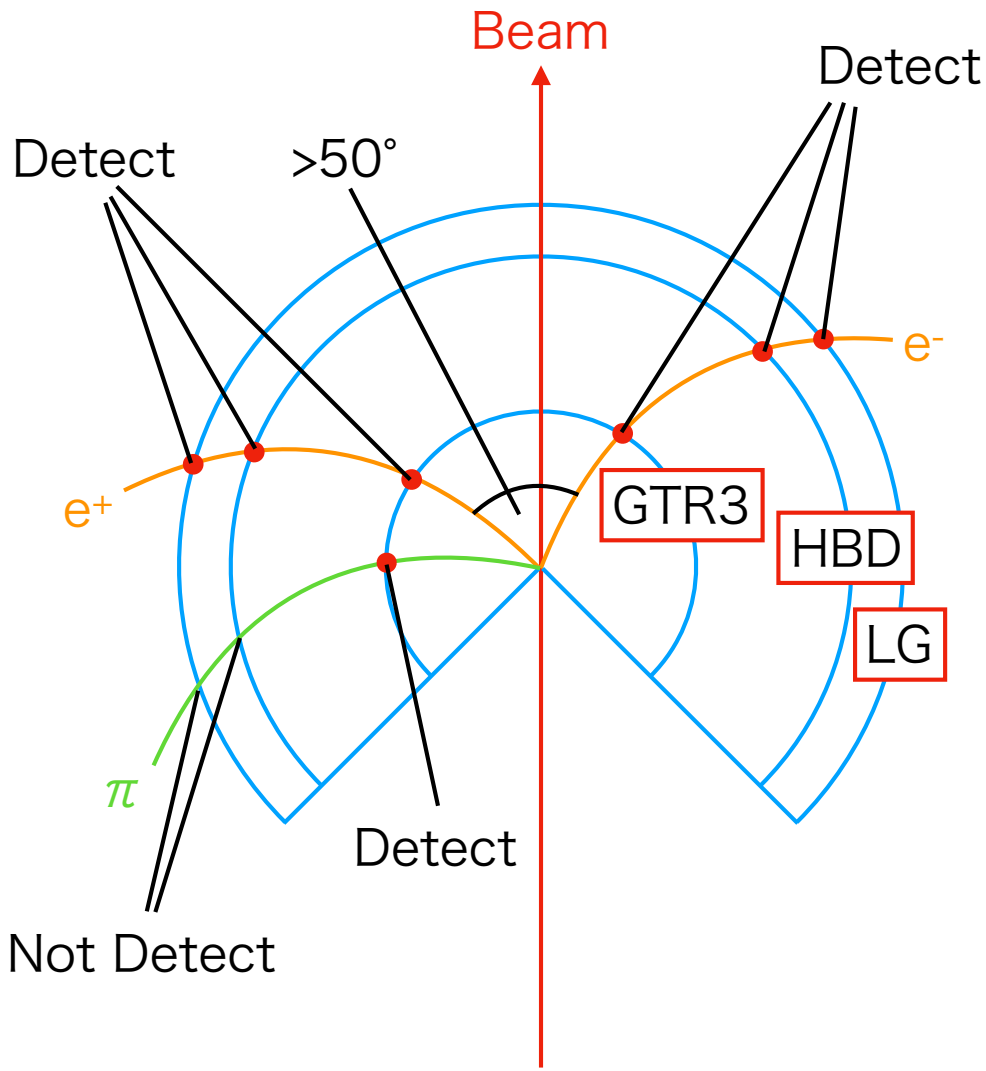
Expected Spectrum



W. Nakai, JPS2017

Trigger Concept

Top View of Detectors



○Target

e+ e- pair from ϕ

○Main Back Ground

- Miss ID of charged π
- e+e- from $\pi 0$
  - $\pi 0$ -> 2γ, γ Conversion
  - $\pi 0$ -> γ e+e- (Dalitz Decay)

○Method

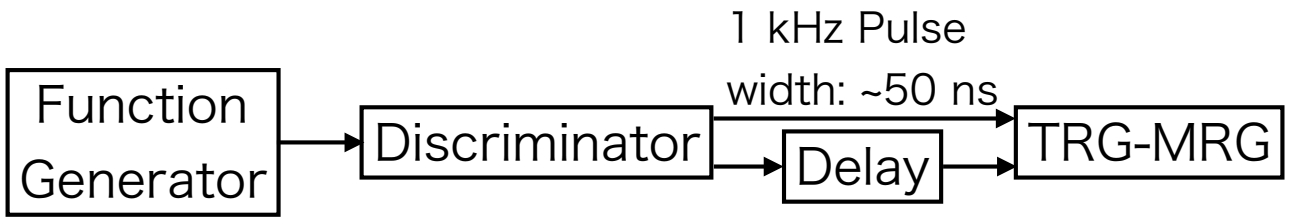
①Detect e+/e- track
by 3 detector's coincidence
(Single rate: <1 MHz/ch)
-> To avoid charged π

②Require the opening angle > 50°
-> To reject e+e- from $\pi 0$

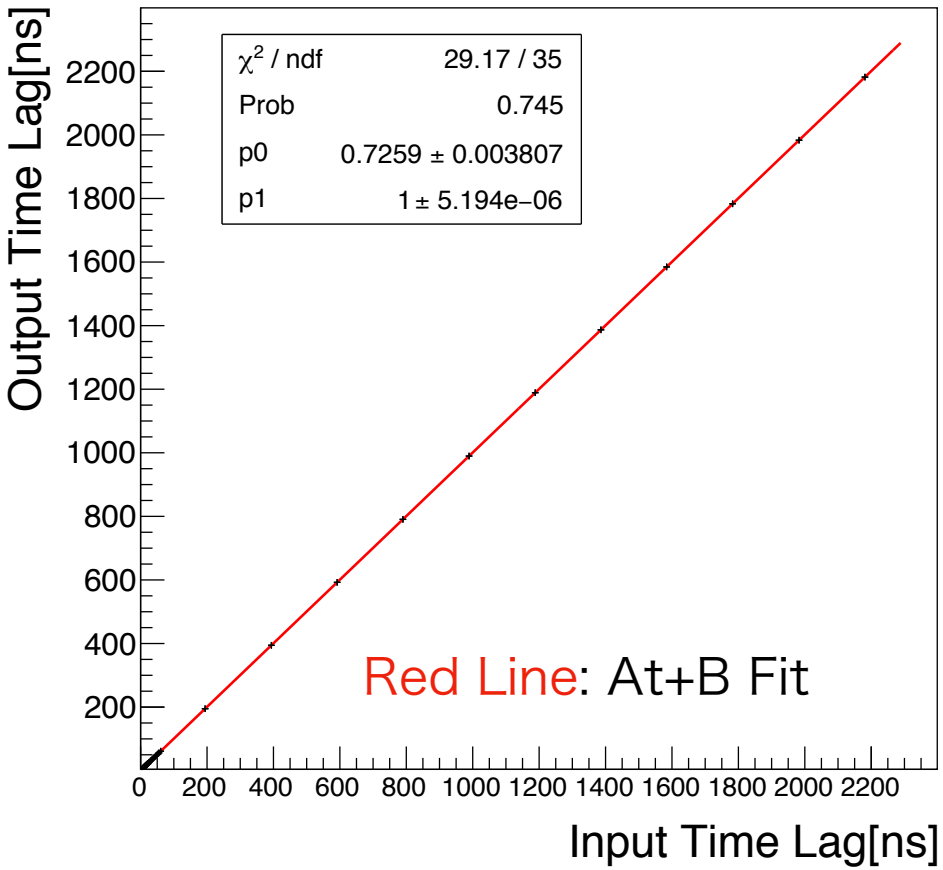
○Expected Trigger Condition

- Trigger rate: ~1 kHz
- ϕ -> ee Surviving Ratio: ~75 %

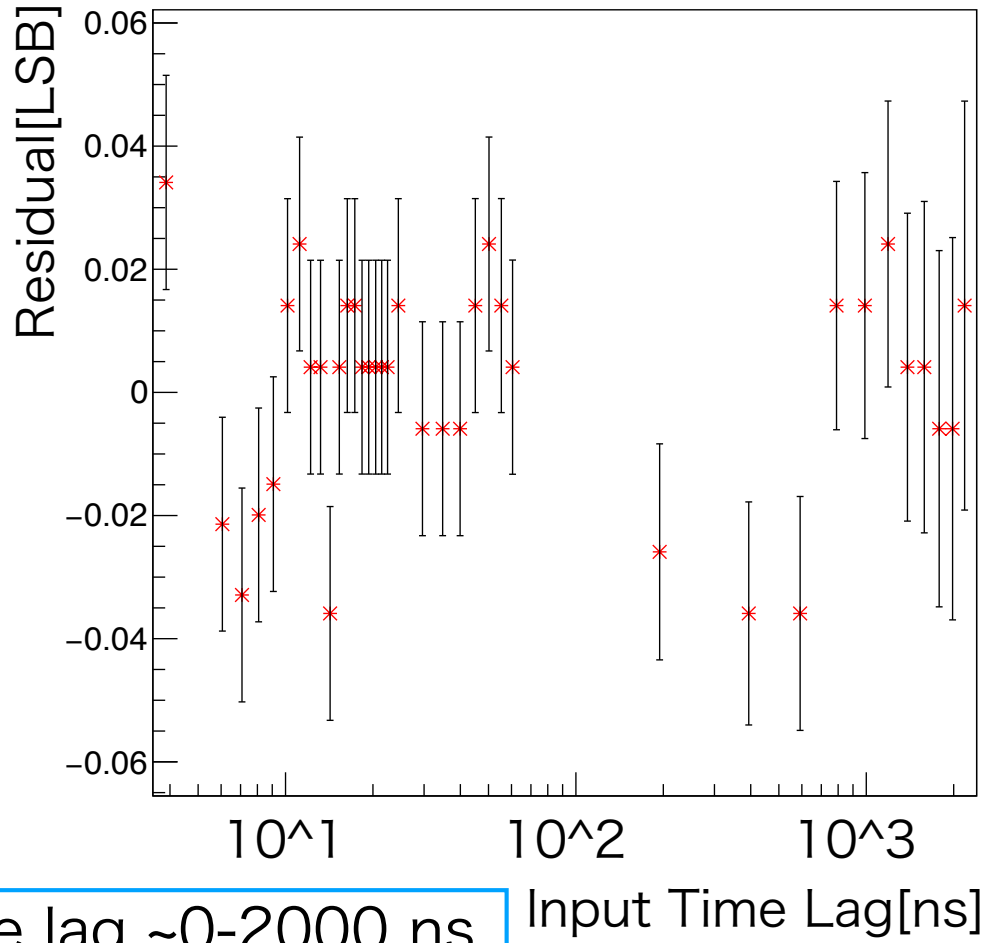
Integral Non Linearity(INL)



Relation between Input/Output Time Lag



Distribution of Residual



INL = [-0.04, +0.04] LSB with time lag ~0-2000 ns

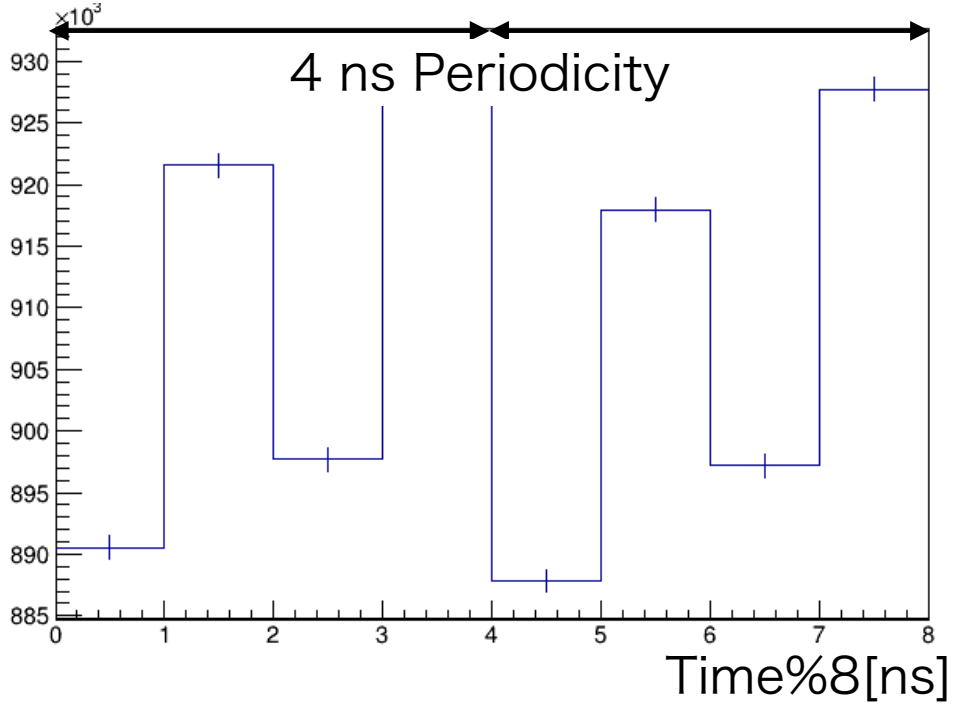
No bad influence

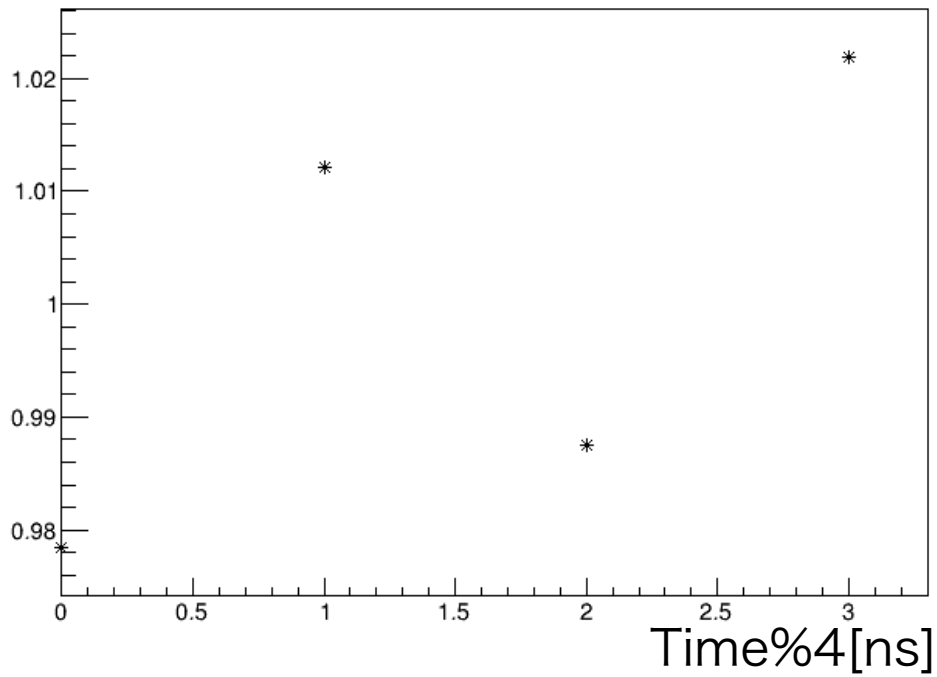
Differential Non Linearity(DNL)

80.008 ns Clock → TRG-MRG

Deserialize 1 GHz -> 250 MHz
-> Clock interval has 4 ns periodicity
-> Check each clock width
from distribution of input clock signal

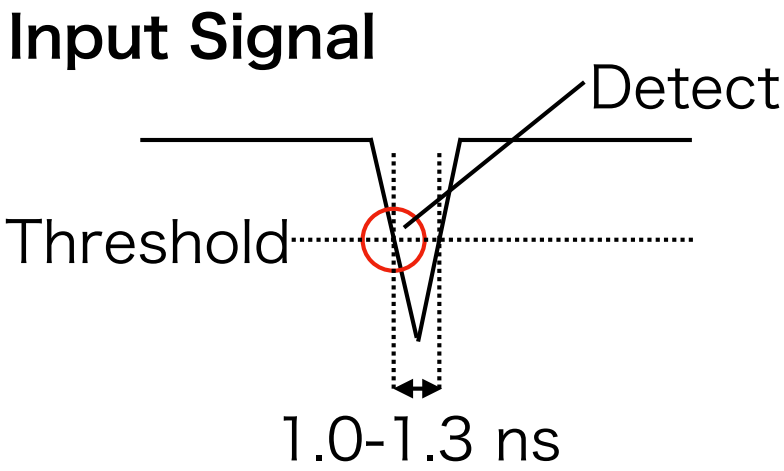
Distribution of clock edge timing





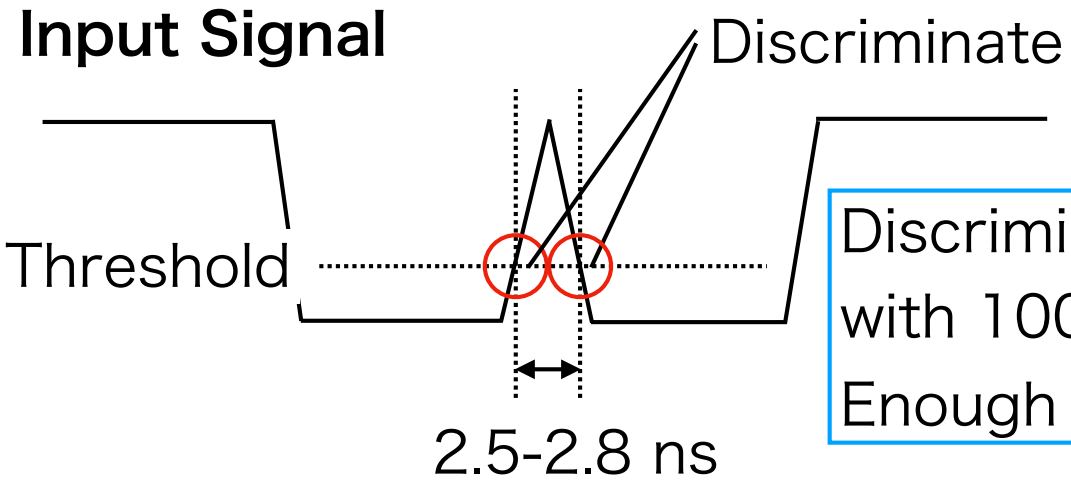
DNL = [-0.022, +0.022] LSB
No bad influence

Minimum Pulse Width



Detect narrow signal (1.0-1.3ns)
with 100% efficiency
Enough to use in the experiment

Double Pulse Separation



Discriminate adjacent 2 signals (2.5-2.8ns)
with 100% efficiency
Enough to use in the experiment

※Those results are limited by test setup