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Development of Front-End Electronics for PandaX-III Prototype TPC

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On behalf of PandaX-III collaboration
14/06/2018

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- Summary

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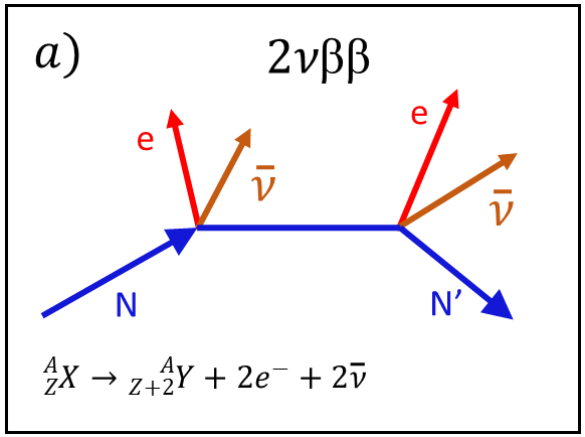
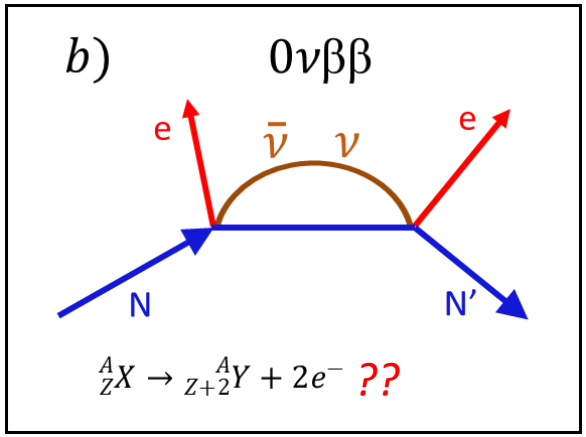
Introduction

- Neutrinoless Double Beta Decay

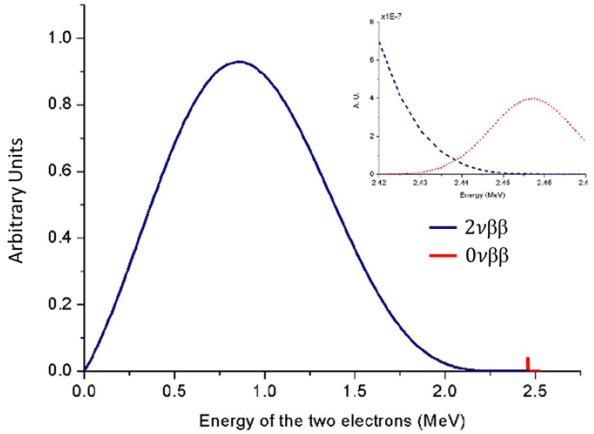


Half-life ≥ 10^{18} y



Half-life ≥ 10^{25} y

- Importance of 0νββ reasearch
  - Majorana neutrino
  - Neutrino mass scale
  - Lepton number violation

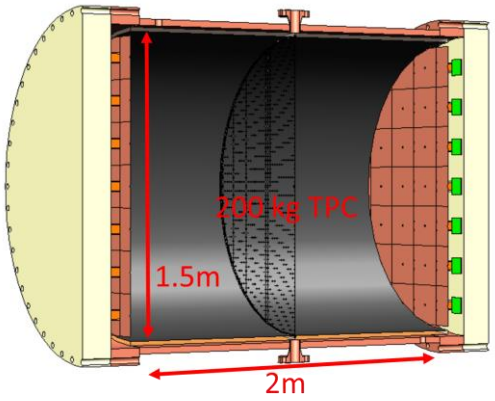


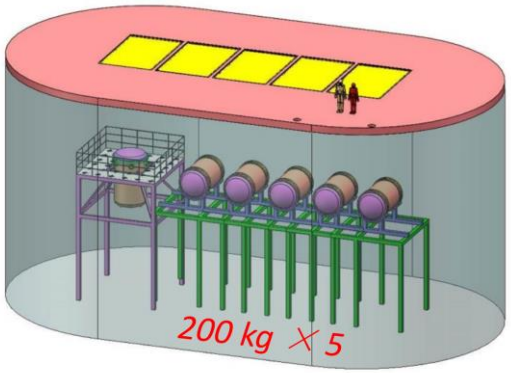
Introduction

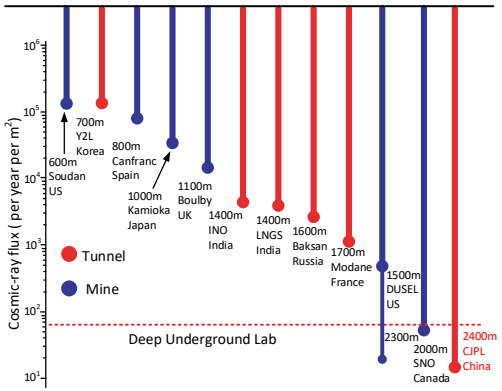
- PandaX-III: the first large scale 0$\nu\beta\beta$ project in China
  - 200 kg high pressure gas TPC for 0$\nu\beta\beta$ of ^{136}Xe

    $^{136}Xe \rightarrow {}^{136}Ba + 2e^{-} + (2\nu_e)$

    - $Q_{\beta\beta}$ (^{136}Xe) ~2.46MeV
- Proposed in 2015
  - SJTU, USTC, PKU…
- Advantages
  - Ultra-low background
  - High energy resolution
  - Large experimental statistics
  - Good background discrimination

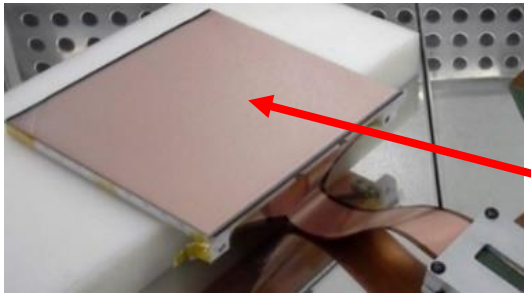


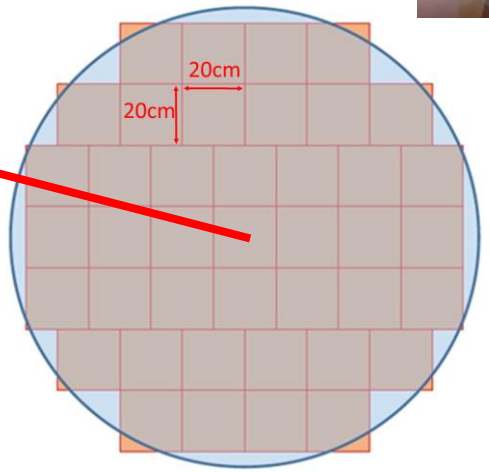


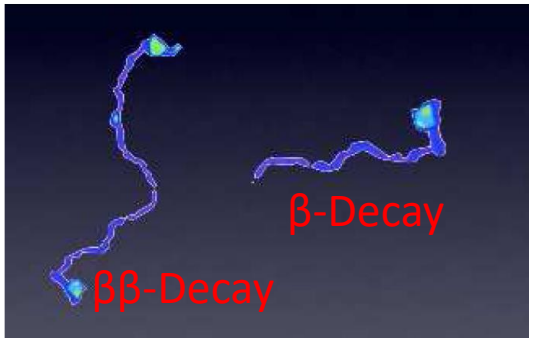


Introduction

- TPC
  - Energy resolution
    - 3% FWHM
  - Position resolution
    - ~3mm





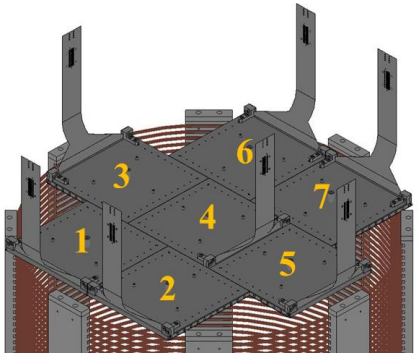


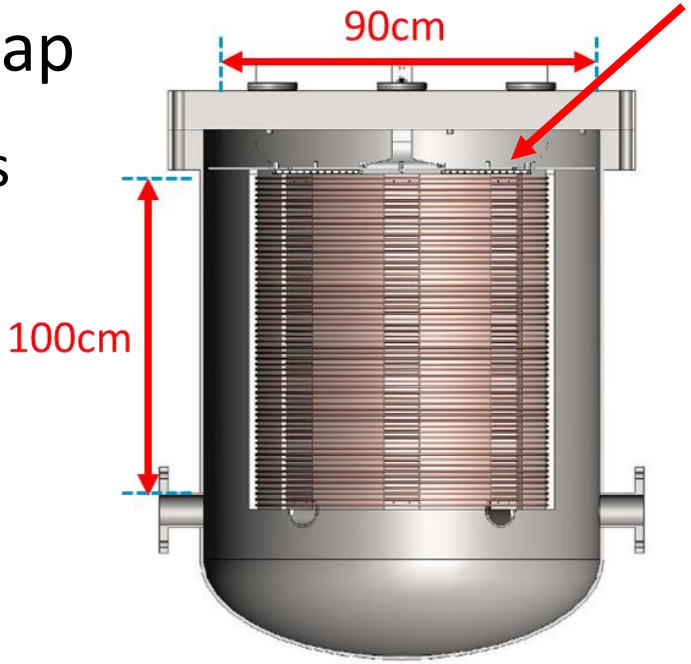
Requirements for Electronics

- Channel Numbers
  - Anode strip signals: 10496
  - Mesh signals: 82
- Event rate: 10 Hz
- Input Range: ≥ 1 pC
- Pulse Width: ≥ 100 μs
- INL: < 3.2%
- Gain Nonuniformity: < 2%
- Noise: < 6 fC

Prototype TPC

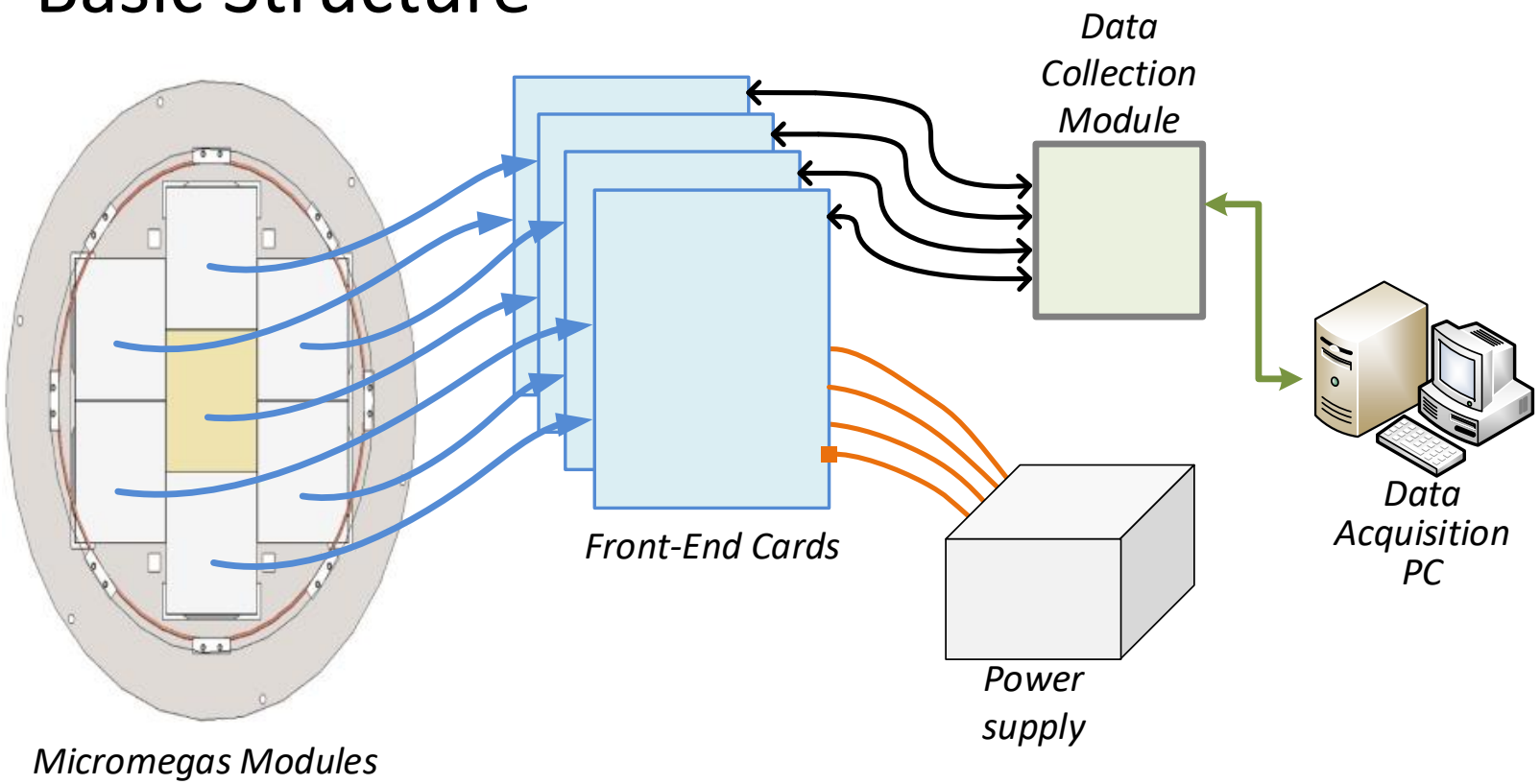
- PandaX-III Prototype TPC
  - 40 kg
  - (-HV) at the bottom
  - 7 Micromegas at the end-cap
    - ➢ 896 anode strips +7 meshs





Readout System

- Basic Structure



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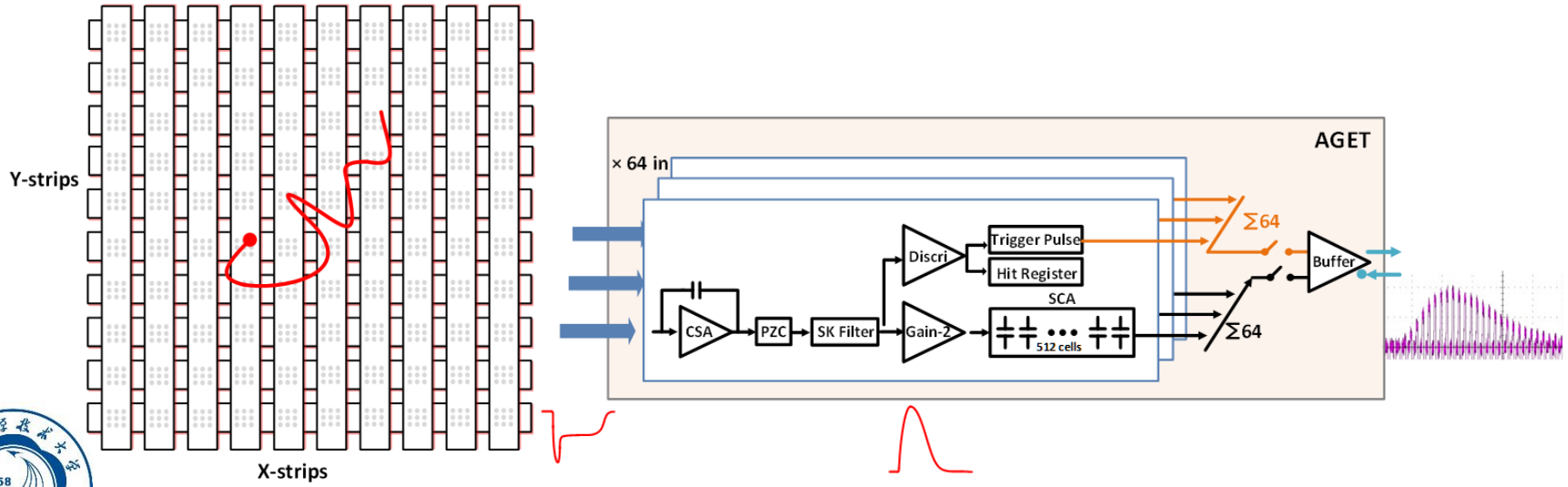
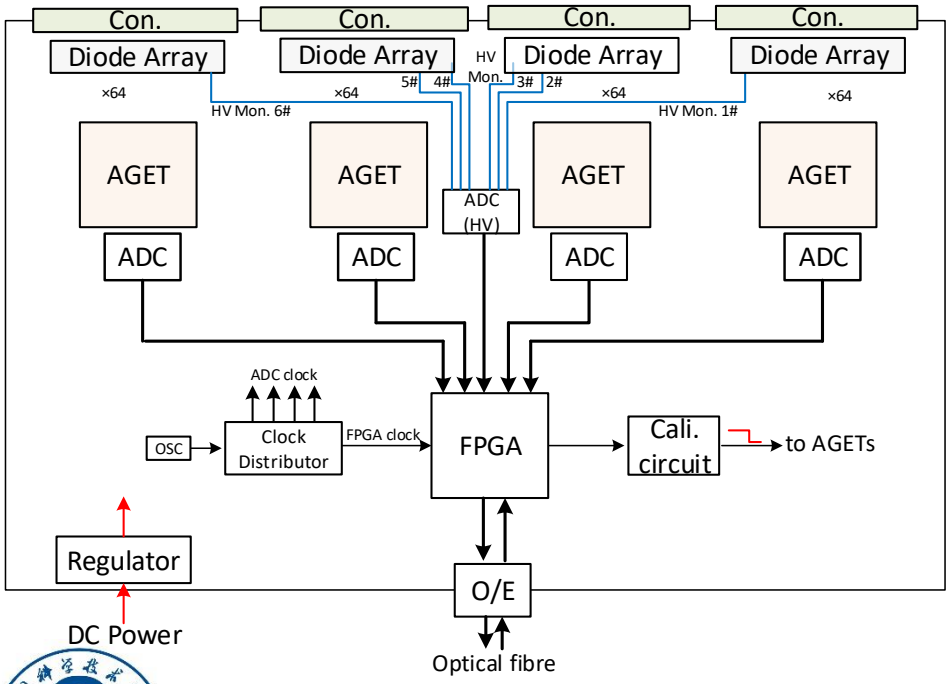
Design of Front-End Electronics

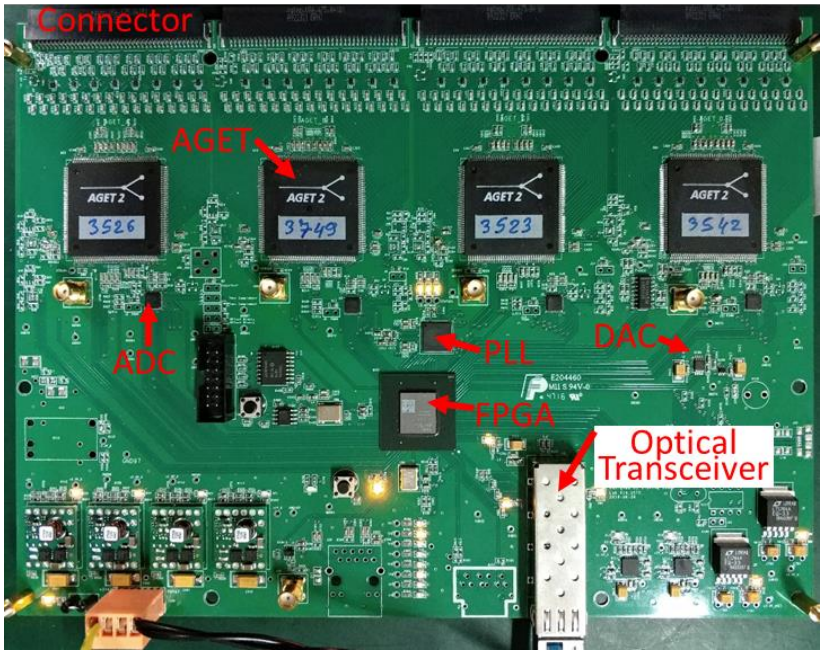
- AGET (ASIC)
  - Number of channels: 64
  - Input range: 120fC, 240fC, 1pC, 10pC
  - Peak time: 50ns - 1μs (16 values)
  - Sampling frequency: 5MHz (1MHz -100MHz)
  - Readout frequency: 20MHz - 25MHz



Design of Front-End Electronics

- Front-end Card (FEC)
  - AGET + ADC+ FPGA
  - Number of channels: 256





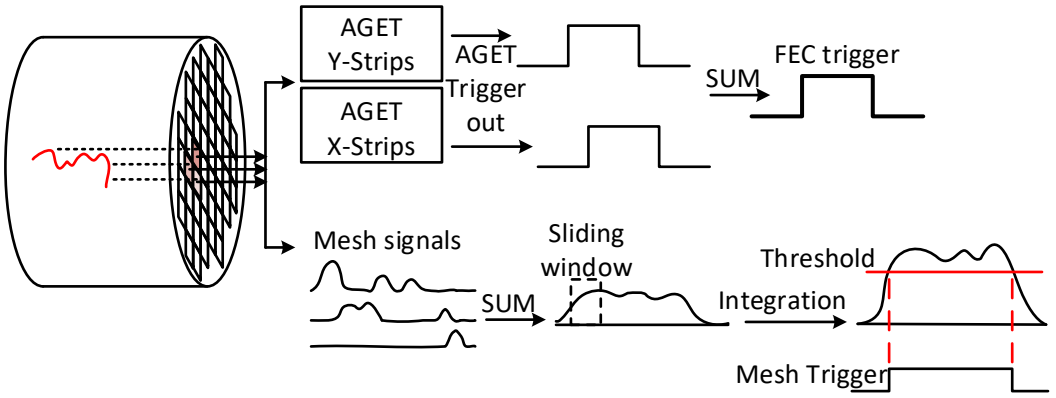
Design of Front-End Electronics

- FPGA(XC7A200T)
  - Logic cells: 215360
  - SRAM: 365
  - GTP: 4

4(AGETs)× 64(channels)× 512(cells)×16(bit) =2.1 Mbit
Event number: 2
Total memory cache: 4.2Mbit

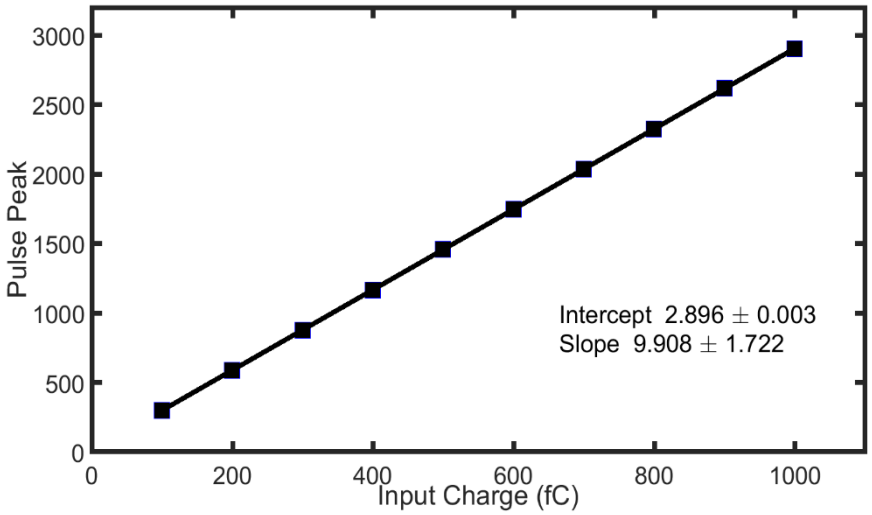
Event rate: 10Hz
Data rate: 21Mbps

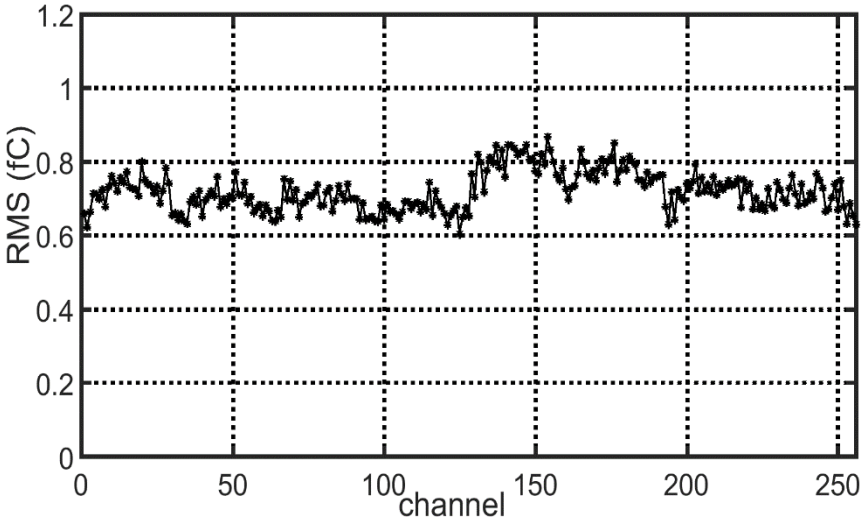
- Calibration circuit
- System trigger
  - Generated by FEC AGET
  - Generate by Mesh signal



Performance Tests

- Condition: 1 pC input range, 1 μs peaking time
  - RMS noise < 0.9 fC
  - INL < 1%

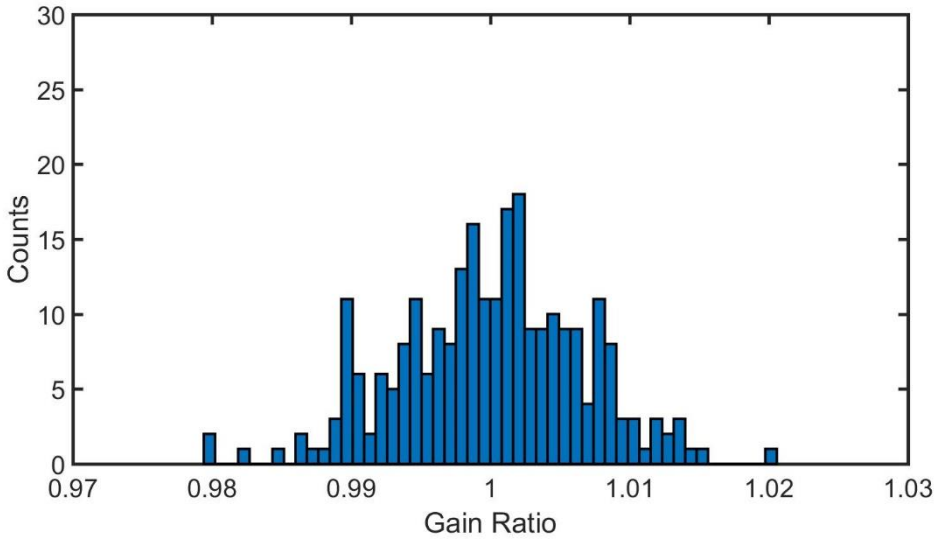


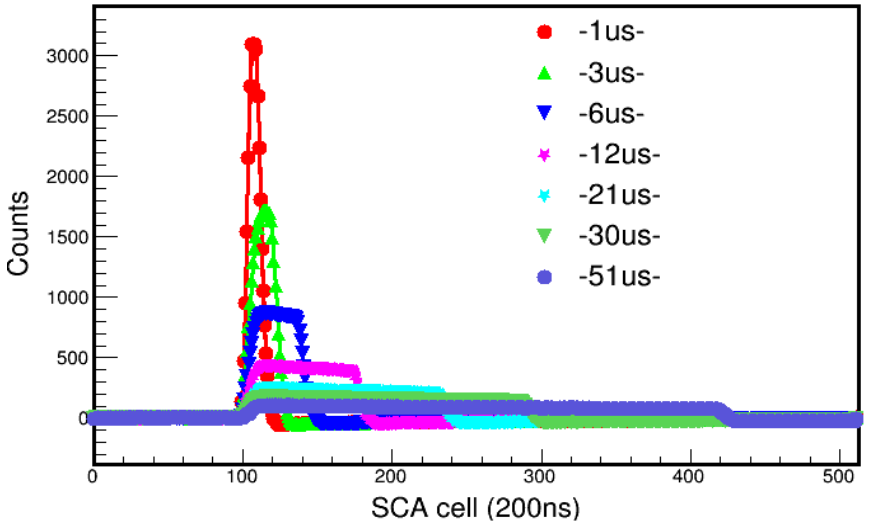


meet the requirements

Performance Tests

- Condition: 1 pC input range, 1 μs peaking time
  - Gain Nonuniformity : ~0.67%
  - Wide Pulse

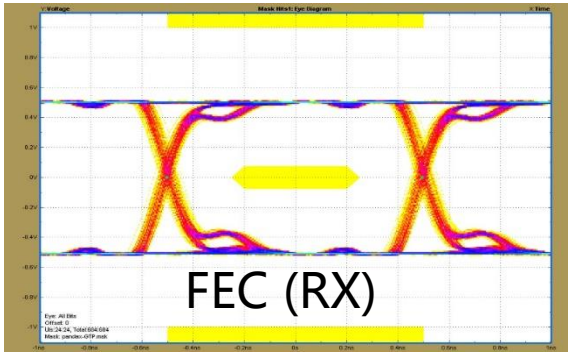


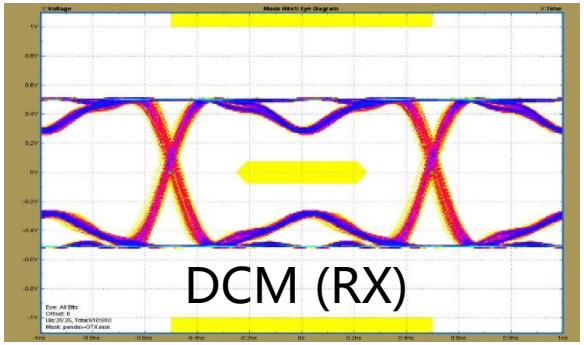


meet the requirements

Performance Tests

- Reliability test of optical link
  - OSC ibert test
  - Bit error test (PRBS7)





Receiver	Transmission	Test time	Test Bit Num	Bit Err Num	Bit error rate (90% Confidence)
FEC	DCM	24h	7×10^{13}	0	$< 3.2\times10^{-14}$
DCM	FEC	24h	7×10^{13}	0	$< 3.2\times10^{-14}$

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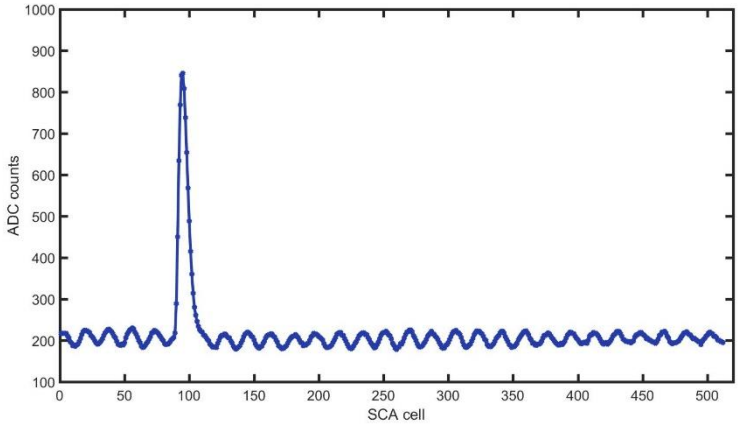
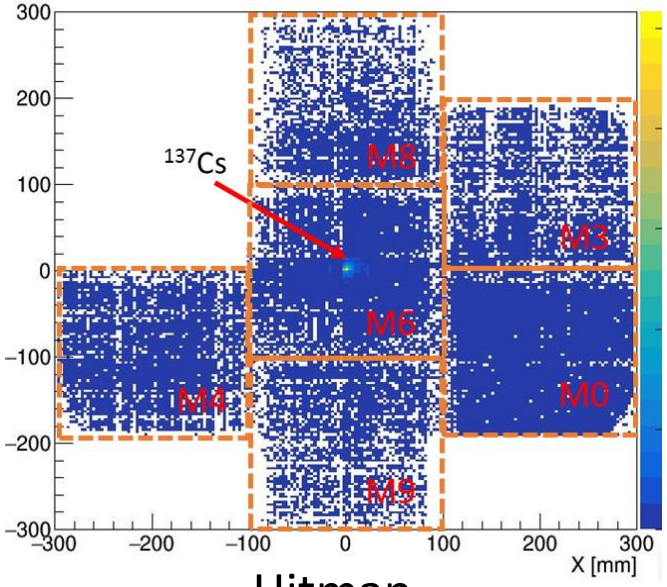
Joint-test



Waveform



Hitmap

Ar, 98.5%

C_4H_{10}, 1.5%

Scene

Contents

Summary

- Summary
  - The performances of FECs meet the requirements of the PandaX-III experiment
  - The FECs with 1024 readout channels work well during the joint-test with prototype TPC
- Next Plan
  - More joint-tests are in progress
  - Engineering design of FEC will be carried out soon

Thanks !