EUROfusion

21st IEEE Real Time Conference -15 June 2018
Colonial Williamsburg, U.S.A

OpenCL implementation of an adaptive disruption predictor based on a probabilistic Venn classifier

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** See the Appendix of F. Romanelli et al., Proceedings of the 25th IAEA Fusion Energy Conference 2014, Saint Petersburg, Russia*

ABSTRACT

The ability and flexibility of the Open Computing Language (OpenCL) for task parallelization in heterogeneous computing platforms (FPGA, CPU, GPU) represent a remarkable advantage when designing advanced data acquisition and processing systems. This work shows a specific implementation of an adaptive probabilistic disruption predictor for a fusion device, tested with signals obtained from JET database. This implementation uses OpenCL as base technology for the design cycle. The system was realized using an FPGA-based architecture that comprises a Cyclone V and a GPU-based architecture that contains an AMDFireProW4300 inserted into a computer running Scientific Linux as Operating System. This contribution presents the methodology, the hardware/software system architecture, and the implementation results in both hardware platforms. The work is focused on the critical aspects involved in the design of these intelligent data acquisition and processing systems with OpenCL. When dealing with this technology, it is essential to be aware of aspects such as the significant differences in the design flow concept between FPGA and GPU implementations, or how to select the part of the algorithm that is better to be executed in each platform, which is not an easy task. The test results show that it is possible to achieve prediction times shorter than 500 us.

(1) ADC CONTROLLER DESIGN

Design of the hardware for controlling the DAQ device, responsible for sending the signals samples to the FPGA-based processing hardware.

[VHDL/Verilog, Quartus II design cycle]

ADAPTIVE DISRUPTION PREDICTOR

OBJECTIVES

- Implementation of an adaptive probabilistic predictor from scratch based on Venn prediction using an OpenCL-design-based advance data acquisition system
- Performance evaluation of the implementation in a OpenCL FPGA/GPU-based data acquisition system

MACHINE LEARNING ALGORITHM

1. Operation start
2. Signal data acquisition and storage
3. Wait for first occurrence of a disruptive and non-disruptive discharges.
4. First model generation
   i. Signals Parameterizing
   ii. Signal normalization
   iii. Feature vector calculation(disruptive and non disruptive)
5. Wait for a new discharge
6. Real-Time prediction with last calculated model in less than 1ms.
7. Signal data acquisition and storage
8. If missed alarm new model generation
   i. New signals parameterizing
   ii. Signal normalization
   iii. Recalculate FV of the current model
   iv. Add disruptive FV to a new model
   v. Add non-disruptive FV to a new model
9. Repeat steps 5 to 8 until the end of the experiment

SIGNALS (JET)

Three Signals sampled at 1KS/s:

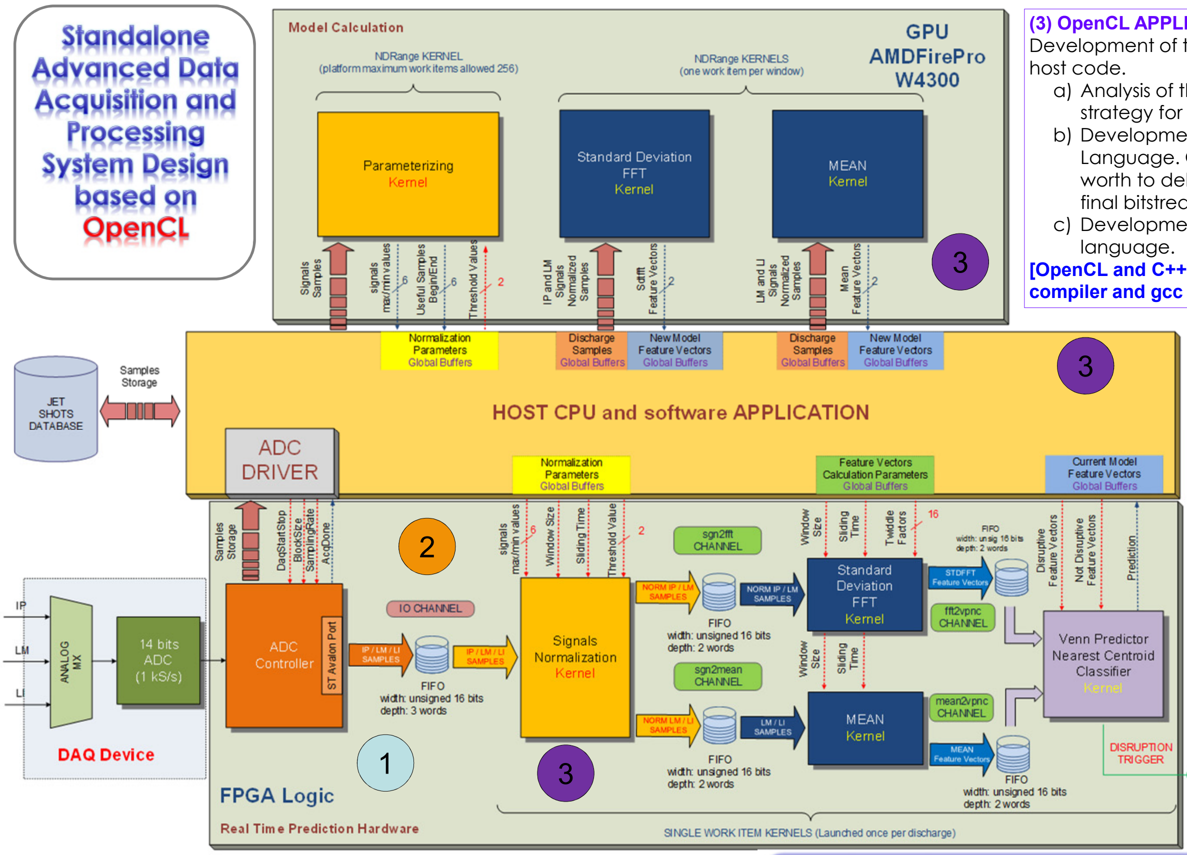
- Plasma current (Ip)
- Locked mode (LM)
- Plasma internal inductance (LI)

FEATURE VECTORS

Four Feature vectors for the Venn Predictor, using a 32 samples window:

- Standard Deviation of the FFT frequency Components for Ip and LM signals
- Mean value for LM and LI signals

Standalone Advanced Data Acquisition and Processing System Design based on OpenCL



(3) OpenCL APPLICATION DEVELOPMENT

Development of the OpenCL kernels code and the C++ host code.

a) Analysis of the processing algorithm and the strategy for the optimal tasks parallelization.
b) Development of Kernels code in OpenCL Language. Compilation is a slow process and it is worth to debug in emulator before generating the final bitstream for the FPGA
c) Development of the Host application code in c++ language.

[OpenCL and C++ design cycle, Intel OpenCL offline compiler and gcc compiler]

(2) OPENCL BOARD SUPPORT PACKAGE GENERATION

Porting your specific FPGA choice reference design of an OpenCL compliant BSP to include your new acquisition hardware

a) Modify the reference design that includes OpenCL-specific components, host-to-FPGA communication IP and Memory IP, to incorporate the Streaming Channels to your specific hardware and the new acquisition hardware.
b) Perform the timing closure and location of the LogicLock region of the design partition for the non-kernel logic.
c) Create the XML files that informs the OpenCL compiler about your custom hardware

[Quartus II and Platform Designer design cycle]

RESULTS

MODEL CALCULATION TIME (* Floating Point Implementation)

Implemented on	Signals Parameterizing	Feature Vectors Calculation
CPU(C++)	0.470 s (per discharge)	1.702 s (per discharge)
GPU*	**0.362 s (per discharge)**	**0.270 s (per discharge)**

FPGA RESOURCES

Logic	81% (25867 LE)
Mem	21% (866K Blocks)
DSP	98% (85 Blocks)

32 SAMPLES WINDOW PREDICTION TIME
** Fixed Point Implementation

Version	max	min	avg	S.D	Time increment per vector
CPU(C++)	251 μs	149 μs	170 μs	31 μs	30 μs
FPGA**	**421 μs**	**382 μs**	**403 μs**	**15 μs**	**1 μs**

CONCLUSIONS

- **Prediction time below 500us in a Cyclone V FPGA, with a highly deterministic behavior (15us) and almost independent of the model complexity (1us per additional disruptive or non-disruptive vector)**
- **Floating-Point (GPU,CPU) and Fixed-Point (Cyclone V FPGA) implementations**
- **Full design cycle deployment, custom hardware, and OpenCL BSP generation included**
- **Fully heterogeneous example CPU (C++) and GPU-FPGA (OpenCL)**

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ACKNOWLEDGMENTS

This work was partially funded by the Spanish Ministry of Economy and Competitiveness under the ENE2015-64914-C3-3-R, ENE2015-64914-C3-1-R, and ENE2015-64914-C3-2-R. This work was supported by EURATOM and carried out within the framework of the European Fusion Development Agreement. The views and opinions expressed herein do not necessarily reflect those of the European Commission.

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This work has been carried out within the framework of the EUROfusion Consortium and has received funding from the Euratom research and training programme 2014-2018 under grant agreement No 633053. The views and opinions expressed herein do not necessarily reflect those of the European Commission.