**A Dual-Channel Low-Power VCSEL Driver ASIC for High-energy Physics Experiments**

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**LOCld65 Design**

The LOCld65 has two separate channels with the same structure and a shared slow control digital part. The design goal is for each channel to amplify a differential signal of greater than or equal to 100 mV (peak-peak) into an 8-mA modulation current for a VCSEL. It consists of two 50-Ω termination resistors, a continuous-time equalizer (CTLE), four stages of limiting amplifiers (LAs), a high-current output driver, and a bias-current generator. The peaking strength of each part in the channel is programmable through an I2C interface.

**Package of LOCld65**

The die of LOCld65 is 1 mm x 1 mm and it packaged in a 24-pin 0.4-mm-pitch QFN package. Each packaged chip is 4 mm (long) x 4 mm (wide) x 1 mm (height).

**Test Vehicle**

Each module is 44.5 mm long, 18.2 mm wide, 5.8 mm high.

The electrical connector is the standard_lb8 connector.

The module supports both panel and board mounting.

We use two TOSAs from TrueLight (Part# TTF-1F59-427).

**Test Results**

A pseudorandom Binary Sequence (2^21-1) was generated in a pattern generator (Picoscope Pulse Model # SDG 12070).

The differential signals were attenuated through a pair of 10-dB attenuators.

The signals were fed to the MTx+ through a pair of coaxial cables.

The output of MTx+ was sent to a sampling oscilloscope (Tektronix Model Number TDS 8000B) with an optical module BOO8BC to observe eye diagrams.

The pattern generator also provided the trigger signal for the oscilloscope.

A power supply provides 1.2 V and 3.3 V for MTx+.

The rise time and the fall time are 29 ps and 38 ps, respectively.

The voltage to provide the bias current of the VCSEL can be decreased as down to 2.0 V at 10 Gbps and 2.1 V at 14 Gbps, respectively, leaving a voltage headroom as high as 1.3 V.

The maximum x-ray energy is 160 keV.

During the test, only LOCld65 was exposed to x-rays, whilst the other parts of the board were protected.

During and after the test, no significant degradation was observed in eye diagram performances, including optical modulation amplitude, average optical power, rise time, fall time, and RMS jitter.

No significant change in 3.3 V power current.

The power current change of 1.2 V was less than 20%.

Single event upset test will be conducted in the future.