A Dual-Channel Low-Power VCSEL Driver ASIC for High-energy Physics Experiments

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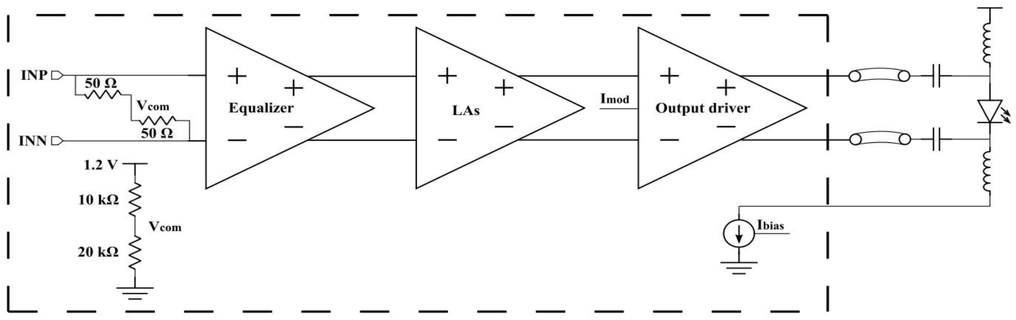
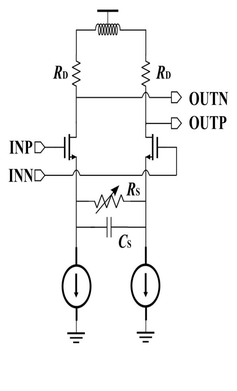


a) The diagram of LOCId65 channel

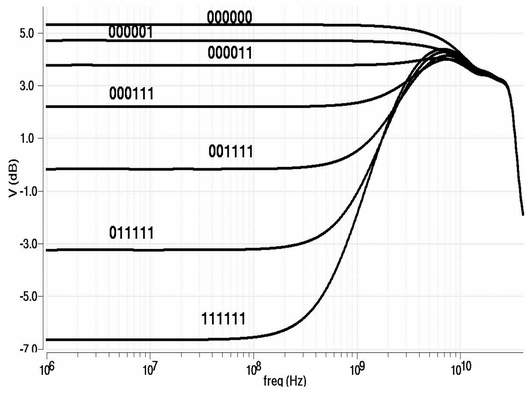
LOCId65 Design

The LOCId65 has two separate channels with the same structure and a shared slow control digital part. The design goal is for each channel to amplify a differential signal of greater than or equal to 100 mV (peak-peak) into an 8-mA modulation current for a VCSEL.

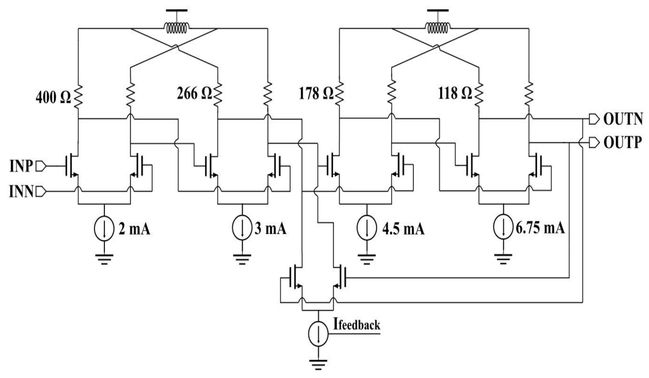
It consists of two 50-Ω termination resistors, a continuous-time equalizer (CTLE), four stages of limiting amplifiers (LAs), a high-current output driver, and a bias-current generator. The peaking strength of the each part in the channel is programmable through an I²C interface.



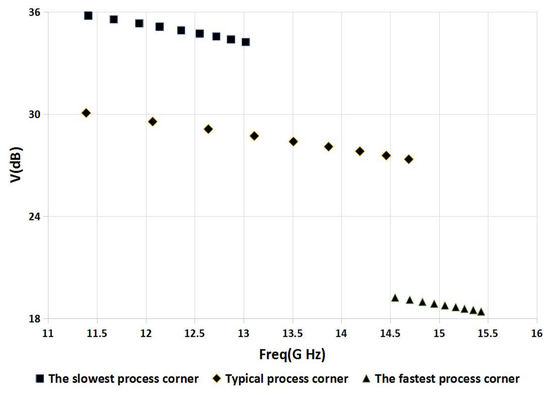
b) The structure of equalizer



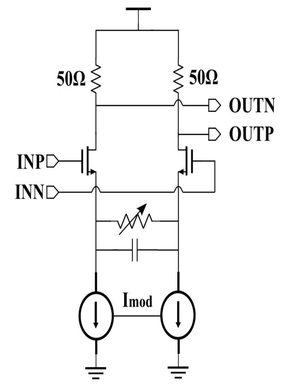
c) The amplitude-frequency response curves under different resistance value settings



d) The structure of LAs



e) The amplitude-frequency response curves under different feedback current settings and in the different process variations



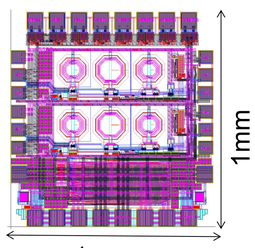
e) The structure of output driver

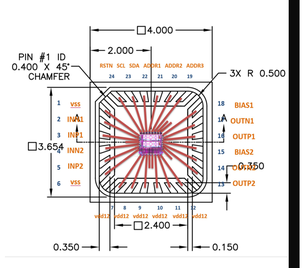
The output driver has a pre-emphasis option to improve the output signal bandwidth above 10 GHz in all process corners.

Equalizer in LOCId65 compensates the high-frequency signal loss due to the transmission line and the ESD diode. Fig c) shows the amplitude-frequency response curves under the different R_S .

We use a four pre-drive stages to amplify signal amplitude to 800 mV (peak-peak). Every two-stage amplifier shares a peaking inductor to save the chip area. A current adjustable active feedback cell is used to adjust the gain and bandwidth of LAs.

Package of LOCId65

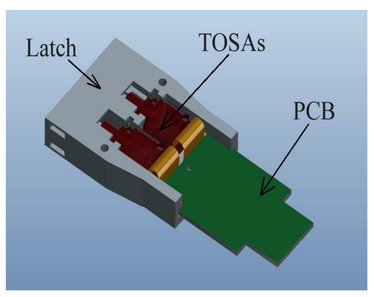




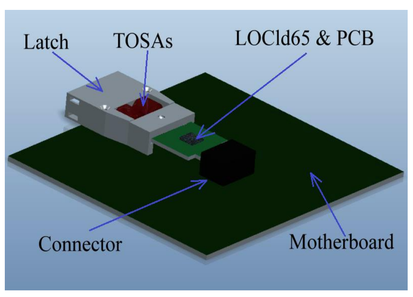
The die of LOCId65 is 1 mm x 1 mm and it packaged in a 24-pin 0.4-mm-pitch QFN package.

Each packaged chip is 4 mm (long) x 4 mm (wide) x 1 mm (height).

Test Vehicle



a) Bottom view of an MTx+ module with an optical latch and two TOSAs



b) Top view of an MTx+ module mounted on a motherboard

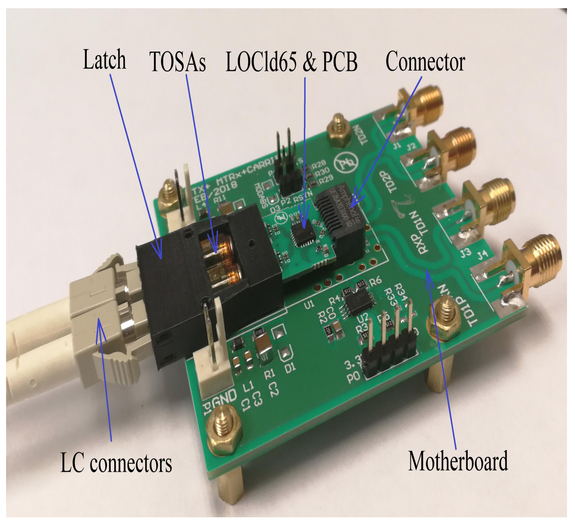
Each module is 44.5 mm long, 18.2 mm wide, 5.8 mm high.

The electrical connector is the standard SFP+ connector.

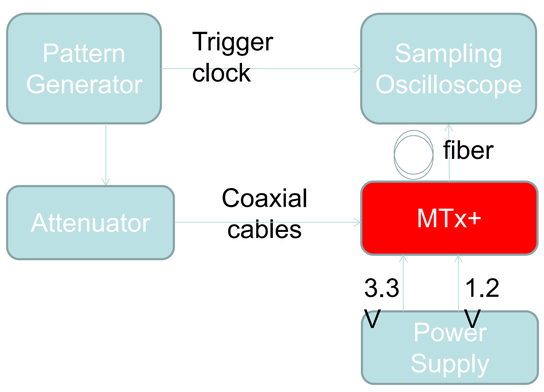
The optical connector is the standard LC connector.

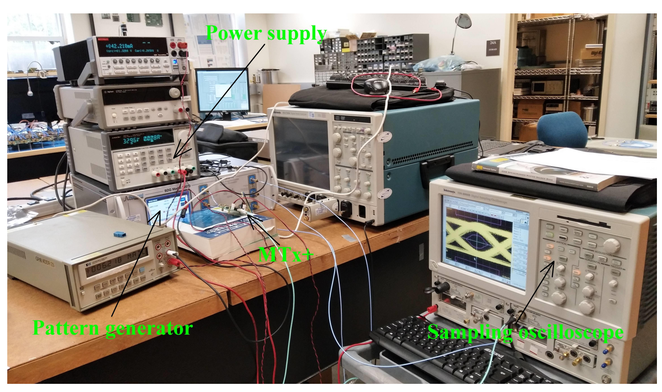
The module supports both panel and board mounting.

We use two TOSAs from Truelight (Part# TTF-1F59-427).

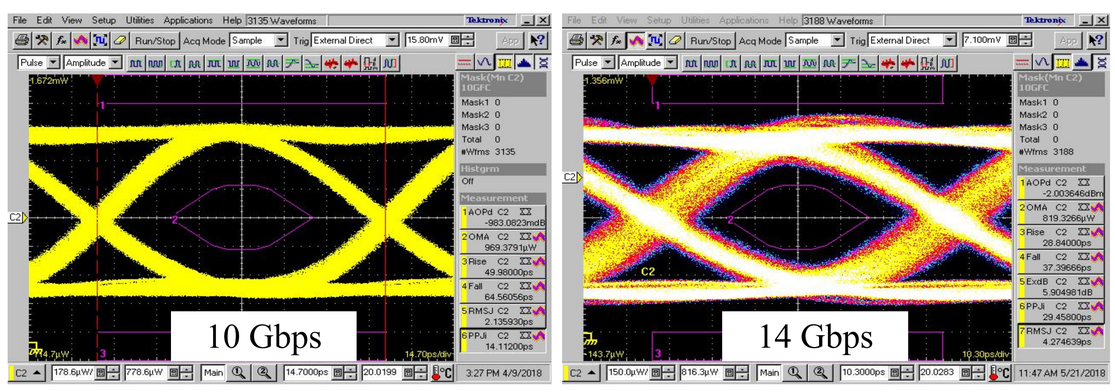


Test Results





a) Block diagram (left) and picture (right) of the test setup



b) Typical eye diagrams at 10 Gbps (left) and 14 Gbps (right)

A pseudorandom Binary Sequence (2^7-1) was generated in a pattern generator (Picosecond Pulse Model # SDG 12070).

The differential signals were attenuated through a pair of 10-dB attenuators.

The signals were fed to the MTx+ through a pair of coaxial cables.

The output of MTx+ was sent to a sampling oscilloscope (Tektronix Model Number TDS 8000B with an optical module 80C08C) to observe eye diagrams.

The pattern generator also provided the trigger signal for the oscilloscope.

A power supply provides 1.2 V and 3.3 V for MTx+.

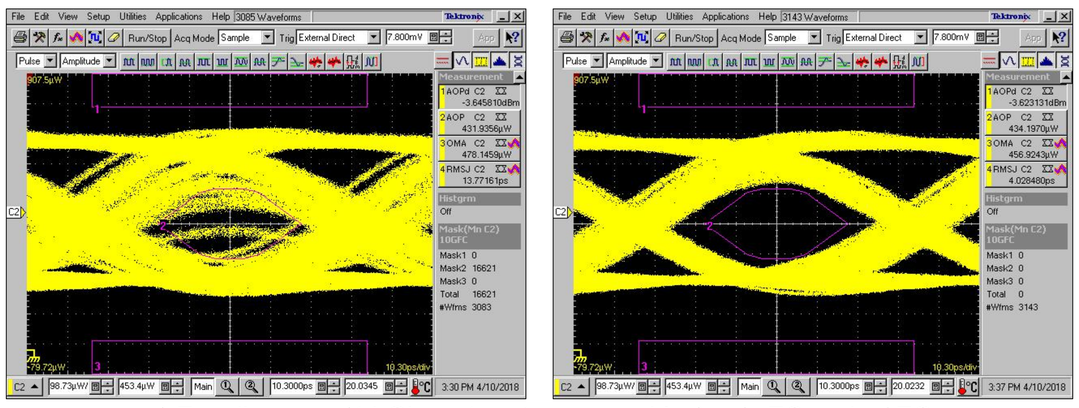
Four prototype chips modules tested and passed 10-Gbps Fiber-Channel eye mask.

The currents of 1.2 V and 3.3 V are 39 mA and 6.3 mA, respectively.

The total power consumption of MTx+ at 14 Gbps is 123 mW, about a quart of the power consumption of MTx.

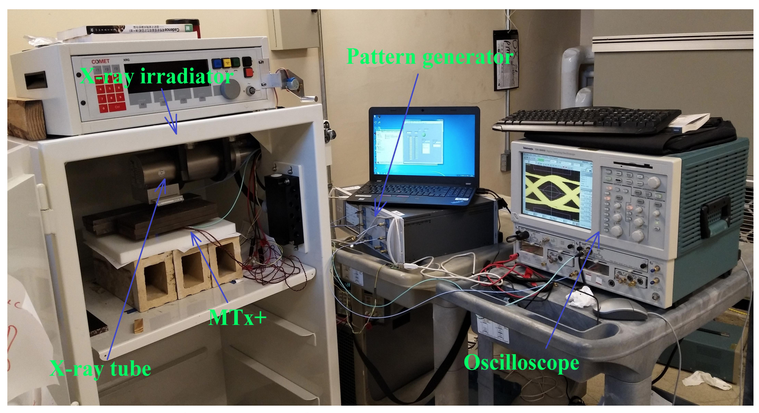
The rise time and the fall time are 29 ps and 38 ps, respectively.

The voltage to provide the bias current of the VCSEL can be decreased as down as 2.0 V at 10 Gbps and 2.1 V at 14 Gbps, respectively, leaving a voltage headroom as high as 1.3 V.



c) Eye diagrams (14 Gbps, 1-meter coax cables), w/o EQ and w/ EQ

The diagrams shown above demonstrate that by adjusting the input equalization strength, the high frequency loss of long cables can be compensated.



d) Picture of the irradiation test setup

A prototype chip survived in x-rays up to 4.9 kGy (SiO2).

The maximum x-ray energy is 160 keV. During the test, only LOCId65 was exposed to x-rays, whilst the other parts of the board were protected.

During and after the test, no significant degradation was observed in eye diagram performances, including optical modulation amplitude, average optical power, rise time, fall time, and RMS jitter.

No significant change in 3.3 V power current. The power current change of 1.2 V was less than 20%.

Single event upset test will be conducted in the future.

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