# Cascading Sensor Network Clock Synchronization Scheme

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## Introduction

For cascading sensor network, which requires that the clock of sensor in the cascading sensor network must be synchronized. However, GPS-based synchronization is not suitable for low-power applications. It is not possible to equip all the sensors with GPS chips for clock synchronization. So in the end, GPS is installed on the sensor management unit(SMU). SMU synchronizes the local clock with the GPS and then uses the broadcast sync frame to synchronize the clock of the lower sensor chain. Since the actual cascaded sensor network has a large amount of data transmission on the uplink from the sensor to the SMU, the transmission delay is not fixed due to the frame buffer mechanism. Therefore, the sync frame can only use the downlink channel from the SMU to the sensor, and the sensor does not respond to sync frames.

## SMU Local Clock Synchronization

SMU through the control of the VCXO voltage control MCU peripheral timer, the use of the timer capture function to count the second pulse interval. Adjust the VCXO voltage by comparing the difference between the count value and 32768000Hz, adjust the frequency to 32.768MHz to achieve local clock frequency synchronization with GPS .Whenever SMU receives a second pulse from GPS, the MCU will generate a synchronization frame. The MCU sends the frame to the FPGA. When the synchronization frame is sent from the FPGA, the FPGA adds the latched value of the time counter to the frame.

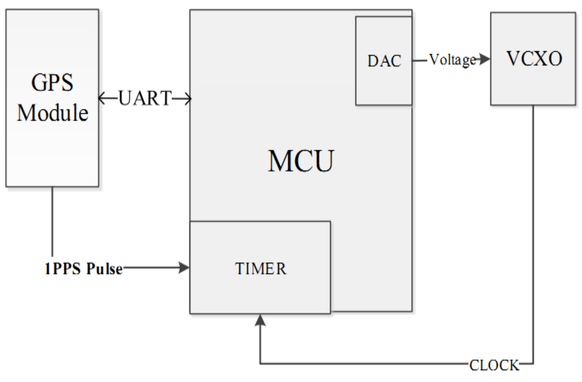


Figure. 1. SMU synchronize local clock with GPS

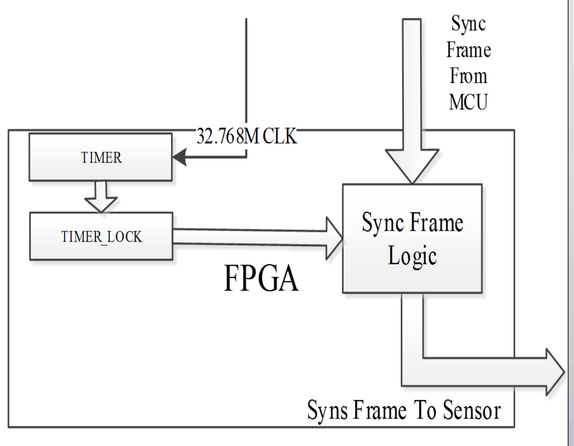


Figure. 2. SMU to generate synchronous frame

## Clock Synchronization of Sensor and SMU

The sensor receives the synchronization frame sent by SMU and does not respond. The sensor changes the SMU count value in the synchronization frame to a local count value, which is then forwarded to the next sensor so that the clock frequency of the entire cascading sensor chain is synchronized, sensor and SMU synchronization process shown in Figure.3. Delay is the transmission delay between two adjacent stations, Offset is deviation between two adjacent units.

The synchronization frame contains the count value of the previous unit when it is sent. When the sensor receives the synchronization frame, the latched local count value can be obtained. Since T2-T1 and T2`-T1` are equal, by adjusting the voltage value of the local VCXO, the sensor realizes that the difference between the local count value and the previous unit count value is the same. Realize the local clock frequency and the previous unit clock frequency synchronization.

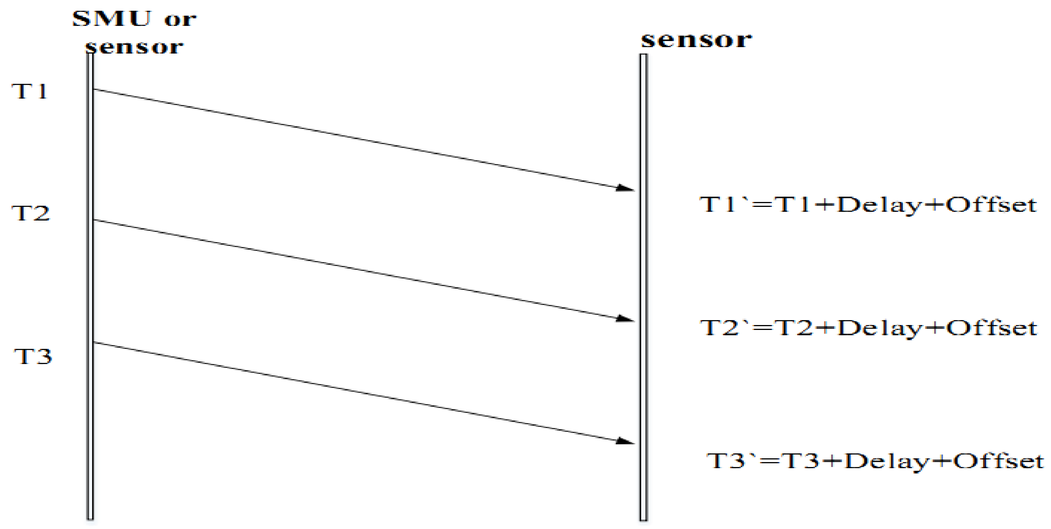


Figure. 3. Clock synchronization of sensor and SMU

## Test

Owing to we only have 20 sensors, the synchronization results of 20 sensors need to be measured, and the results are linearly fitted to infer the synchronization status of the 20th station. Sensor and SMU, sensor and sensor each use a 1-meter cable connection. Sensor outputs the clock after synchronization, the signal input to the frequency meter to measure. Twenty sensors to take interval measurements, measuring 2, 4, 6, 8, 10, 12, 14, 16, 18, 20 ten sensors. Each sensor recorded 600 data to calculate the stability and center frequency of the clock.

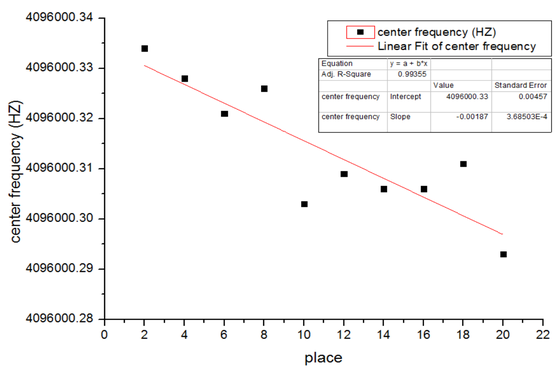


Figure. 4. Clock center frequency fitting results

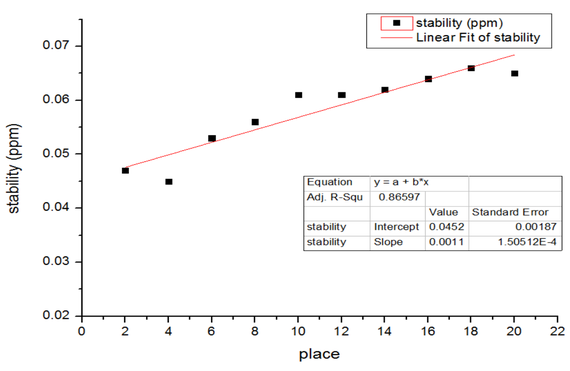


Figure. 5. Clock frequency stability fitting results

## Conclusion

In this paper, we propose a hybrid clock synchronization architecture to realize the clock synchronization of cascaded sensor networks, which is of practical value for the cascaded links that are suitable for one-way synchronization frames. This scheme achieves the effect that a similar GPS chip is used for clock frequency synchronization in each sensor.