The Phase-1 Upgrade for the Level-1 Muon Barrel Trigger of the ATLAS Experiment at LHC

V. Izzo[1], A. Aloisio[1,2], R. Giordano[1,2], S. Perrella[1,2], R.Vari[3]

[1] INFN Sezione di Napoli, via Cintia, I-80126, Napoli, Italy [2] Dept. Of Physics, via Cintia, I-80126, Napoli, Italy [3] INFN Sezione di Roma1, P.le A. Moro, I-00185, Roma, Italy

1. Introduction

In the Level-1 Muon Barrel trigger system [1] of the ATLAS detector at CERN, three concentric layers of Resistive Plate Chambers (RPC) are used in order to detect muons (Fig.1, left). Starting from the hits on the RPCs, the on-detector electronics triggers muons with specific programmable values of transverse momentum (p_T) and tags the candidate tracks with the corresponding Bunch Crossing identifier (BCID). The algorithm looks for hit coincidences within different detector layers inside a programmed geometrical road, which defines the transverse momentum cut. The trigger is composed of the low-p_T and the high-p_T systems, which apply different selection schemes (Fig.1, right). Trigger data is then transferred from on-detector to the off-detector trigger electronics boards via optical link.

The Level-1 Muon Barrel in segmented in 64 trigger sectors, following the eightfold structure of the detector. For each trigger sector, a Barrel Sector Logic (SL) board, installed in a counting room, collects the RPC trigger data, completes the trigger algorithm and transfers the trigger candidates to the Muon to CTP Interface (MuCTPI) board.

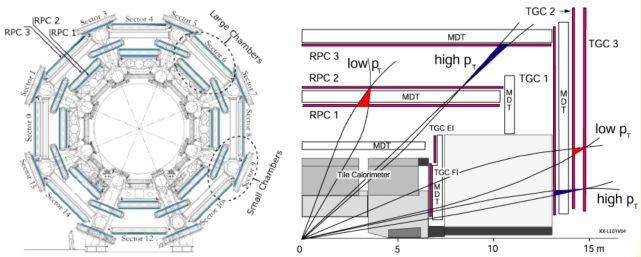

Fig.1 The ATLAS Barrel region section on the azimuthal plane, with the three concentric RPC detectors (left); The low-pT and high-pT trigger scheme, showing the middle-pivot detector (RPC2), the inner low-pT confirm detector (RPC1) and the outer high-pT confirm detector (RPC3) (right)

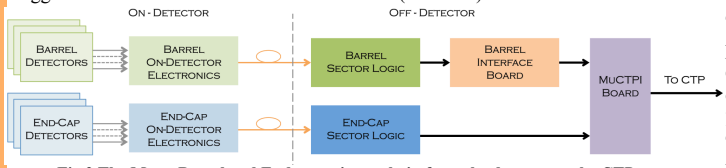

Fig.2 The Muon Barrel and End-cap trigger chain from the detector to the CTP

The MuCTPI combines trigger data from the Barrel and the End-cap region, and provides the combined muon candidate to the Central Trigger Processor (CTP). The challenge of the L1 trigger system is a reduction of the event rate from a collision rate of 40 MHz to an overall acceptance rate of about 100 kHz, with a maximum fixed latency of 2.5μs.

The trigger chain from the muon detectors to the CTP, for the Barrel and End-cap region, is shown in fig.2; an additional module is installed for the Barrel system, the Barrel Interface Board, which is the interface between the Barrel SL and the MuCTPI.

2. Motivation for the Upgrade

Although the system has been performing well for almost a decade, various upgrades for the ATLAS Level-1 trigger system were already deployed, and others are foreseen in the next years, due to the always-increasing LHC luminosity. The main motivation for such upgrades is that the trigger system has to cope with tight requirements on trigger efficiency and to become more selective and sensitive to rare physics events. Most of the trigger upgrades are based on state-of-the-art technologies and allow designing more complex trigger menus, performing topological selections, and supporting new physics studies; new technologies will increase processing power and data transfer bandwidth.

For the Phase-I upgrade of the experiment [2], starting in 2019, one of the upgrades concerns the MuCTPI board. Its full redesign is required in order to provide full-granularity muon information to L1 Calorimeter system, allowing combined calorimeter/muon topological trigger algorithms, and to be able to interface to the Muon SL using high-speed optical links, thus increasing the data transfer bandwidth and the possibility to support new physics studies by processing more than 2 trigger candidates per sector.

3. Implementation

According to the ATLAS Phase-1 upgrade TDR, in order to transfer the Barrel trigger data to the new MuCTPI via optical link, a new version of the VME Barrel Interface Board was designed (fig.3). The new Barrel Interface Board is based on a Xilinx Artix-7 Field Programmable Gate Array device (FPGA) [3] equipped with high-speed embedded transceivers. All the functionalities of the previous Barrel Interface Board will be reproduced; at the same time, the new board will be able to perform more complicated local trigger or monitoring logic, by profiting of the large amount of resources available in the FPGA device.

Moreover, the Barrel Interface Board uses multi-gigabit transceivers, to serialize and optically transmit Level-1 Barrel trigger data to the new MuCTPI, providing a much higher bandwidth than the one available during the first runs of ATLAS; the high-speed optical links will also fulfill the fixed latency requirement for trigger data.

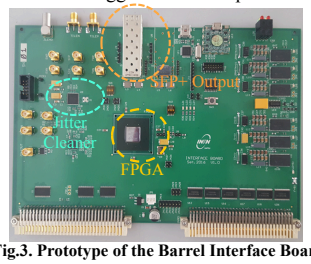

Fig.3. Prototype of the Barrel Interface Board

4. Test Results

The prototype of the Barrel Interface Board has been intensively tested in the lab and resulted to be fully working. The board has been also used in integration tests at CERN with the new MuCTPI board prototype, in order to characterize and validate the optical transmission protocol at 6.4 Gbps, 8B/10B encoded, with fixed latency.

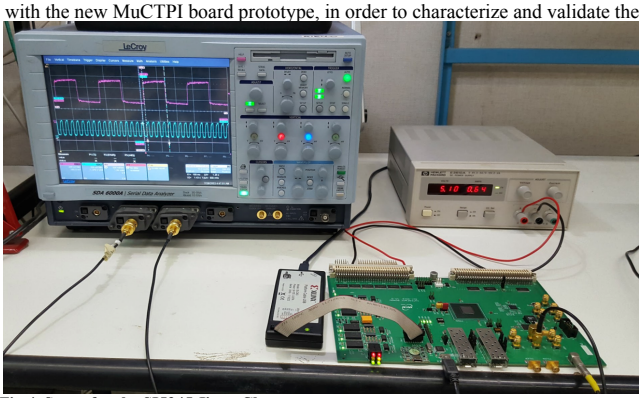

Fig.4. Setup for the SI5345 Jitter Cleaner test

The firmware has been defined and optimized, during the component validation lab tests. Two aspects of the board were verified with a particular care: the Silicon Labs **SI5345 Jitter Cleaner** functionalities and the **6.4 Gb/s data transfer** capabilities.

Fig.4 shows the test setup for the SI5345 Jitter Cleaner, having a 40 MHz input clock and producing a 320 MHz clock, with a constant phase relationship with the input (Zero Delay Mode), to be used by the high-speed transceivers.

The Period Jitter on the output clock signal of the SI5345 was measured to be **~22 ps**; the Cycle-to-Cycle jitter was measured to be **~38 ps**.

Concerning the tests at CERN between the first prototype of the Barrel Interface Board and the MUCTPI prototype, a stable connection was established on optical fibre @6.4 Gbps, and a measurement of the latency between the two modules was performed.

All the results are as expected: Xilinx IBERT tool was used to check the link stability, giving a **Bit Error Ratio better than 10^{-15}**; we used an oscilloscope to measure the transmission latency to be **less than 75 ns**.

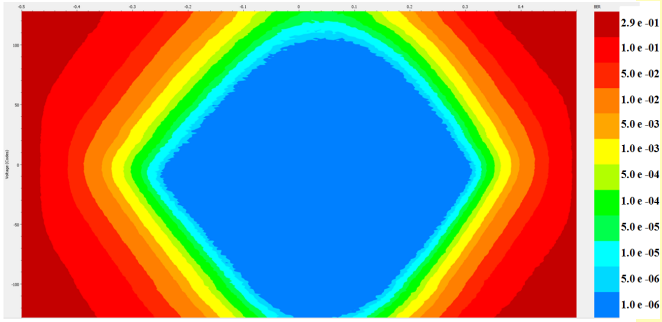

Fig.5. Eye diagram for 6.4 Gb/s transmission on fiber

5. Conclusions

We described the design of the new Barrel Interface Board, to be used to transfer RPC trigger data to the MuCTPI board, for the Phase-I upgrade of the Level-1 Muon Barrel Trigger.

The first prototype of the board was successfully tested and the boards will be produced in 2018.

References

[1] F. Anulli et al., "The Level-1 Trigger Muon Barrel System of the ATLAS experiment at CERN", JINST 4, P04010, 2009

[2] "Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System", 2013

[3] "Xilinx Artix-7 FPGAs Data Sheet", ds181, 2017