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The Phase-1 Upgrade for the Level-1 Muon Barrel Trigger of the ATLAS Experiment at LHC

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The Level-1 Barrel Trigger of the ATLAS Experiment is based on Resistive Plate Chambers (RPC) detectors. The on-detector trigger electronics identifies muons with specific values of transverse momentum (p_T) using of coincidences between different layers of detectors. Trigger data is then transferred from on-detector to the off-detector trigger electronics boards. Data is processed by a complex system, which combines trigger data from the barrel and the endcap regions, and provides the combined muon candidate to the Central Trigger Processor (CTP).

The system performed very well for almost a decade. However, to cope with continuously increasing LHC luminosity and more demanding requirements on trigger efficiency and performance, various upgrades for the full trigger system were already deployed, and others are foreseen in the next years. Most of the trigger upgrades are based on state-of-the-art technologies and allow designing more complex trigger menus, increasing processing power and data transfer bandwidth. Thus, it will be possible to send more trigger candidates, to perform topological selections, and to support new physics studies.

In this paper, we describe the design of the first prototype of the new Barrel Interface Board, designed around a Xilinx FPGA, which transfers RPC trigger data to the CTP system; the board supports the optical transmission of the trigger data with fixed latency and new trigger algorithms. We discuss the design strategies, the hardware implementation and the results of the first functional and integration tests.

Description

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