Real-time Data Flow Control for CBM-TOF Super Module Quality Evaluation

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1. Background

Super module assembled with MRPC detectors is the component unit of Time of Flight (TOF) spectrometer for the Compressed Baryonic Matter (CBM) experiment. Quality of super modules need to be evaluated before it is applied in CBM-TOF. The maximum data rate is up to 6 Gbps at each sandwich TDC station (STS), which is used to digitize time signal exported from super module.

In this paper, a real-time data flow control method for quality evaluation is presented. In this method, data flow is divided into three types, scientific data flow with digitized time information, status data flow and system control data flow. All of the three type data flow should be transmitted orderly.

2. Building model for data flow

The model diagram of data flow is shown in Figure 1. There is three type data flow: scientific data flow, status data flow and control data flow. As is shown in Figure 1, the readout system is the bottleneck in high speed data transmission, which needs to be considered carefully to avoid data jam. Besides, status data of FEE and readout system should be uploaded to status monitor for real-time monitoring. Moreover, control data should be downloaded to FEE and readout system, so that we can control the behavior of specified module according to current status in real time.

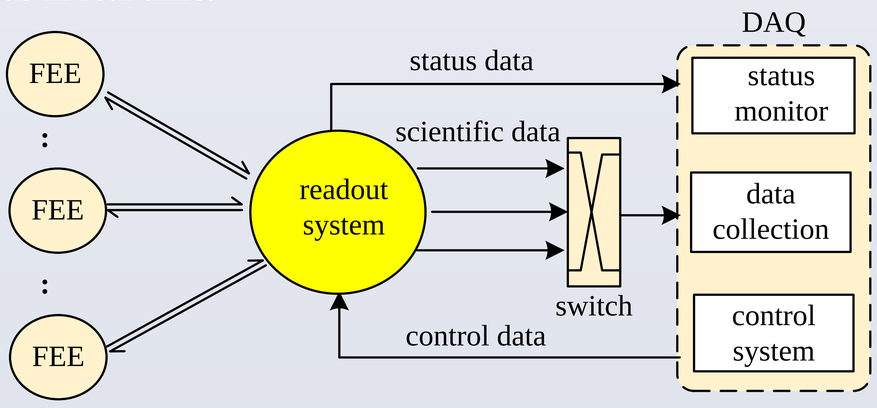

Figure 1 Model of data flow

3. Multi-channel TDC Implementation

According to the model proposed above, the concrete implement of data flow control is shown in Figure 2. It has a good extensive potential when the number of STS increases. To share the pressure of transmitting 6 Gbps data in real time, the control of data flow is designed as a hierarchical and distributed structure based on Gigabit Ethernet. Firstly scientific data as well as status data of each STS is received by 4 master DMBs via optical fibers. Then by logic configuration, scientific data and status data of STS is separated at master DMB and is uploaded in independent physics links thereafter. Each DMB, master or slave, has 2 daughter boards (DRMs) on it. After first stage equipartition between master DMB and slave DMB and second equipartition between DRMs, scientific data is equally distributed to 16 DRMs. Each DRM is expected to support Gigabit Ethernet transmission to DAQ at the rate of 400 Mbps. After separated with scientific data, status data is aggregated into a specialized DMB via crate backplane, and then is uploaded to DAQ. As for control data, it is firstly downloaded from DAQ to the specialized DMB. Then it is fan out to other DMBs via crate backplane and is also sent to STS via optical fiber.

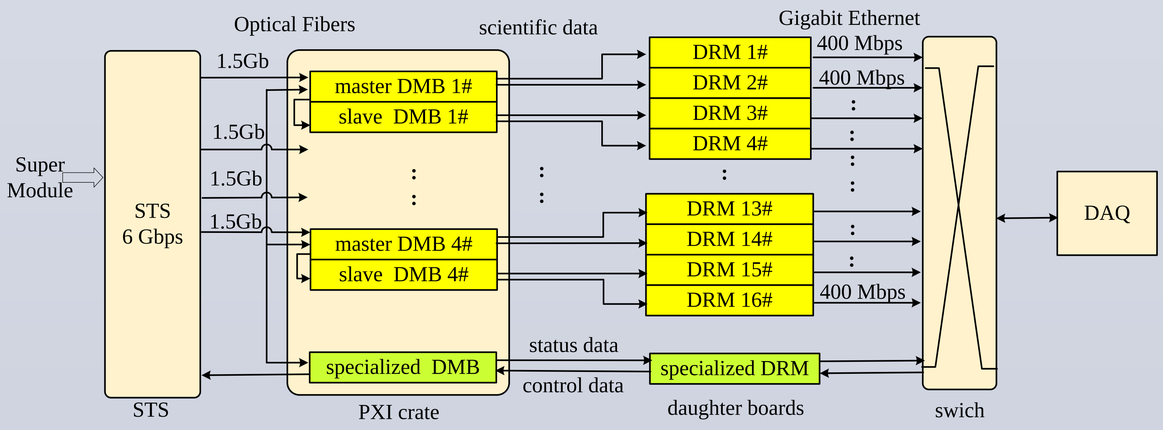

Figure 2 Implement of data flow control

4. Implement of DMB and DRM hardware circuits

DMB and DRM is the hardware support for data flow control. The design structure of DMB and DRM is shown in Figure 3, and corresponding physical photo is shown in figure 4. DMB is designed as a mother board with 2 DRMs on it. There are 4 Gigabit transceiver blocks (GXBs) integrated in DMB FPGA. GXB is used for receiving high speed data from STS and distributing data to 2 DRM and slave DMB. J2 connector is used for communication among DMBs via crate backplane.

DRM is designed to convert FPGA customized protocol data with Ethernet format data and to transmit data to DAQ via Gigabit Ethernet. It is implemented on the basis of SoC FPGA technology which package FPGA and ARM processor in a single die. Embedded Linux software, which runs on hard processor system, can exchange data with PC via Gigabit Ethernet.

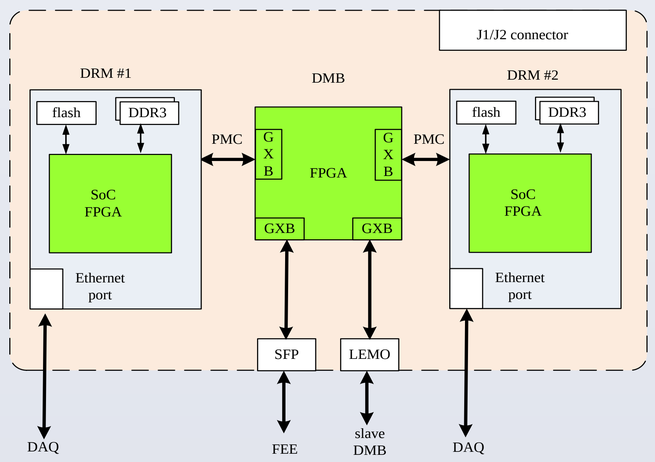

Figure 3 Design structure of DMB and DRM

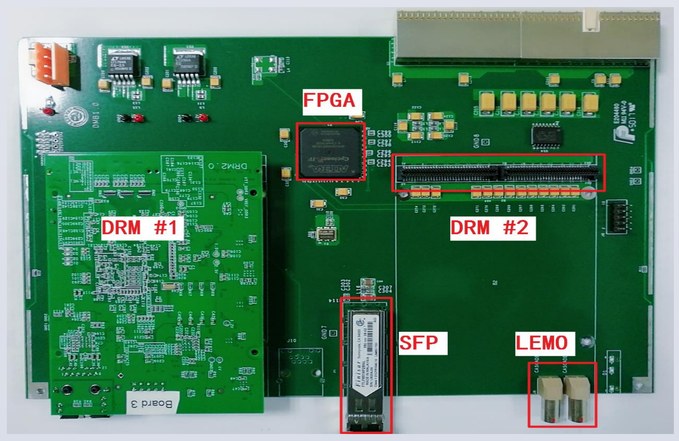

Figure 4 Physical photo of DMB and DRM

5. Conclusion

Preliminary test result indicates that average transmission capability of single DRM reaches 540 Mbps over the expectation of 400 Mbps. This data flow control method can meet the requirement of CBM-TOF supper module quality evaluation.