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## **A new high speed, Ultrascale+ based, board for the ATLAS jet calorimeter trigger system**

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To cope with the enhanced luminosity at the Large Hadron Collider (LHC) in 2021, the ATLAS collaboration is planning a major detector upgrade. As a part of this, the Level 1 trigger based on calorimeter data will be upgraded to exploit the fine granularity readout using a new system of Feature EXtractors (FEX), which each reconstruct different physics objects for the trigger selection.

The jet FEX (jFEX) system is conceived to provide jet identification (including large area jets) and measurements of global variables within a latency budget of less than 400ns. It consists of 6 modules. A single jFEX module is an ATCA board with 4 large FPGAs of the Xilinx Ultrascale+ family, that can digest a total input data rate of ~3.6 Tb/s using up to 120 Multi Gigabit Transceiver (MGT), 24 electrical optical devices, board control and power on the mezzanines to allow flexibility in upgrading controls functions and components without affecting the main board. The 24-layers stack-up was carefully designed to preserve the signal integrity in a very densely populated high speed signal board selecting MEGTRON6 as the most suitable PCB material. This contribution reports on the design challenges and the test results of the jFEX prototypes. In particular the fully assembled final prototype has been tested up to 12.8 Gb/s in house and in integrated tests at CERN. The full jFEX system will be produced by the end of 2018 to allow for installation and commissioning to be completed before LHC restarts in March 2021.

### **Description**

Trigger, board

### **Institute**

CERN

### **Speaker**

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### **Country**

Switzerland

### **Minioral**

Yes

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