A multi-channel digitizer board for the BDX experiment

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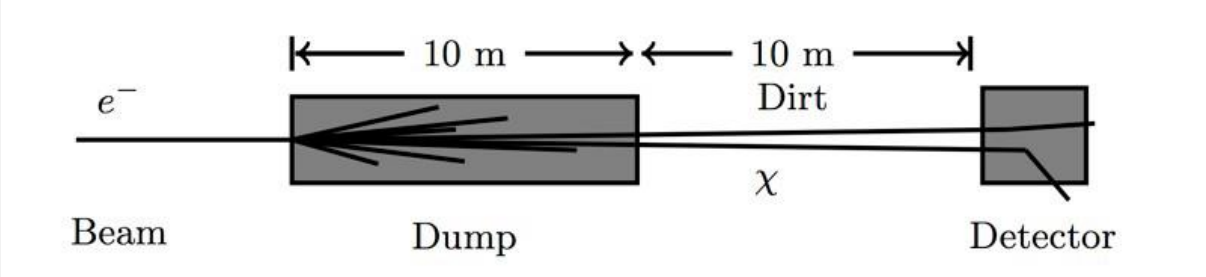
Outline

- BDX experiment
- Board features
- Preliminary results
- Feature work
- Conclusions

Introduction: the Beam Dump eXperiment@JLab

- Beam Dump eXperiment:
  Light Dark Matter (LDM) direct detection
  in a e− beam, fixed−target setup
- χ **production**
  - High−energy, high−intensity e− beam impinging on a dump
  - χ particles pair−produced radiatively, through A' emission
- χ **detection**
  - Detector placed behind the dump, ~20m
  - Neutral−current χ scattering on atomic e− through A' exchange, recoil releasing visible energy
  - Signal: high−energy EM shower, E > .3 GeV



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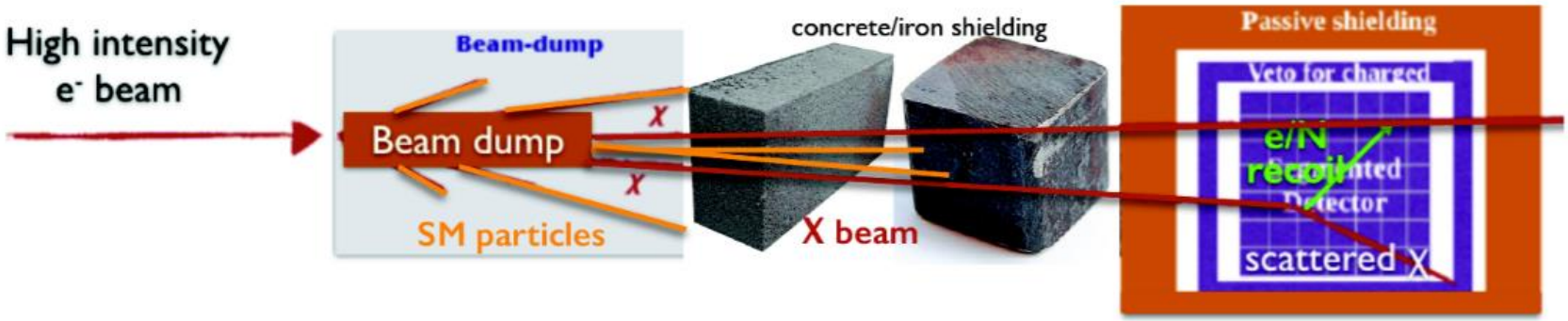

The experiment is designed with two goals:

Producing and detecting LDM

- High-intensity e^- beam, $\simeq 10^{22}$ electrons-on-target (EOT)/year
- Medium-high energy, >10 GeV
- $\simeq 1\ m^3$ (1-5 tons) detector
- EM-showers detection capability

Reducing background

- Passive shielding between beam-dump and detector to filter beam-related backgrounds (except νs)
- Passive shielding and active vetos surrounding the active volume to reduce and identify cosmogenic backgrounds
- Segmented detector for background discrimination based on event topology
- Good time resolution to perform detector-veto coincidence

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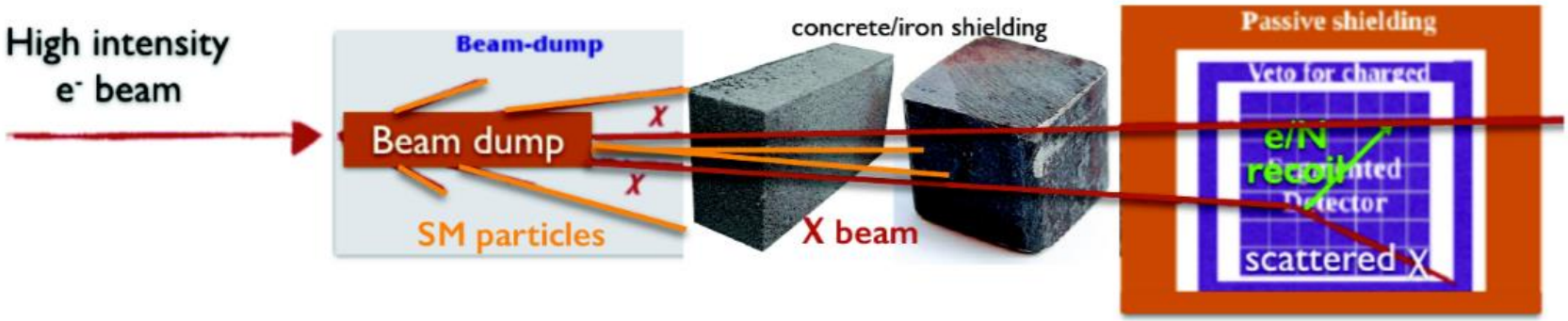

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Detector is an EM calorimeter based on CsI (Tl) crystals read by SiPM

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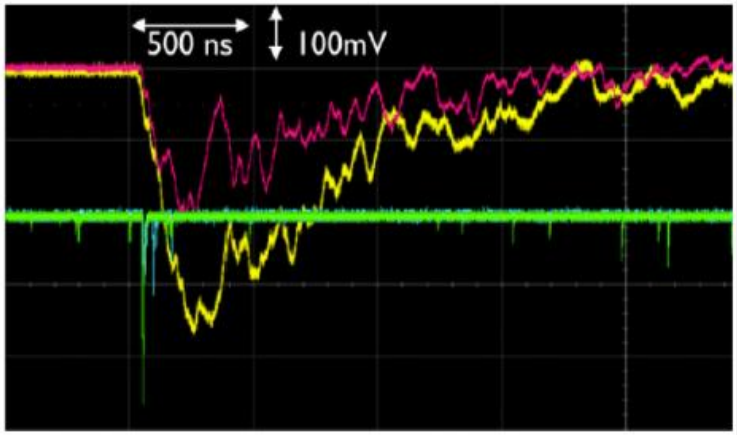
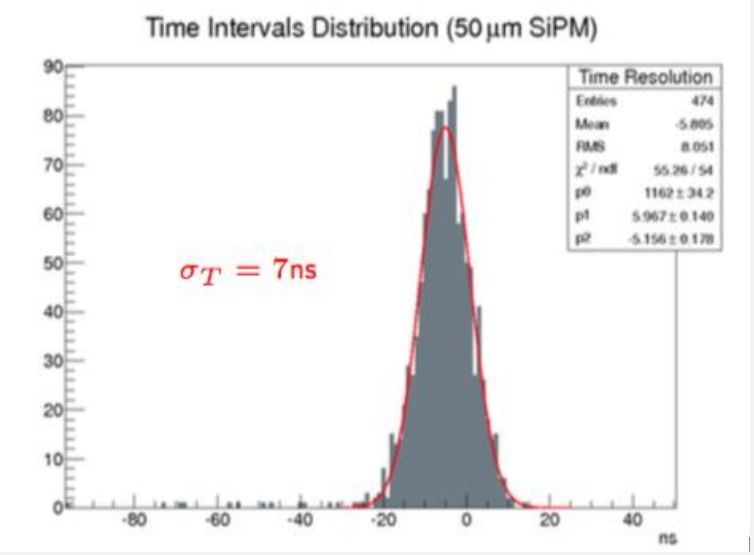
BDX Calorimeter R&D: CsI (Tl) + SiPM

A testbench was setup to measure CsI(Tl) crystal + SiPM properties

- **Setup:**
  - Cosmic-ray coincidence with two plastic scintillator counters read by PMT
  - Trigger given by two PMTs coincidence
  - CsI(Tl) crystal with 25-μm, 6x6 mm^2 SiPM readout.
  - FEE as foreseen in the final detector (ad hoc trans-impedance amplifier)
- **Results:**
  - Light-yield with SiPM readout: ≈ 1 phe / MeV / mm^2 (1 μs integration)
  - Time resolution @ 30 MeV: σ_T = 7 ns
- Results were later confirmed with measurements from BDX detector prototype: **CsI(Tl)+SiPM readout is the optimal choice for the BDX experiment**





BDX requirements

- Light Yield of searched events is high
  - ~5 phe threshold
  - SiPM noise is cutout (~1phe @ 1 MHz)
  - hit amplitude is O(100 mV)
- Hit timing properties:
  - duration: O(10 μs)
  - bandwidth: O(10 MHz)
  - rate @ 5 phe threshold: O(10 Hz)

From front-end to DAQ

- Architecture and front-end inherited from KM3NeT experiment:
  - FastADC sampling (250MHz)
  - Trigger-less front-end system:
    - front end applies only zero-suppression trigger
    - sampling window is time-variable
    - all non-zero data forwarded (streaming-like data flow)
  - Scalable Event Building architecture (scalability depends on network).

From front-end to DAQ

- Architecture
  KM3NeT expe
  - FastADC sa
  - Trigger-less
    - front end a
    - sampling w
    - all non-ze
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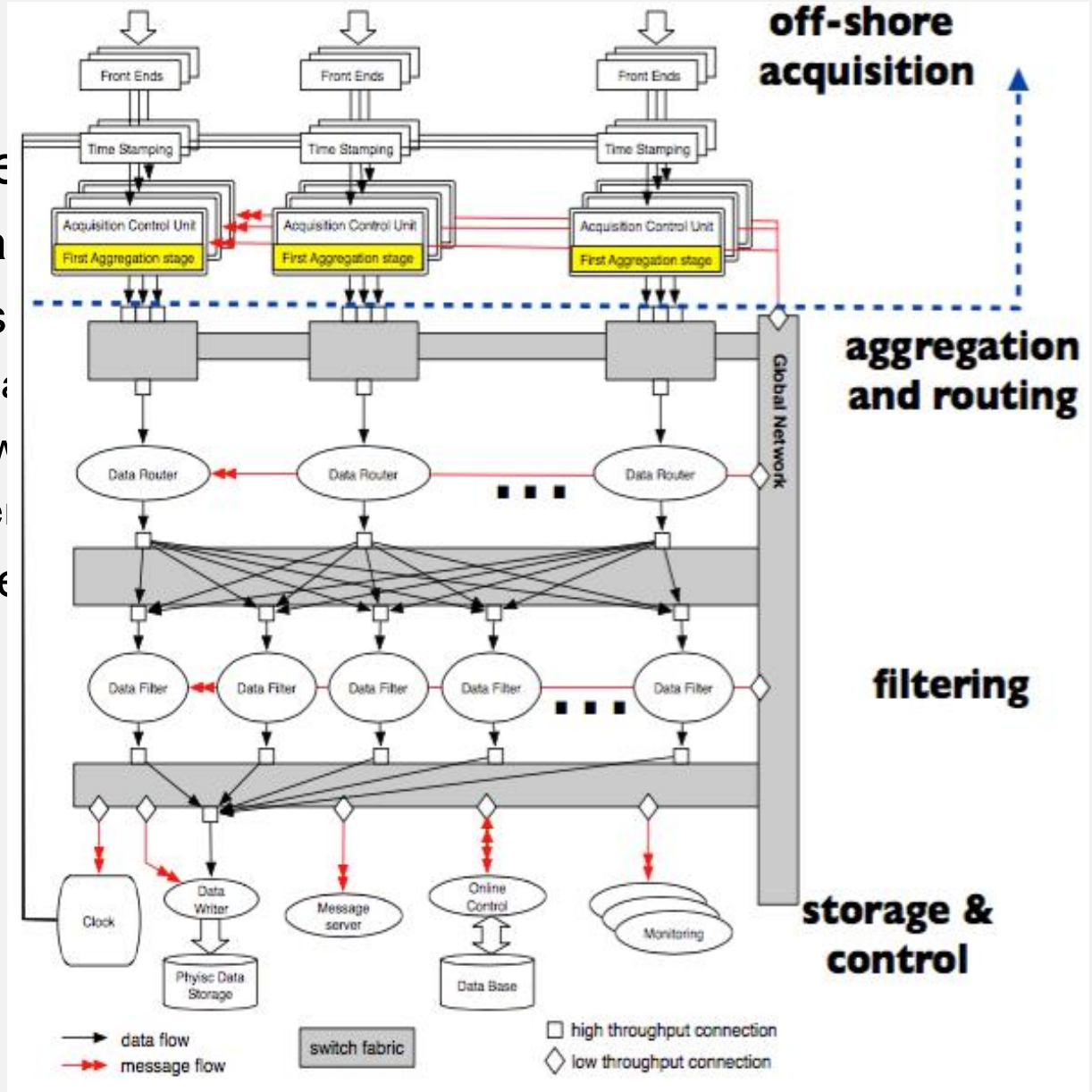
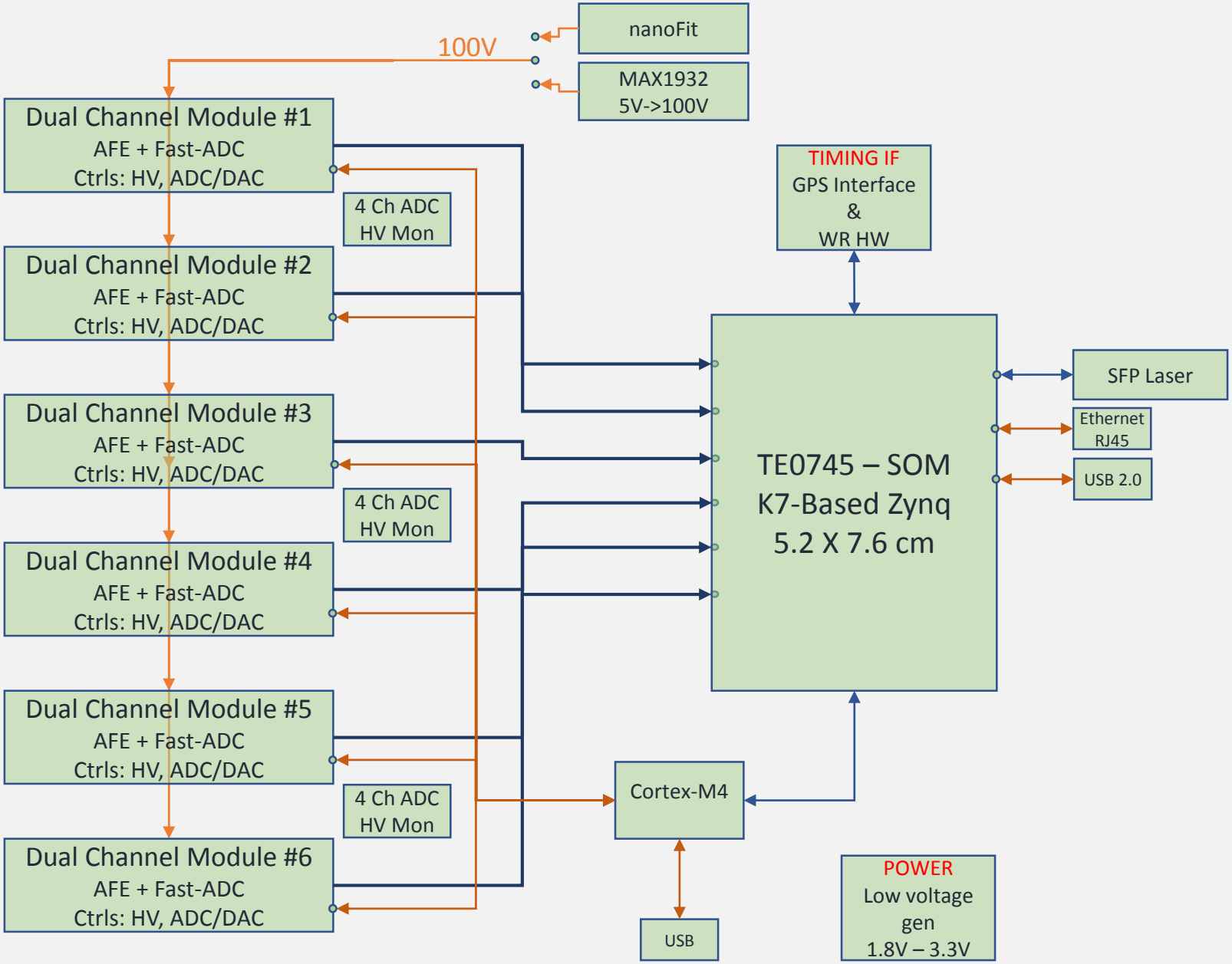


The digitizer board

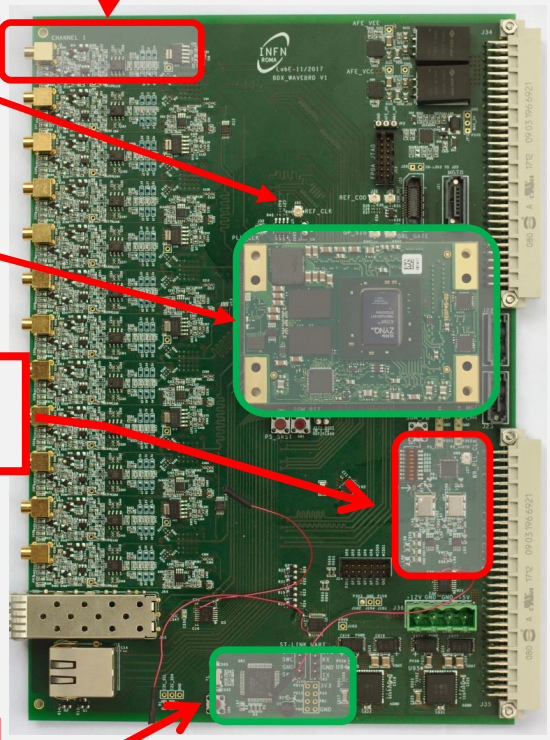
- The board is designed as a mother-board:
  - 12 analog front end channels
    - selectable gain (either 2 or 80)
    - HV provided and monitored on-board
    - pedestal set by DAC
  - 6 dual-channel ultra low-power FastADCs
  - PLL to generate and distribute sampling clock
  - accepts an external timing reference
  - an ARM-M4 controls the on-board peripherals
  - communication peripherals (GbE, SFP, …)
- The FPGA is actually a Commercial-Off-The-Shelf (COTS) System On Module (SOM) <u>mezzanine card</u> based on Zynq-7045.

Board Block Diagram



Board features

- Timing Flexible:
  - PLL to multiply and fan out the sampling clock to FastADCs and FPGA
  - White Rabbit enabled
  - Clock&Time Dedicated inputs
  - Daisy-chainable
- Customizable
  - COTS SOMs come in various flavors
  - Using SOM pinout, FPGA could be redesigned for different projects
  - FastADC is BOM-selectable
    - 12/14 bit resolution
    - 65/125/160/250 MHz max sampling rate
- ARM-M4 for peripheral control (ADC, DAC, PLL, etc)

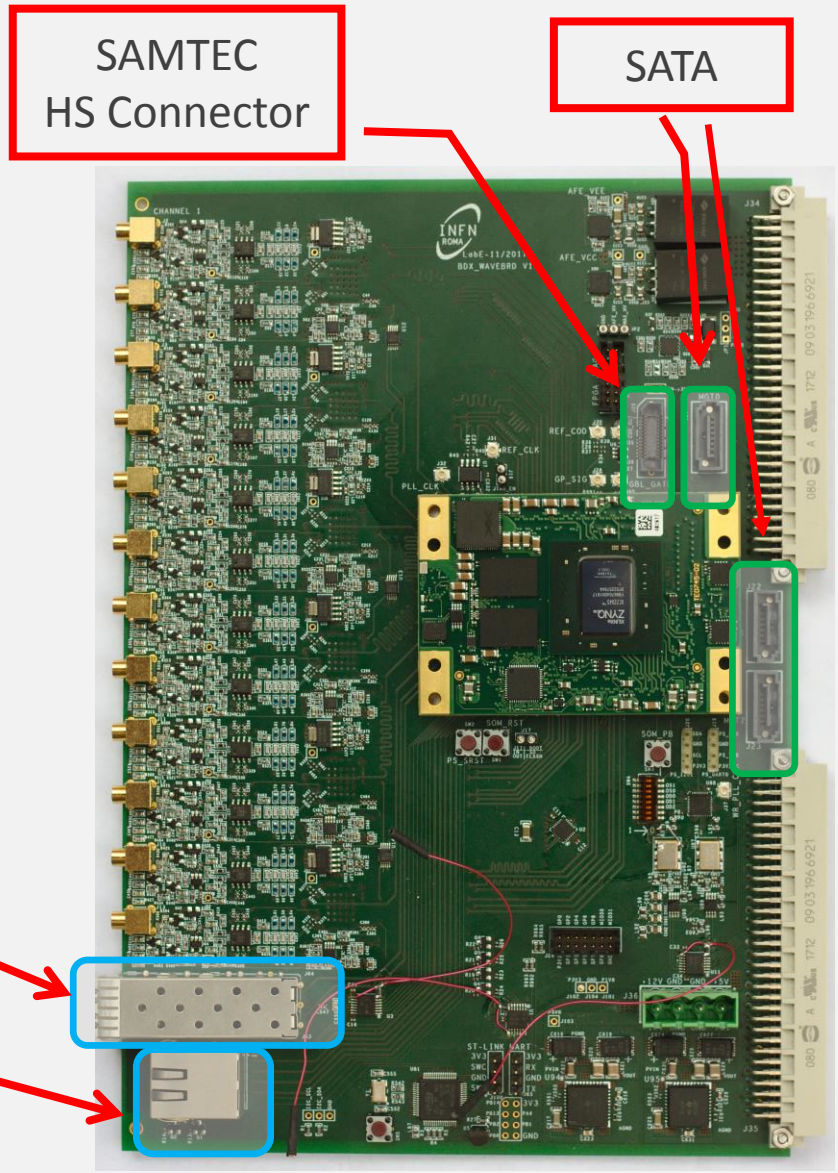


Trenz Electronics – TE0745 – Pluggable SOM

- K7-Based Zynq
- Zynq-7030/7035/7045
- DC/DC onboard
- 1GB DDR3
- 32 MB SPI Flash
- 1 Gb Ethernet PHY
- USB 2.0 PHY
- I2C, RTC, EEPROM (MAC)
- 250 I/O pins + 6 MIO
- I/O banks power from connector

Board features: Interfaces

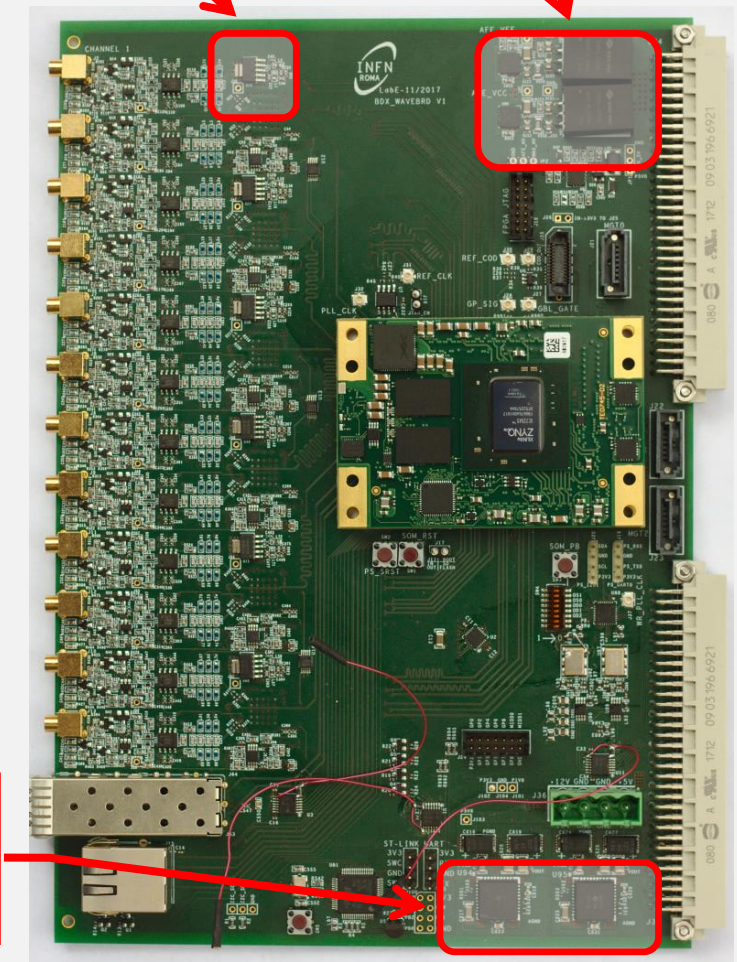
- HS interface resources:
  - 1 x GbE connector (PS driven)
  - 1 x SFP connector (PL driven)
  - 3 SATA connectors
  - High Speed Samtec expansion connector
  - Boards can be easily daisy chained using FPGA MGTs on SATA connectors.
  - 1 x USB On The Go



Board features: Power

- Power
  - Dedicated 1.8V linear regulator per FastADC
  - Dedicated linear regulators for analog front-end supplies (+5V and -5V)
  - VME connectors only for power and mechanical support
  - High Voltage provided on-board

Total power ~20 W



Board features

- Board cost is adjustable to target project
  - Use the right ADC: price ranges from 9 to 65 €/ADC channel
  - Use the right SOM: 500€ to 780€

Total cost ranges from 1.3k€ to 1.9k€ per board

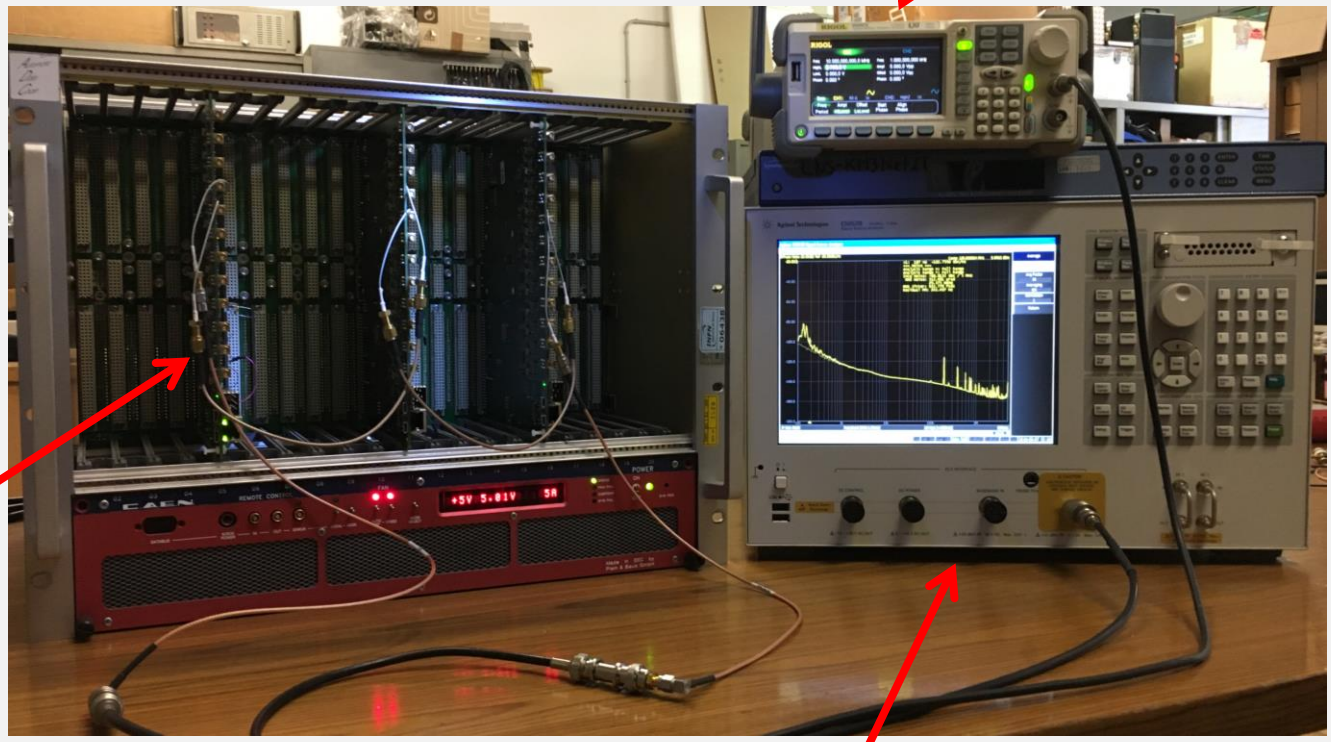
Timing: test bench setup

- Assess timing performance
- The board clock input is 10 MHz
  - GPS receivers usually produce 10 MHz
  - The on-board PLL accepts up to 250 MHz
- 3 boards in daisy-chain configuration
  - Last board outputs 250 MHz instead of 10 MHz
- Performance assessed measuring last board jitter with E5052B-Signal Source Analyzer
- Two sets of measures, according to chain input clock:
  - 10 MHz free-run (uses locally synthesized frequency from PLL)
  - 10 MHz from clock generator

Timing test bench picture

- The create contains 3 daisy-chained boards
- Jitter measures:
  - On-board 10 MHz generation (free-running)
  - External Generator (DG5052)

RIGOL DG5052
10 MHz Gen

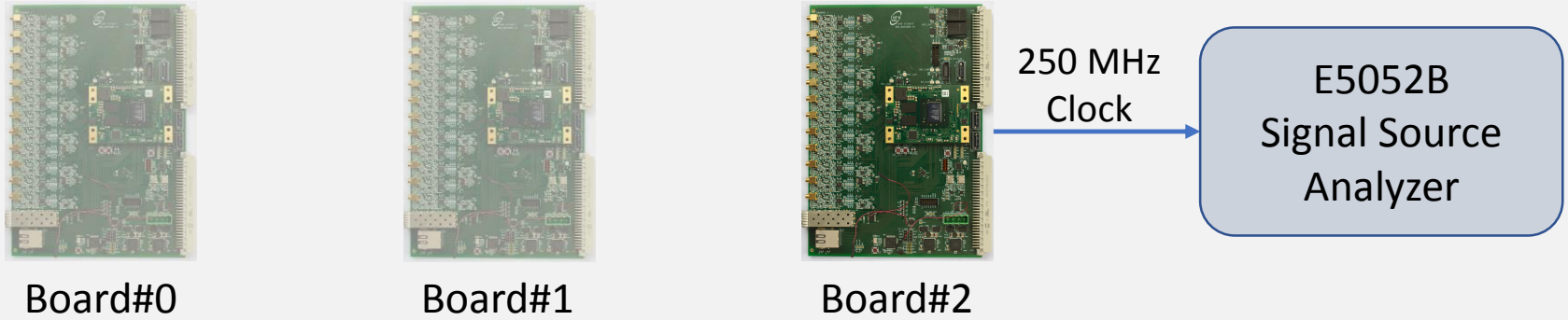


VME Crate
w/ Board UT

E5052B SSA

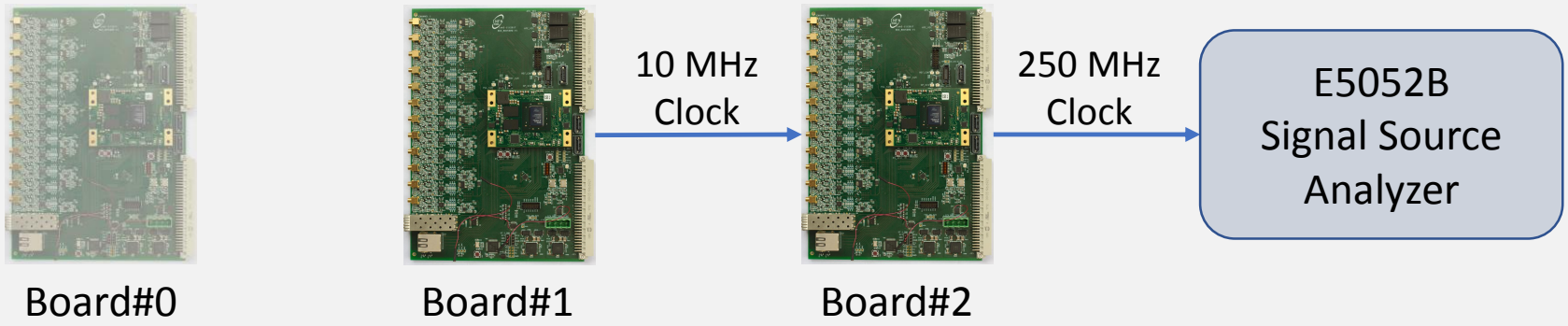
Timing: test bench setup

- Ref 10 MHz clock path:
  Board#2 is free-running using PLL quartz



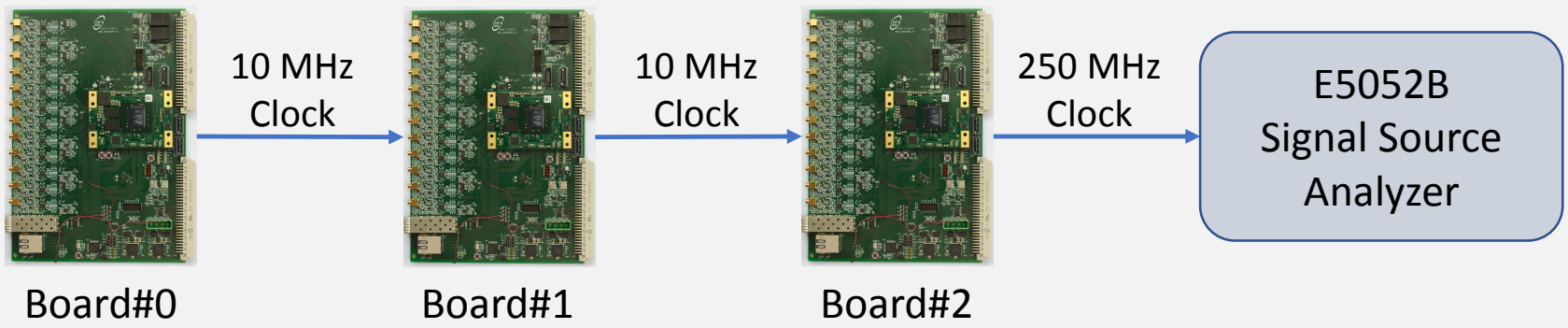
Timing: test bench setup

- Ref 10 MHz clock path:
  Board#1 freerun →Board#2



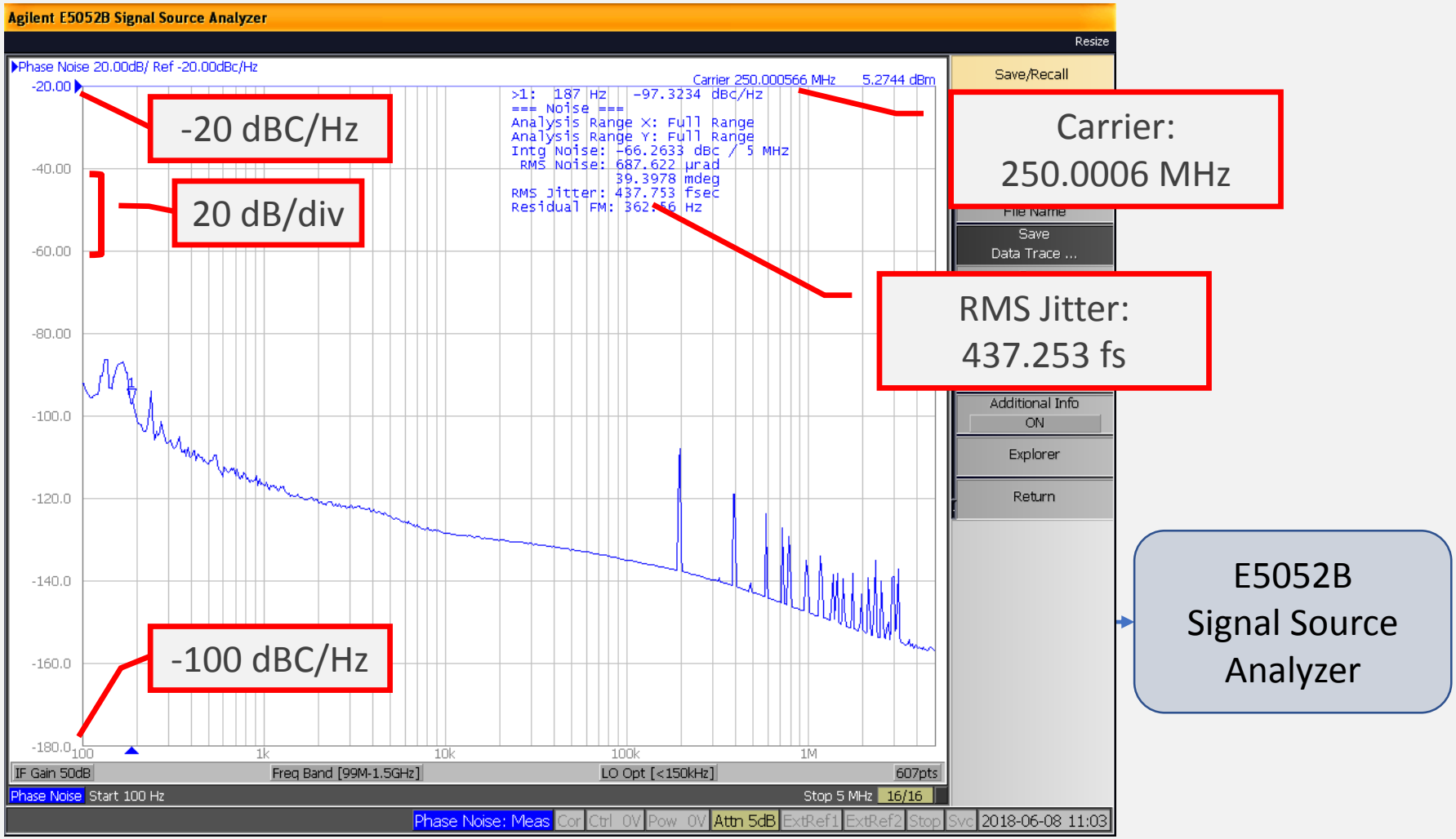
Timing: test bench setup

- Ref 10 MHz clock path:
Board#0 Freerun → Board#1 → Board#2



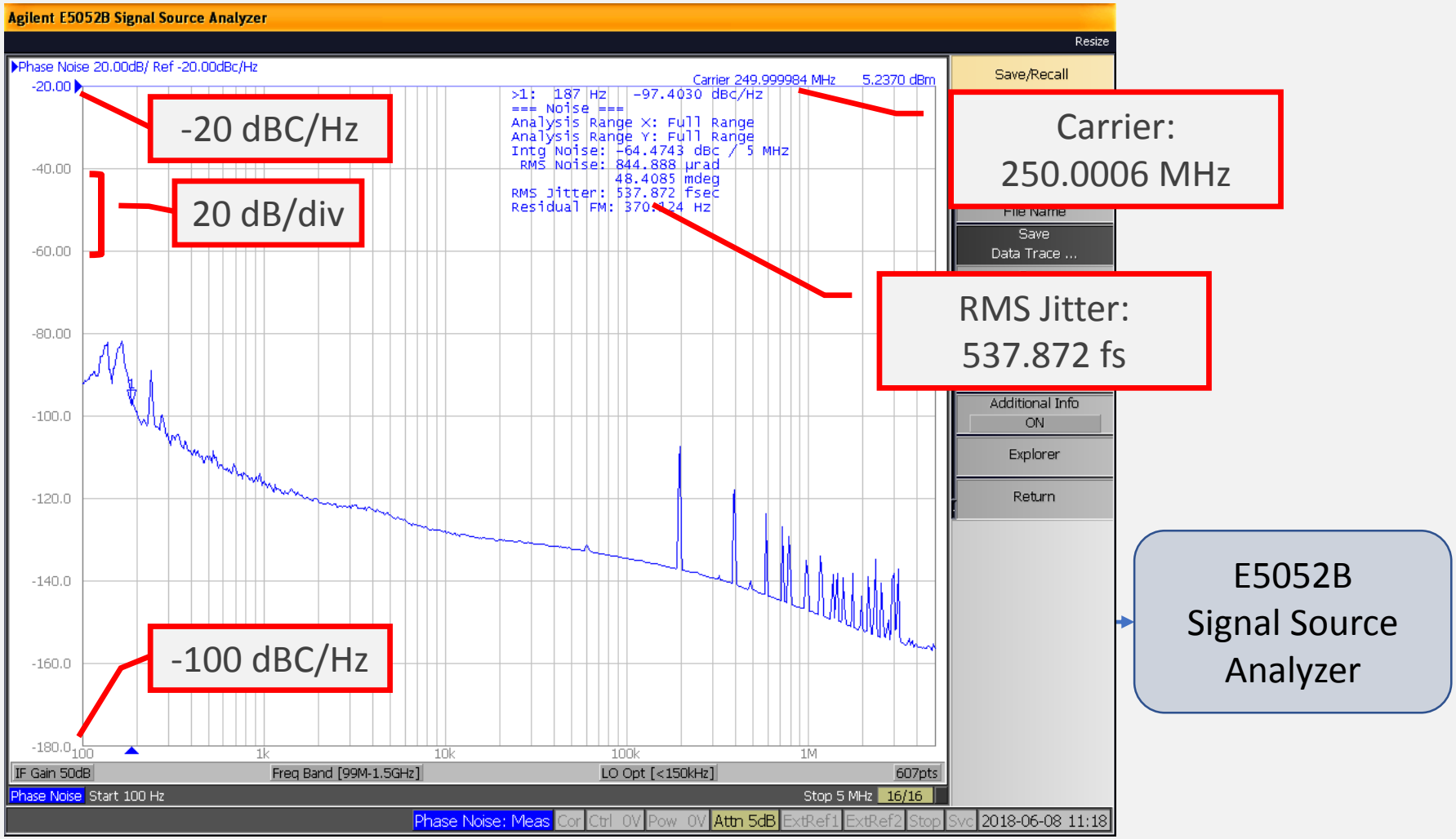
Timing: test bench setup

- Ref 10 MHz clock path:
  Board#2 freerun



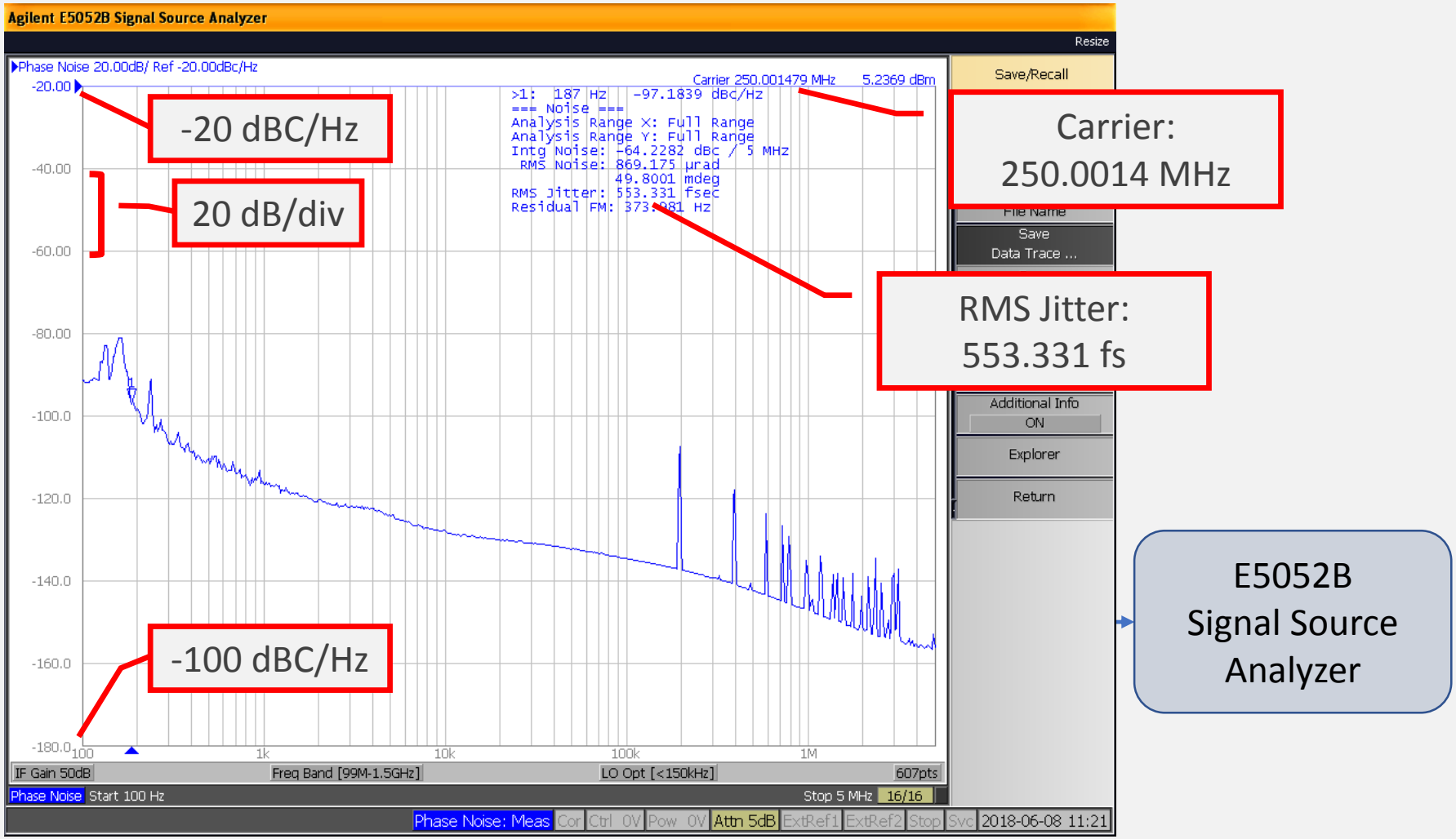
Timing: test bench setup

- Ref 10 MHz clock path:
  Board#1 → Board#2



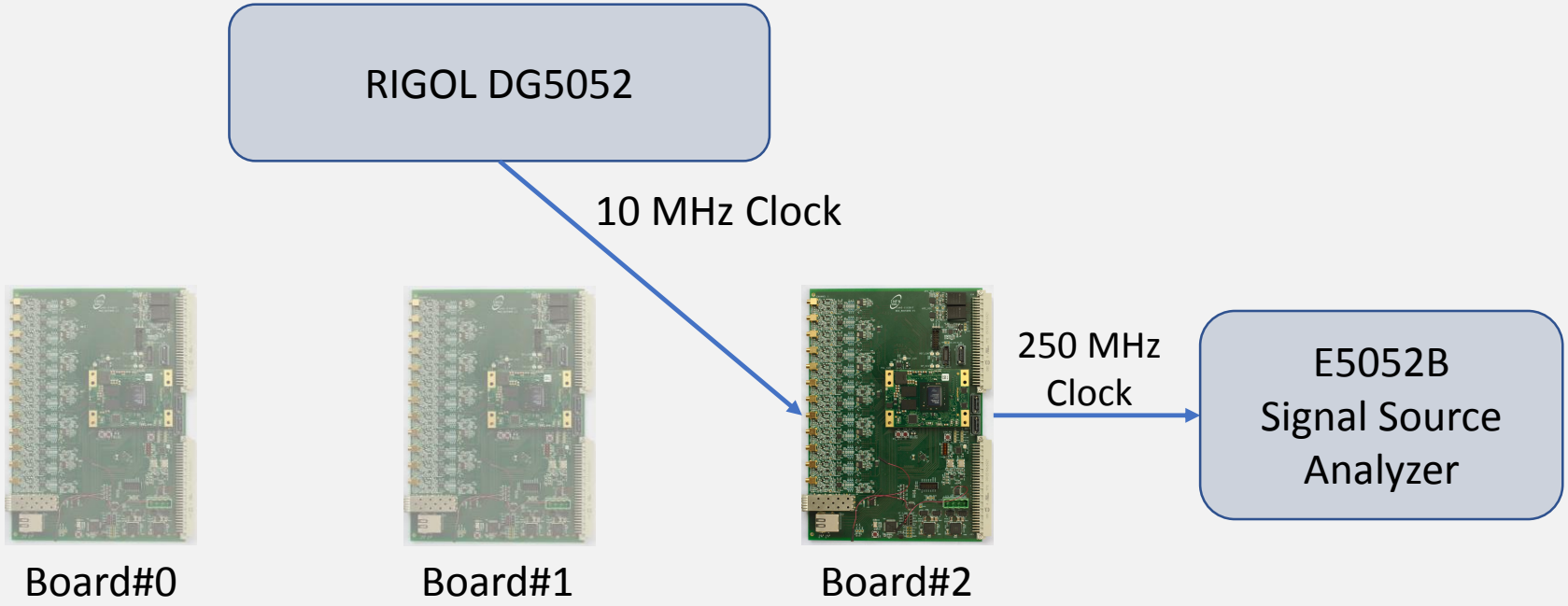
Timing: test bench setup

- Ref 10 MHz clock path:
  Board#0→ Board#1 → Board#2



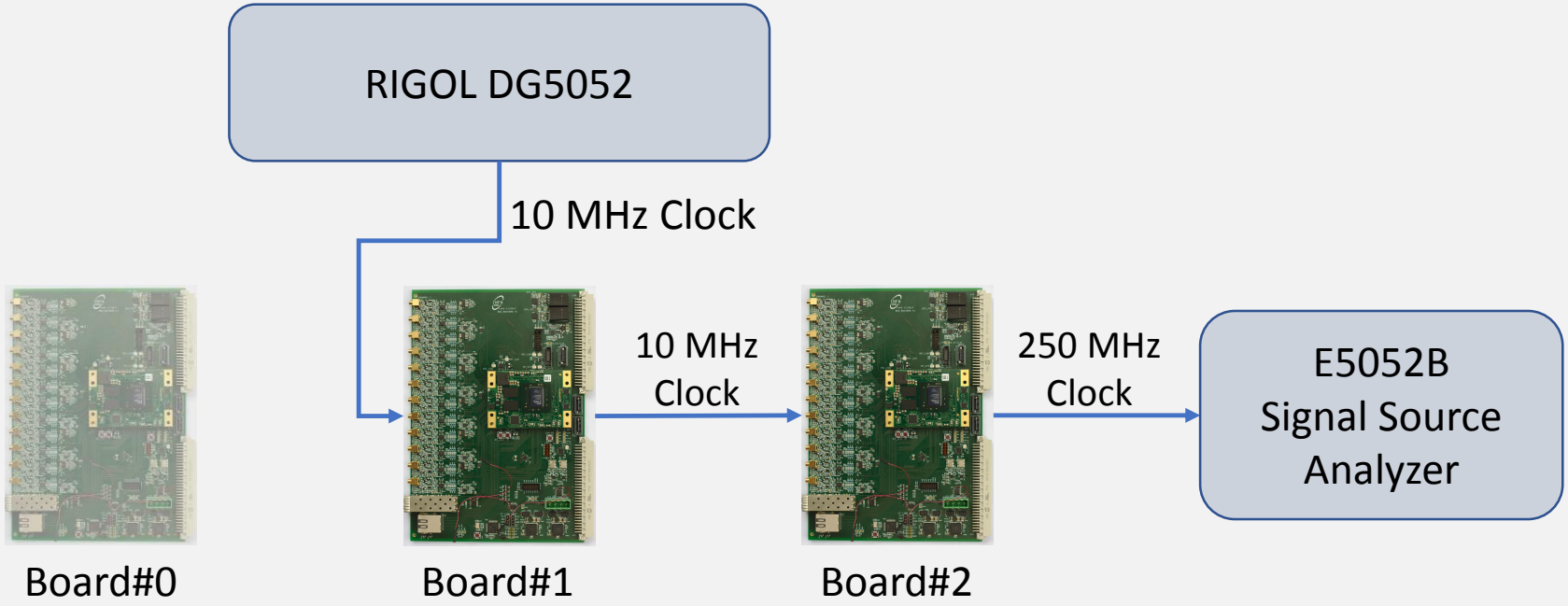
Timing: test bench setup

- Ref 10 MHz clock path:
  Gen →Board#2



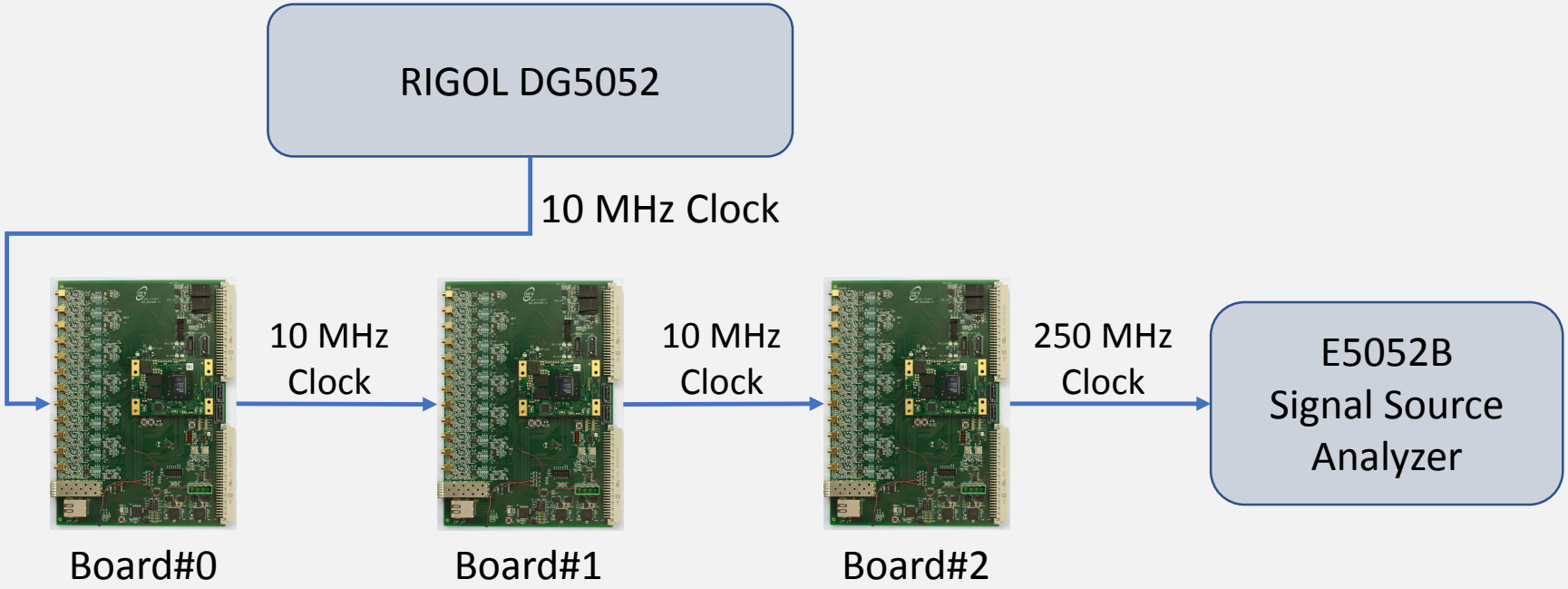
Timing: test bench setup

- Ref 10 MHz clock path:
  Gen →Board#1 →Board#2



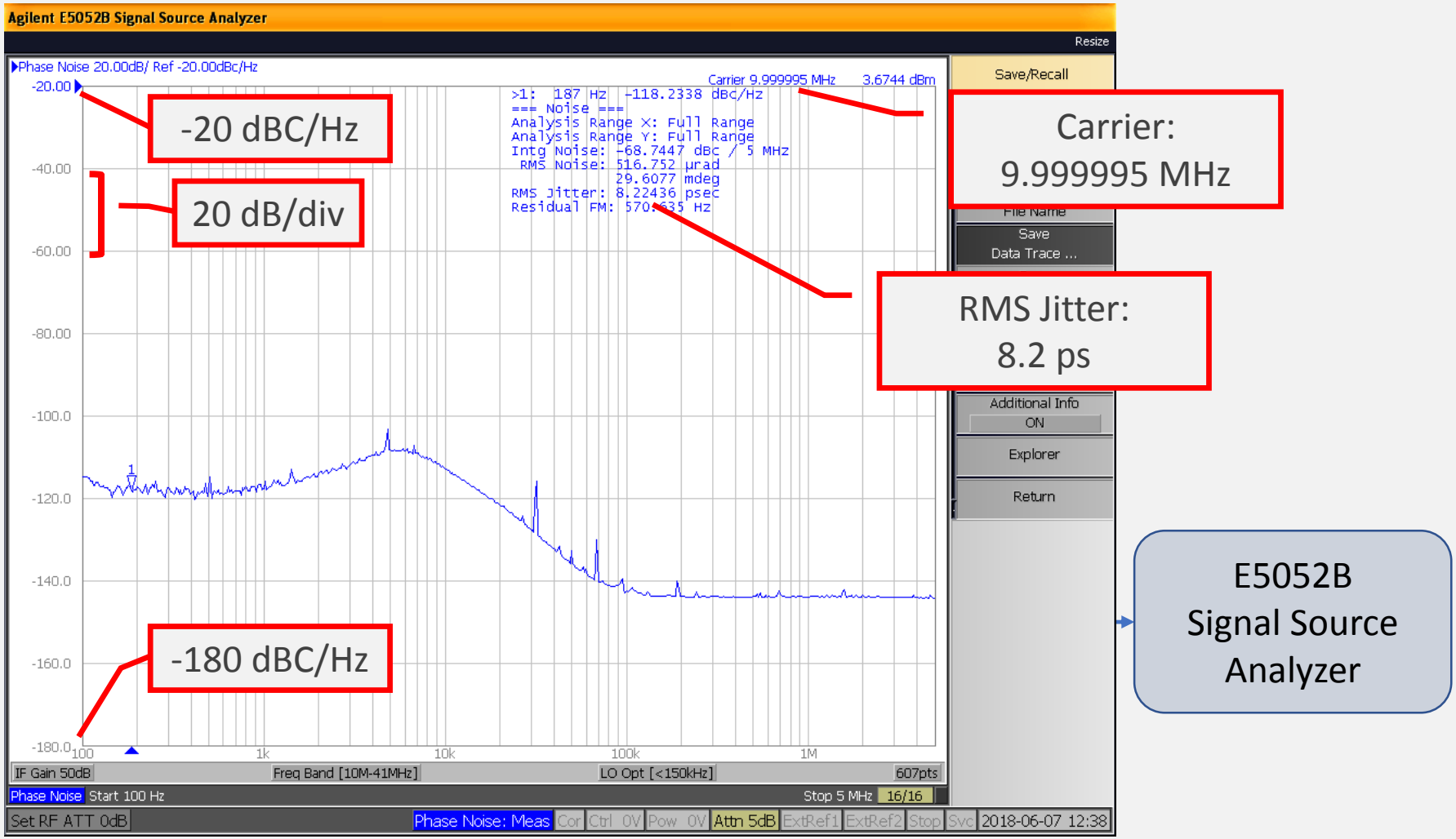
Timing: test bench setup

- Ref 10 MHz clock path:
Gen → Board#0→ Board#1 → Board#2



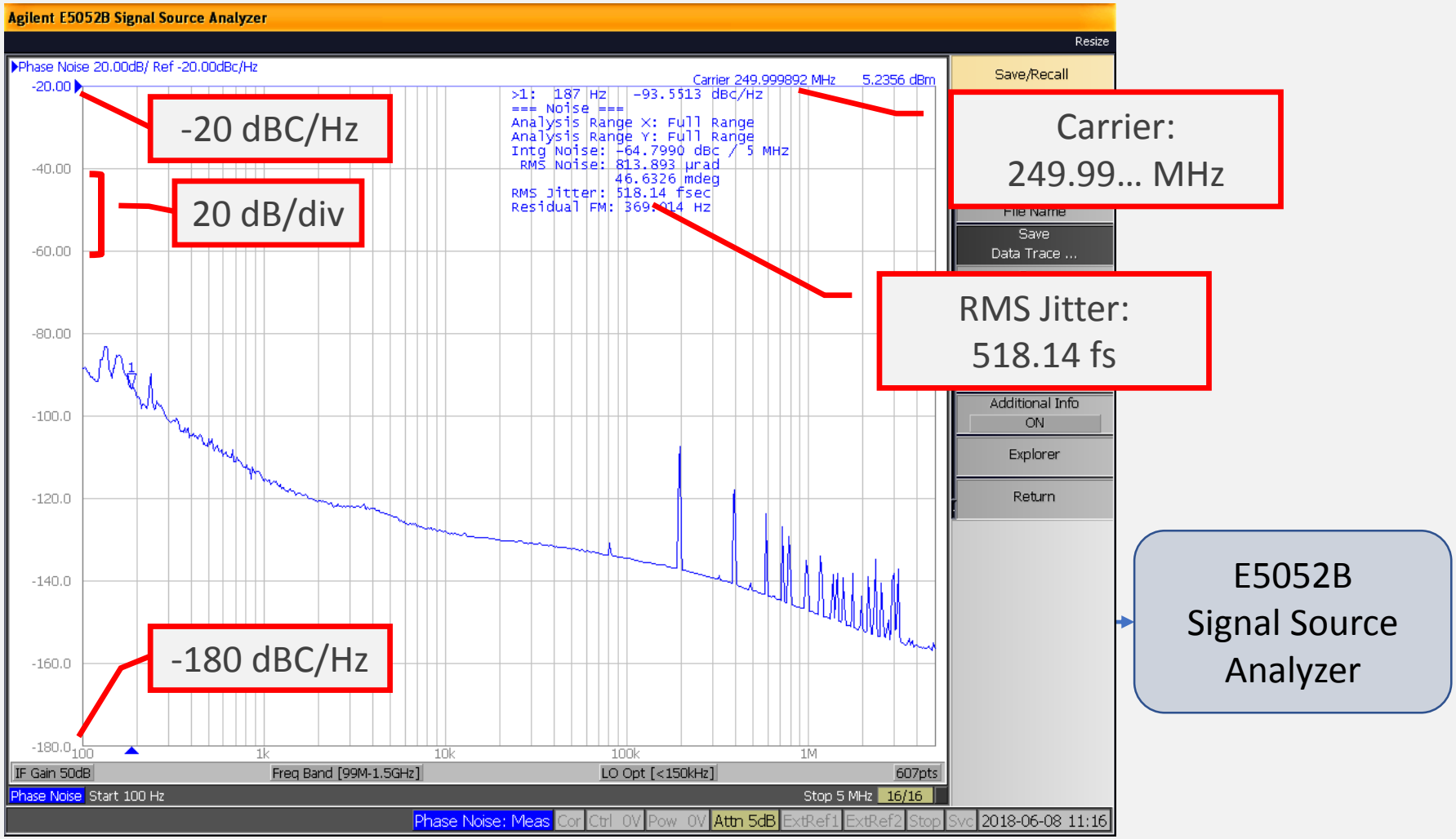
Timing: test bench setup

- Ref 10 MHz clock path: Generator Clock JItter



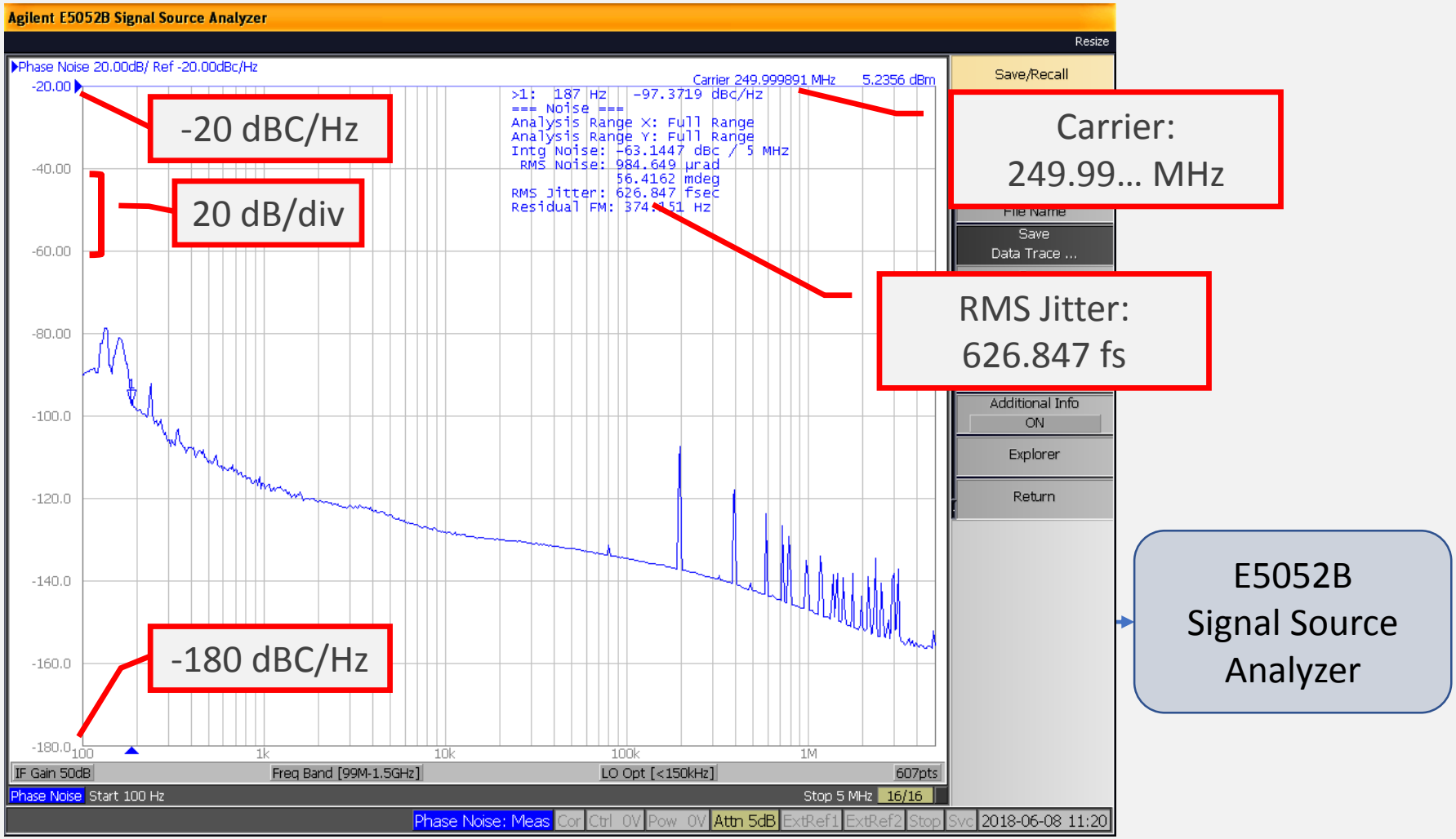
Timing: test bench setup

- Ref 10 MHz clock path:
  Gen →Board#2



Timing: test bench setup

- Ref 10 MHz clock path:
  Gen →Board#1 →Board#2



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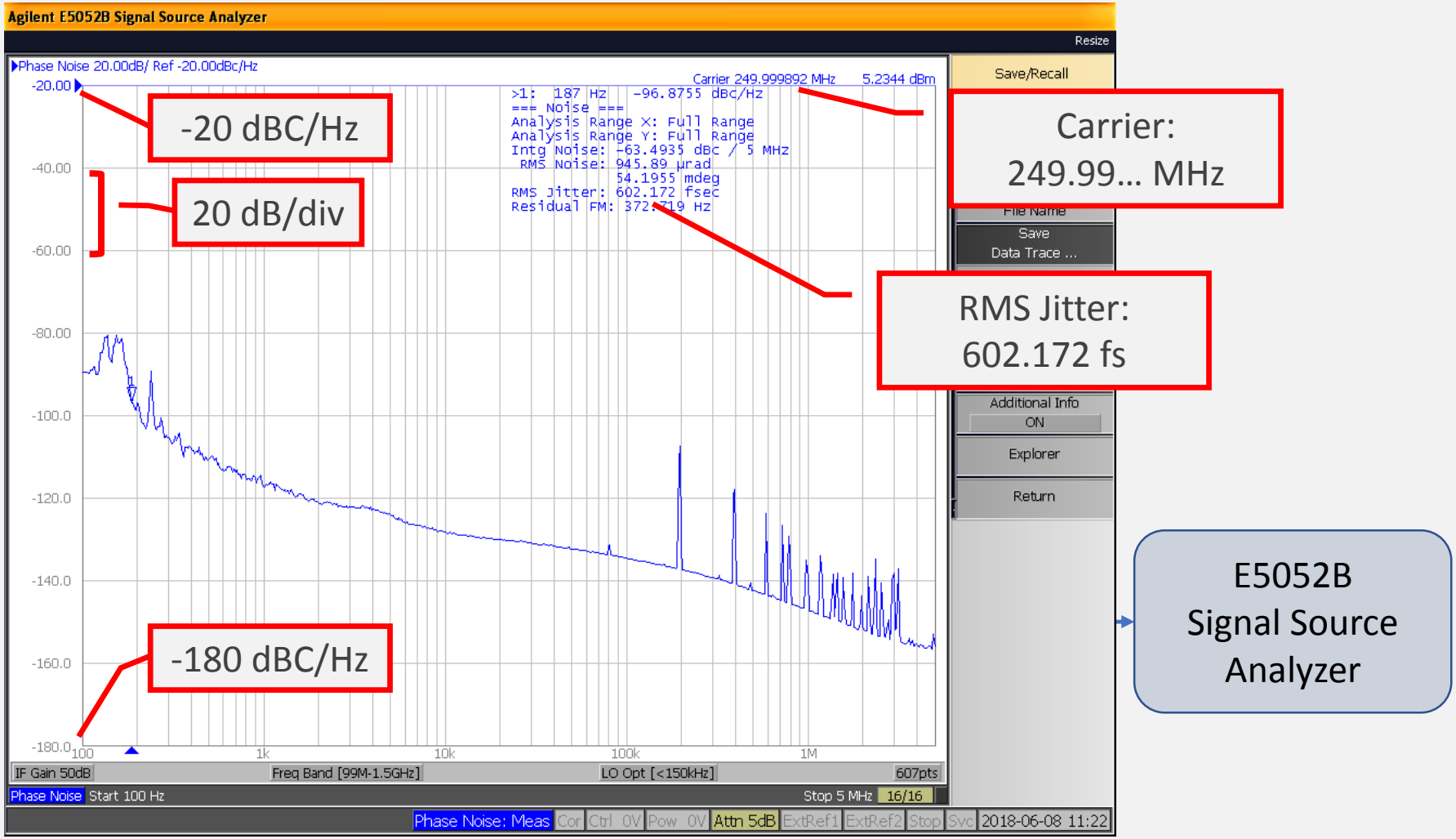
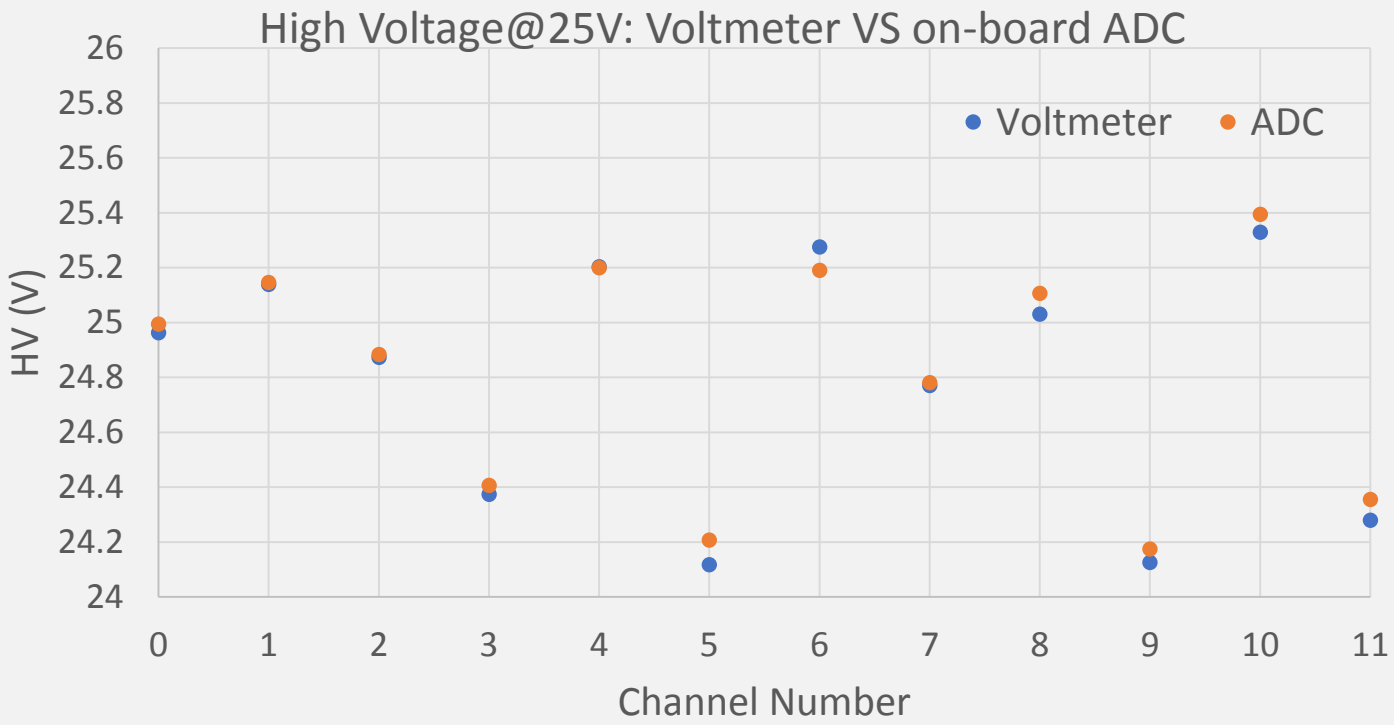


High Voltage set and measurement

- The board can set High Voltage to power sensors (typically SiPM)
  - HV is AC-coupled to sensor signal
  - up to 90V on-board generation
  - HV is linearly regulated (input up to 100V)
  - Range is from 25 to 75V, DAC selectable
- Changing HW configuration, the same circuit can control a HV generator
  (e.g. PMT HV can be set by a control voltage ranging from 0 to 2V)

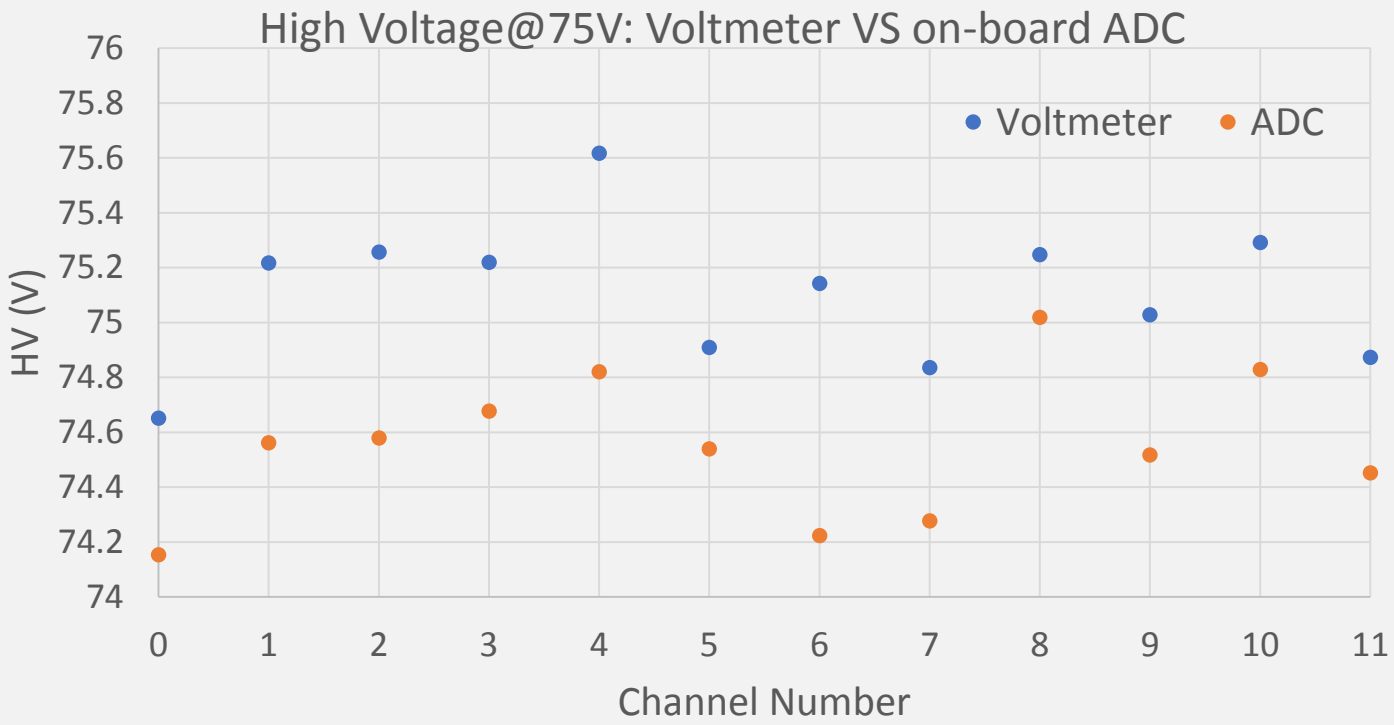
High Voltage set and measurement

- High Voltage set to 25V:
  - Values read by Voltmeter and on-board ADC
  - Channel average error: 0.2%



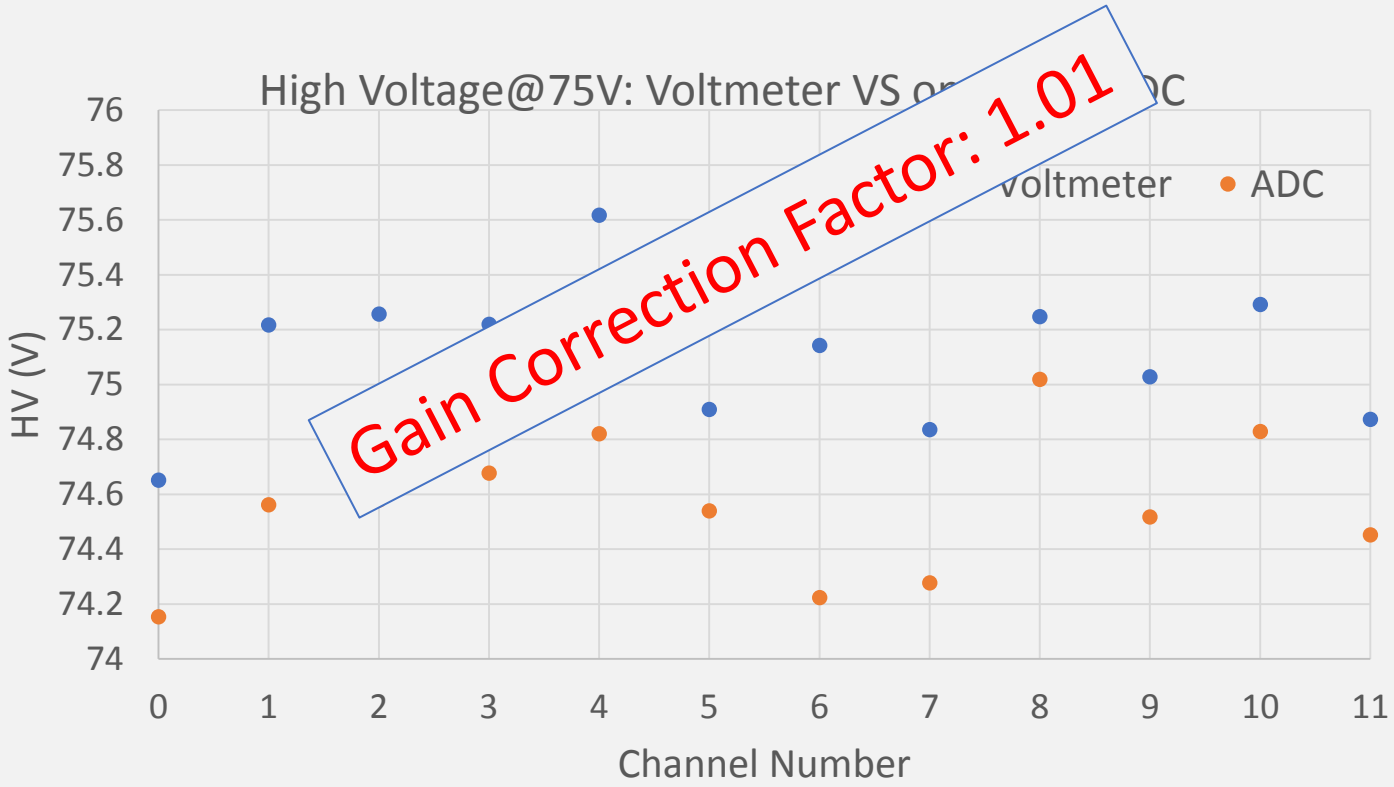
High Voltage set and measurement

- High Voltage set to 75V:
  - Values read by Voltmeter and on-board ADC
  - Channel average error: 0.7%

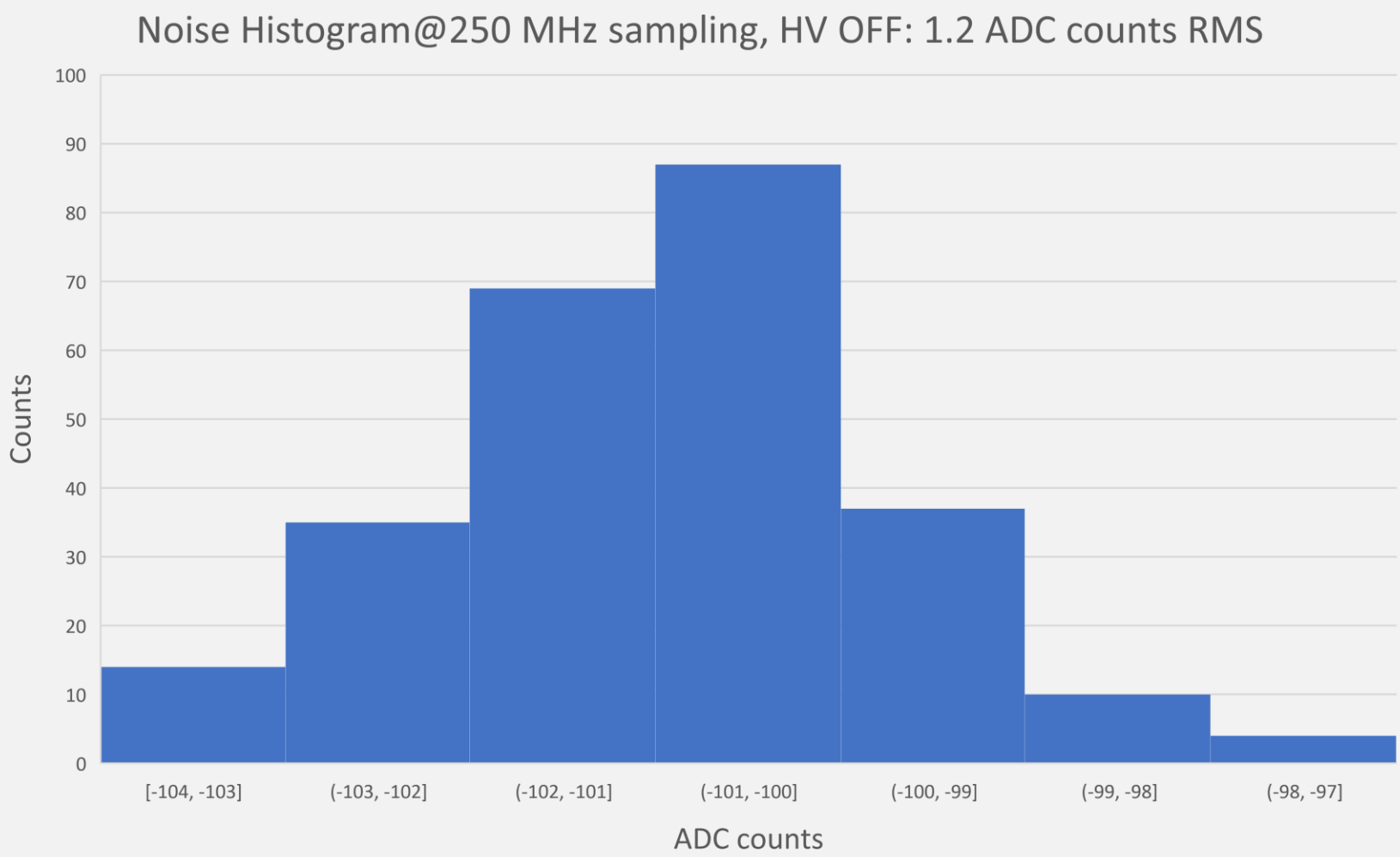


High Voltage set and measurement

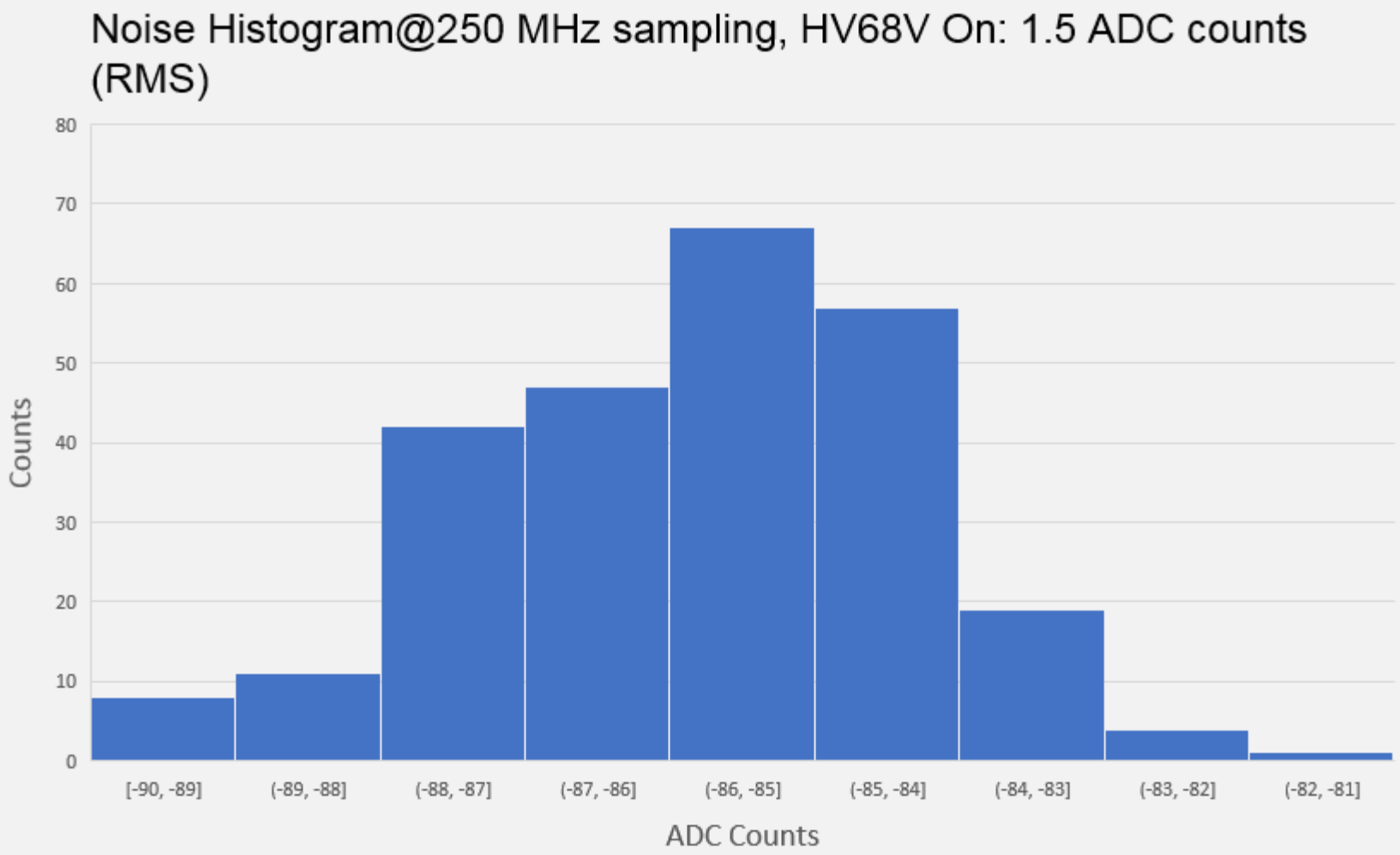
- High Voltage set to 75V:
  - Values read by Voltmeter and on-board ADC
  - Channel average error: 0.7%



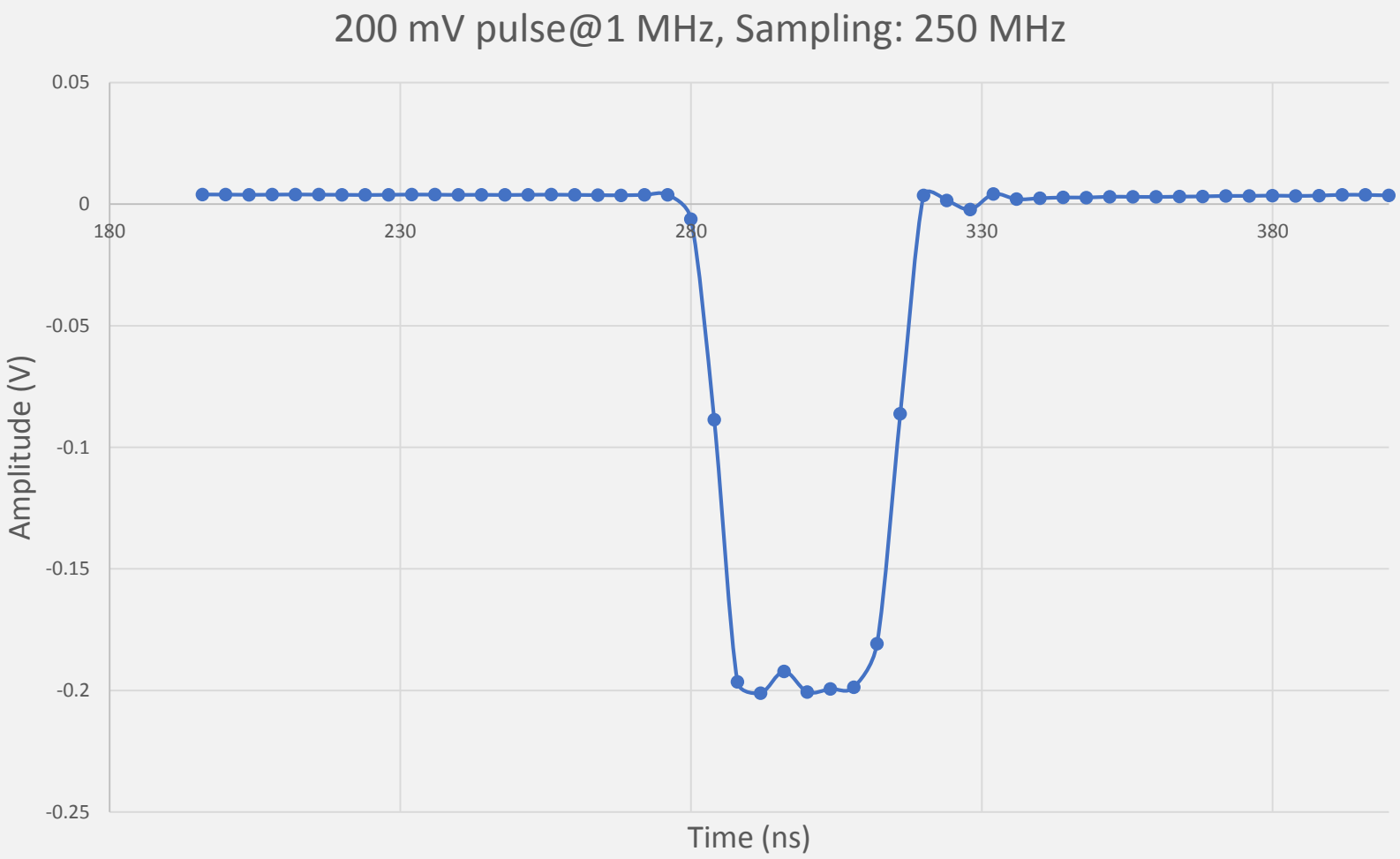
Board preliminary results: Noise w/o HV



Board preliminary results: Noise w/ 68V HV



Board preliminary results: Sampling



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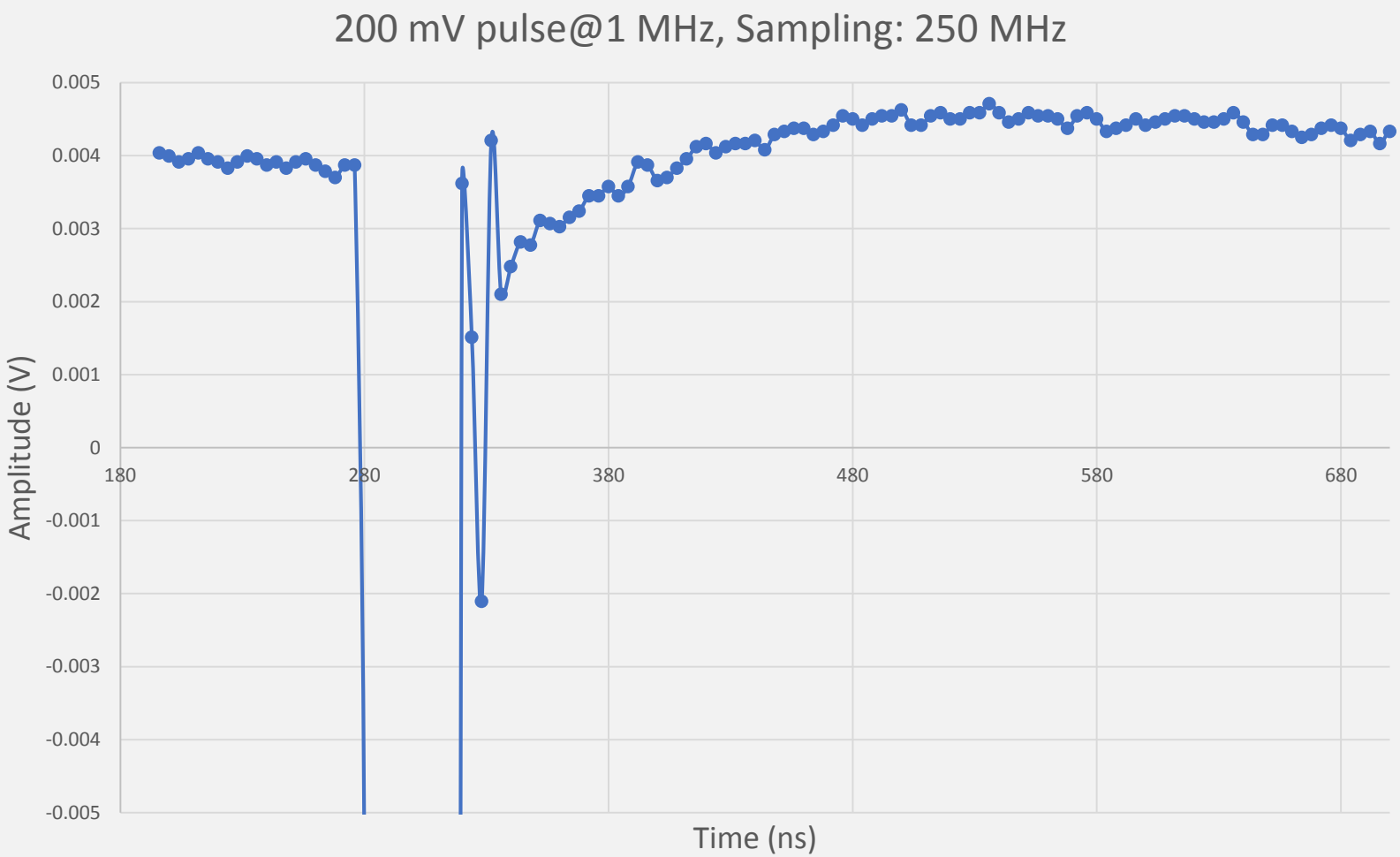


Future work

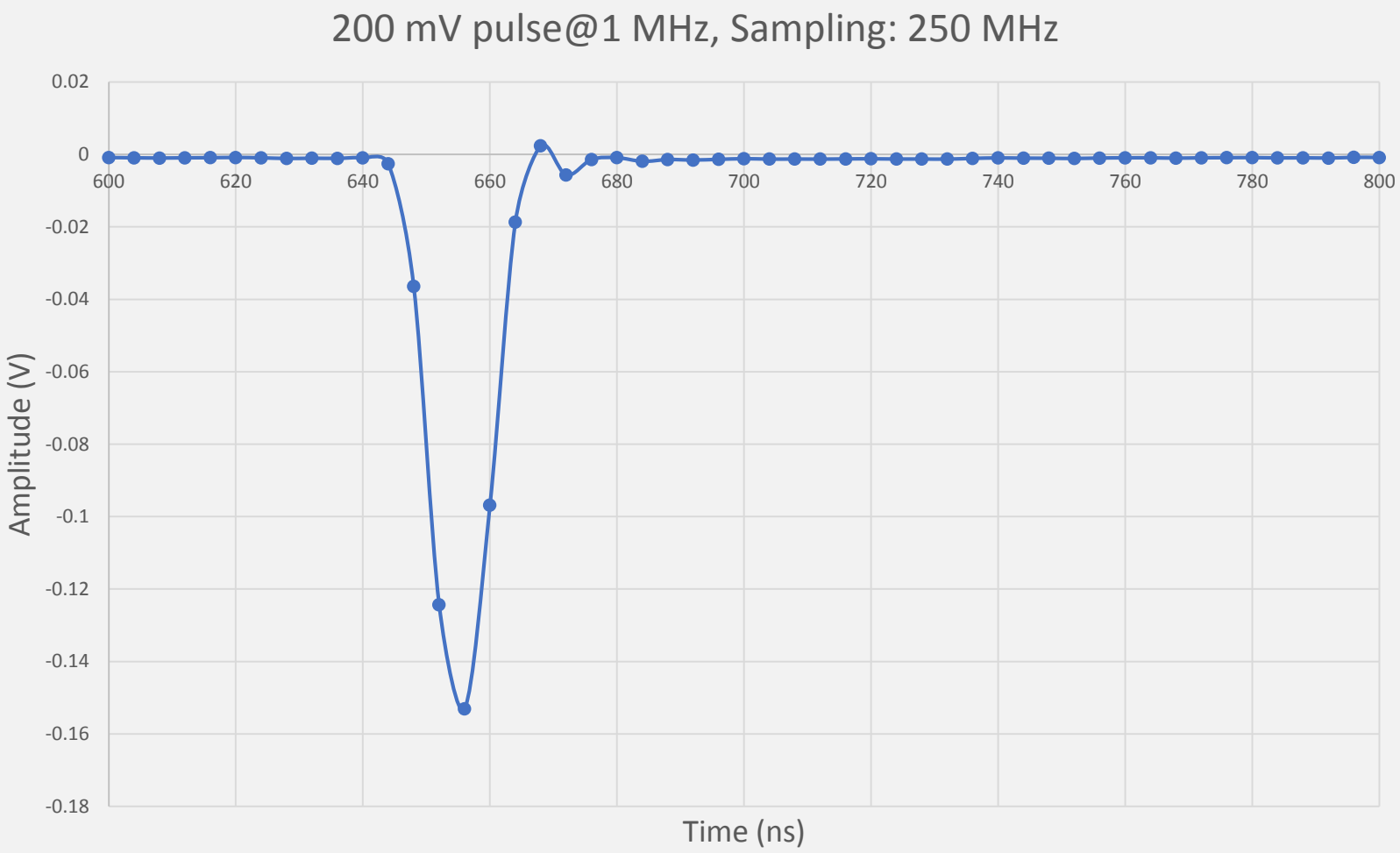
- Sampling:
  - Performance assessment w/ all channels active
  - Amplitude Channel Calibration
  - Effective bit resolution
  - Effective timing resolution measurement through waveform reconstruction
- Slow control and DAQ:
  - implementation of slow control protocol (like EPICS, MIDAS, or other)

BDX status

- **Beam Dump eXperiment** at JLab:
  search for Dark sector particles
  in the 1 ÷ 1000 MeV mass range.
  - High intensity (≈ 10^{22} EOT/year), high energy (11GeV) e-beam
  - Detector: ~800 CsI(Tl) calorimeter + 2-layers active veto + shielding.
    Reuse BaBar crystals with improved SiPM readout.
- BDX can be ready to run within ~2 years
- Current experiment status:
  - Full proposal submitted to JLab PAC 44: **conditionally approved**
  - After PAC45 update, on-site background measurements and detector optimization studies
  - Presented update to PAC46 for approval

Thank you

Board preliminary results: sampling



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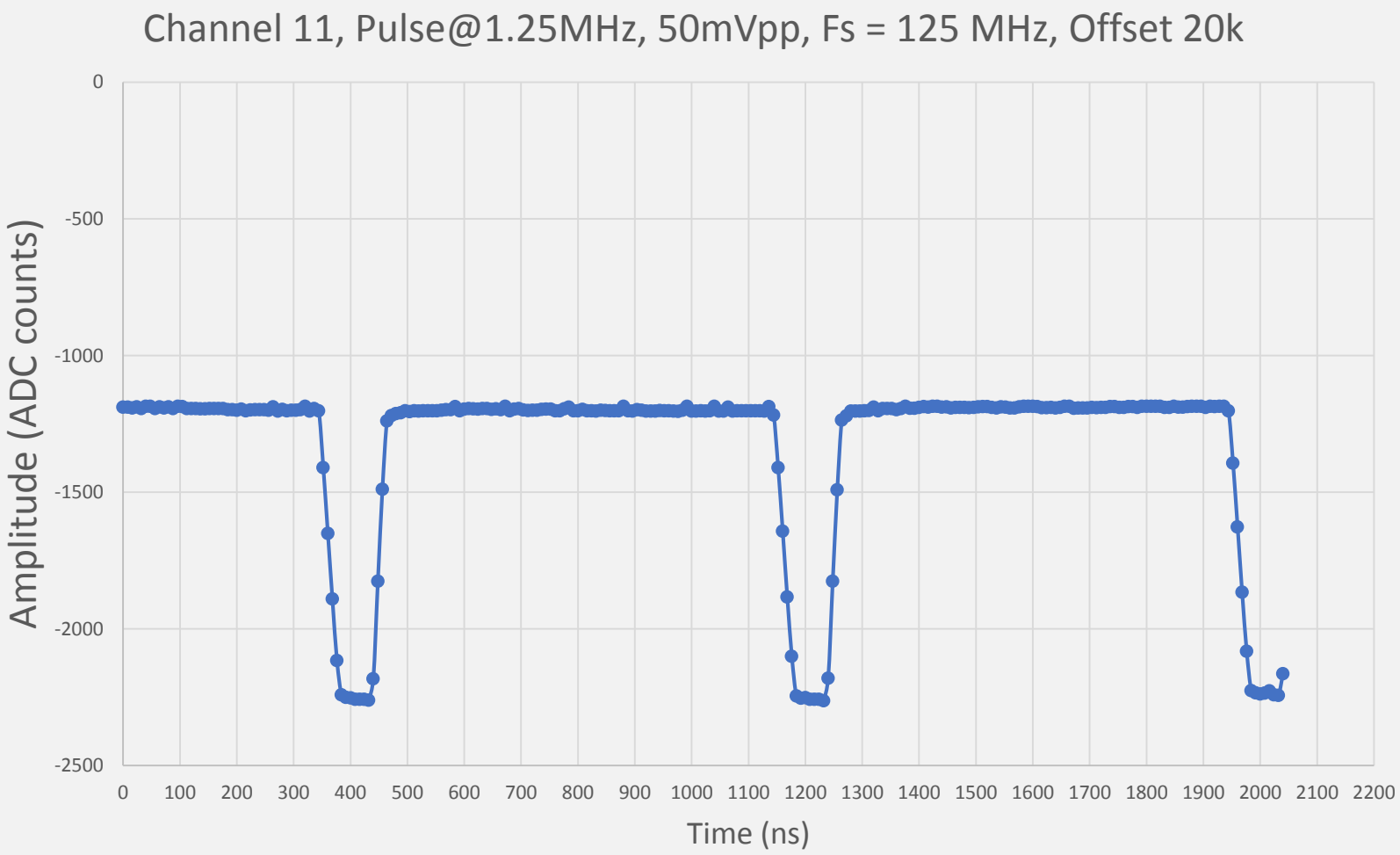

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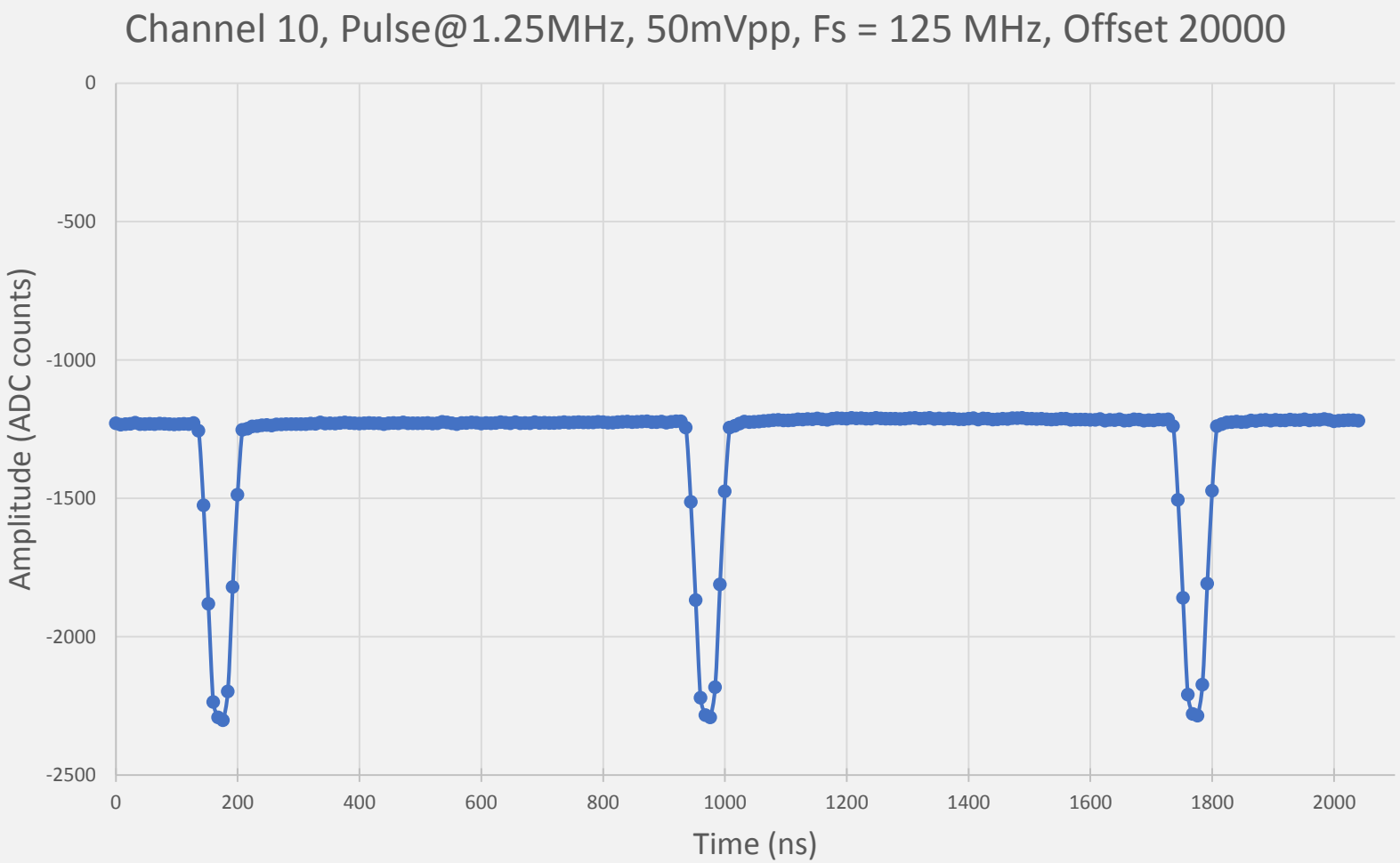
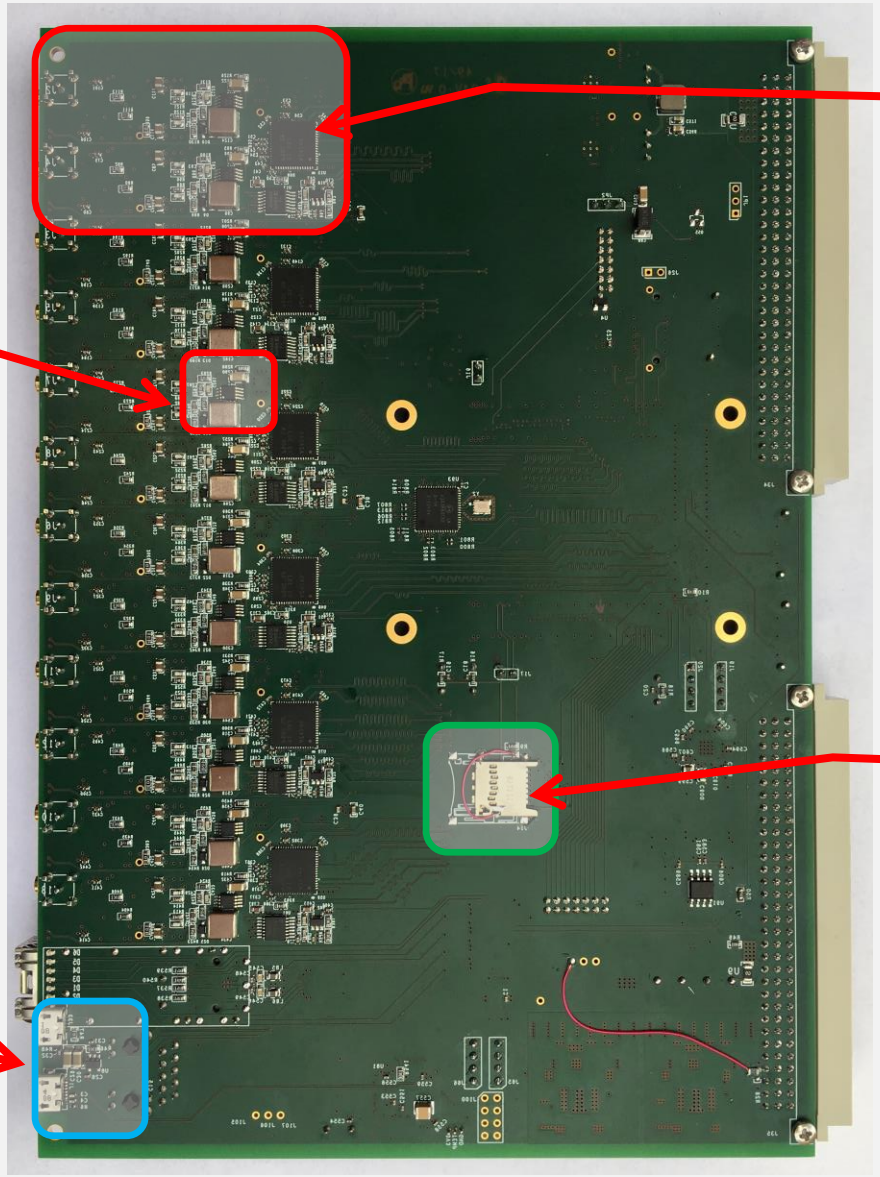
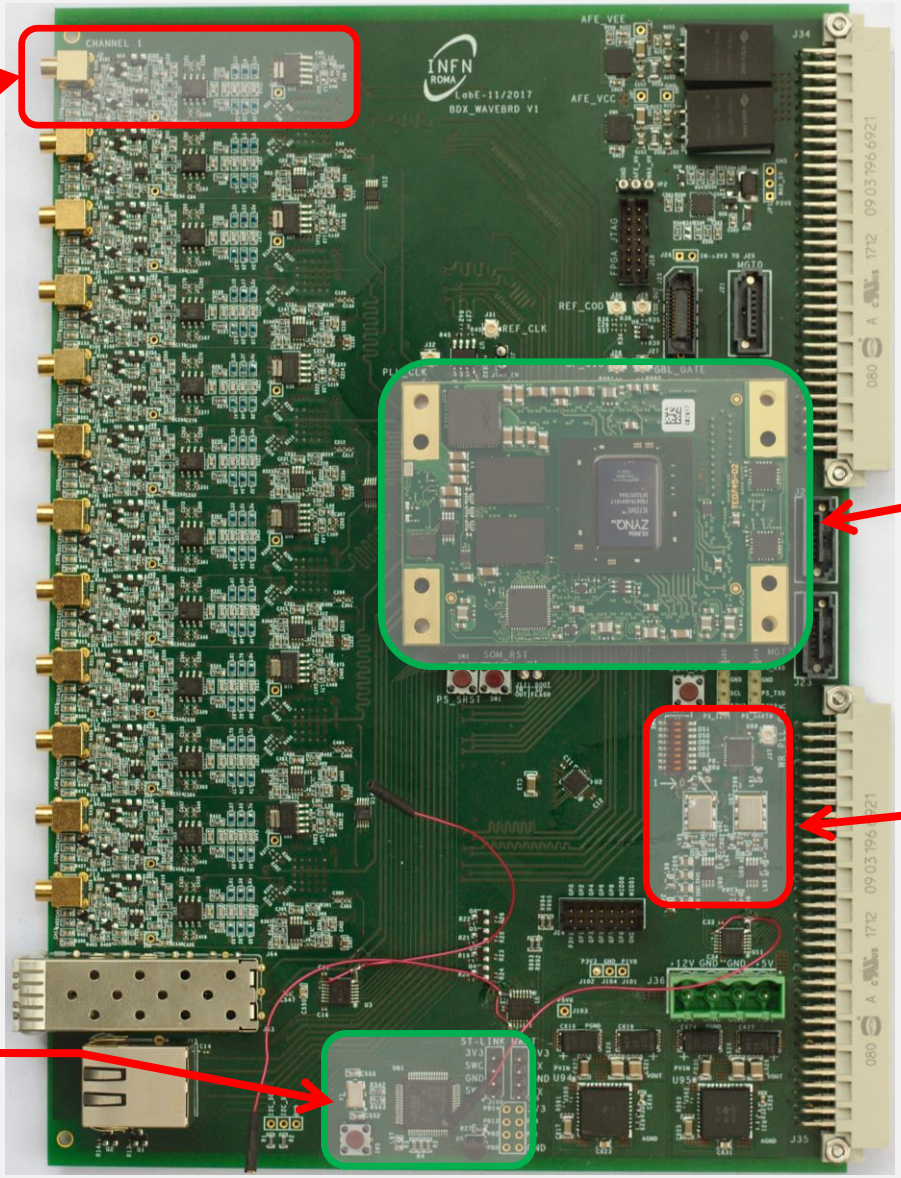


Board features



Board features: SOM, WR, M4 and front-end

Single Channel
FrontEnd
w/ High Voltage

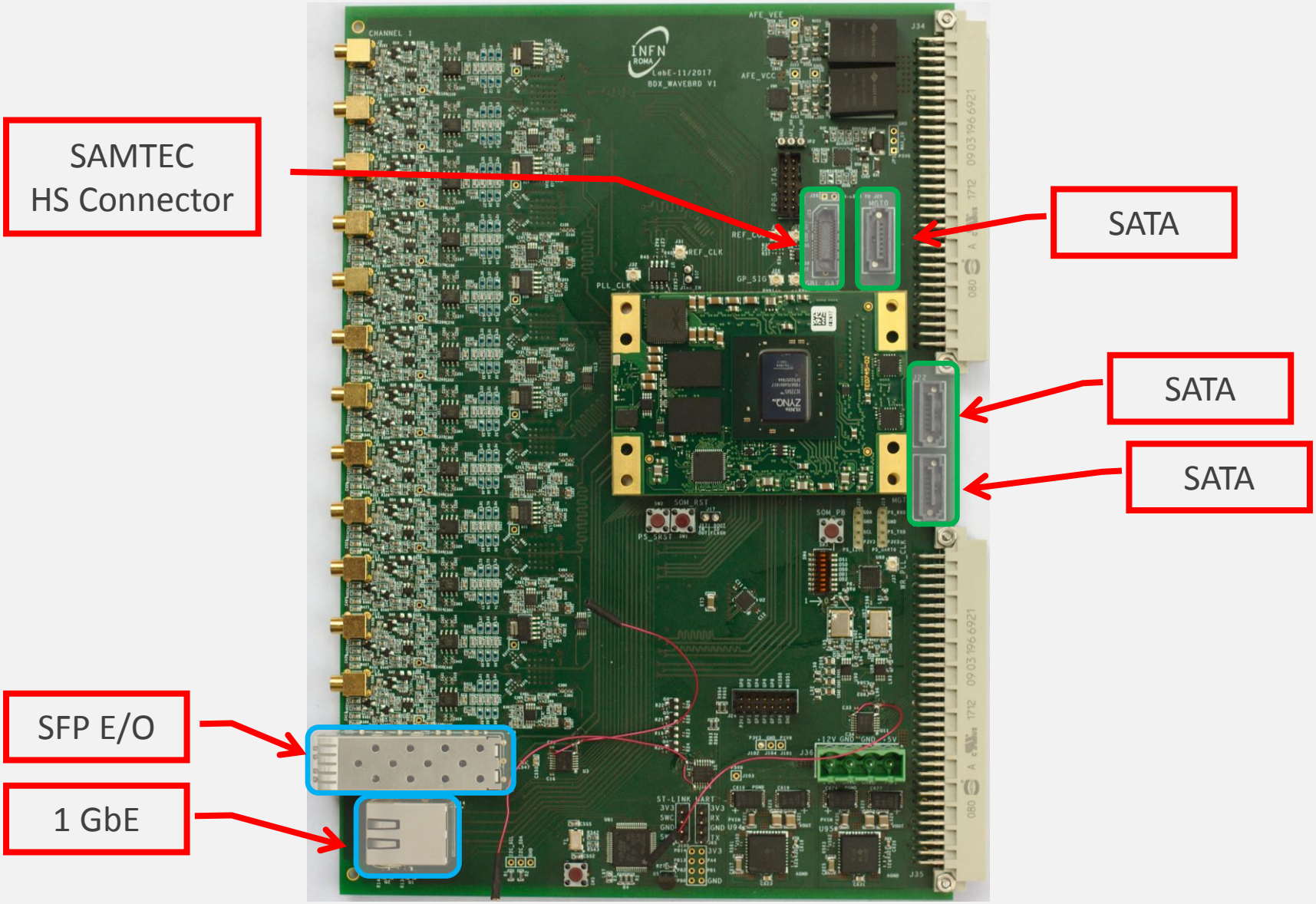


SOM

WHITE
RABBIT

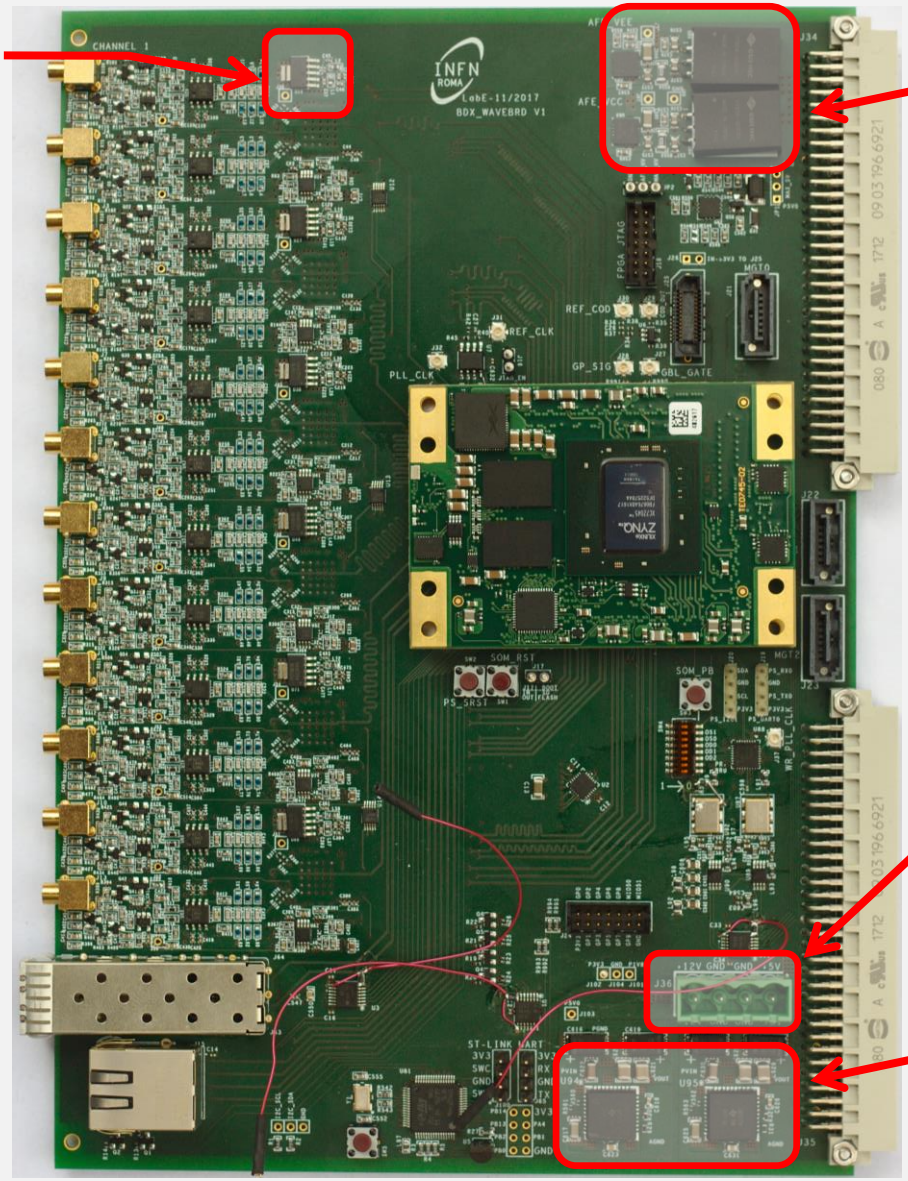
ARM-M4
Board Control

Board connections: HS interfaces



Board features: Power

1.8V FastADC Linear Regulator



Analog Supplies (+5V, -5V)

Input Power Connector

Digital Supplies (1.8V, 3.3V)