Design of Mesh-signal Readout Electronics for PandaX-III Prototype TPC

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1. Introduction

Particle And Astrophysical Xenon Experiment III (PandaX-III) is an experiment which uses a high-pressure gas TPC to search for Neutrinoless Double Beta Decay (NLDBD) of ^{136}Xe. PandaX-III TPC measures event energy, track and other various features of NLDBD.

The prototype is a small-scale, single-ended TPC. The active volume of the prototype TPC is 66 cm in diameter and 78 cm tall, and 16 kg of gas xenon is contained within it at 10 bar. 7 Microbulk Micromegas detectors are installed in the charge readout plane at the top with cathode at the bottom. The prototype TPC is designed to study the specific solution of PandaX-III experiment in Shanghai JiaoTong University (SJTU).

2. Readout Requirements

As shown in Fig. 1, the front-end electronics is comprised of 4 Front-End Cards (FECs) and 1 Mesh Readout Card (MRC). The back-end electronics is 1 Data Collection Module (DCM).

To reconstruct a complete 3D track by measuring the position of hit strips, trigger synchronization for each end-plate is required. The MRC is designed to acquire all mesh signals and generate individual 'Mesh-trigger' signals. While in the prototype TPC, 7 mesh signals are required to readout by MRC.

Considering that NLDBD Q-value of xenon-136 is ~2.5 MeV and the typical Micromegas amplification is ~1000 times, the input charge can be calculated as ~10 pC. After simulation, the Integral Non Linearity (INL) should be less than 3.2%, and the RMS noise should be less than 6 fC with 10 pC range.

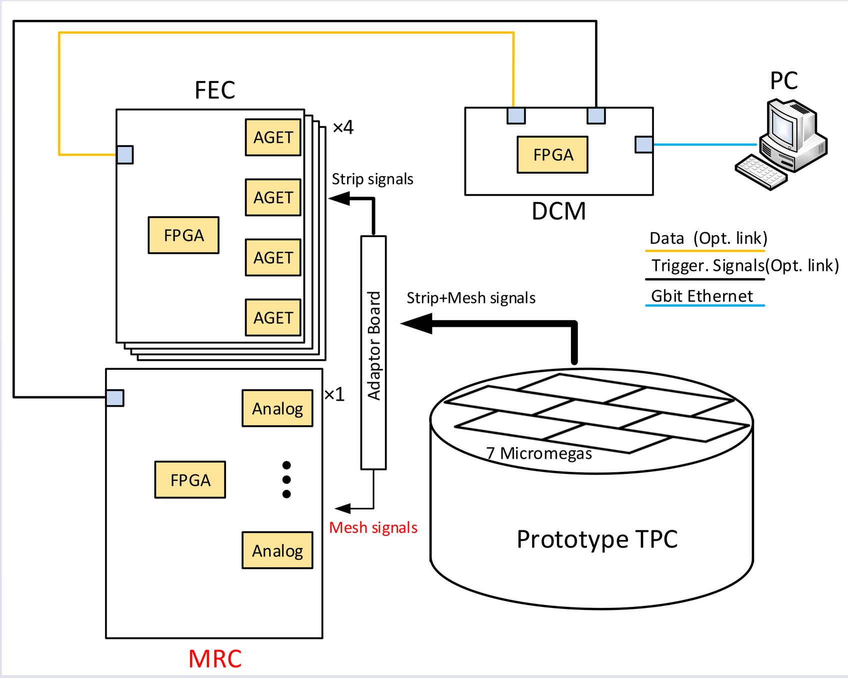

Fig. 1. Architecture of readout electronics system for PandaX-III prototype TPC.

3. Design of MRC

MRC uses discrete components to implement the charge measurement circuits as shown in Fig. 2. There are 41 analog channels on the MRC serving all meshes from Micromegas detectors, and 8 input channels with 2 ADCs has been welded for joint-test with the prototype TPC. Each input channel contains ESD protection, charge sensitive preamplifier, pole-zero cancellation circuit, CR-RC^2 shaper, baseline restorer and output buffer. MRC uses 11 quad, 12-bit, 50MSPS, serial, LVDS A/D converters to digitize the analog waveform, and records data on an FPGA chip. All the data from the MRC are sent to DCM with serial optical links and treated as trigger signals to help the front-end cards readout valid anode signals. Fig. 3 shows the photograph of MRC.

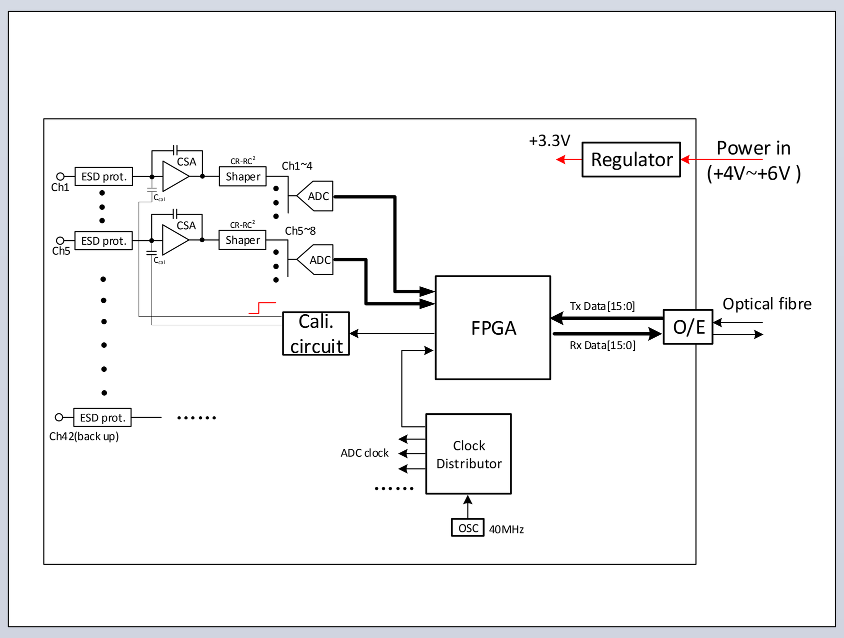

Fig. 2. Block diagram of MRC.

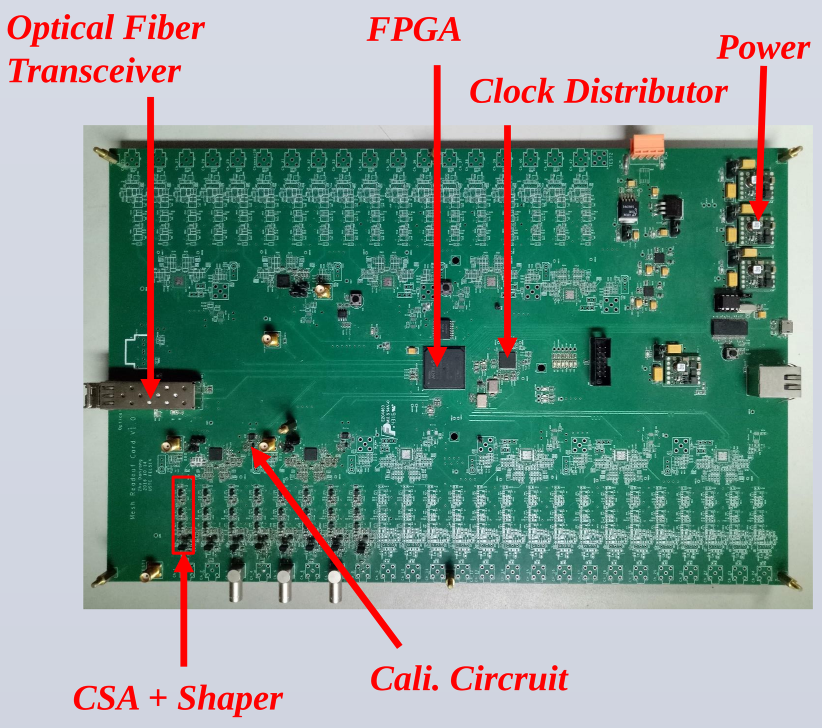

Fig. 3. Photograph of MRC.

During the experiment, zero-suppression algorithm should be applied to the data from MRC to effectively utilize the bandwidth. If mesh signal is narrow pulse, MRC can only send peak value when it is over the programmable threshold. DCM fan-outs mesh trigger to all FECs. But if mesh signal is wide pulse, MRC uses a 1us sliding window to calculate pulse area of waveform. By comparing the pulse area with threshold, MRC generates trigger signal and sends it to DCM. Fig. 4 shows the original ADC output waveform. MRC can also send the waveform over threshold, as shown in Fig. 5.

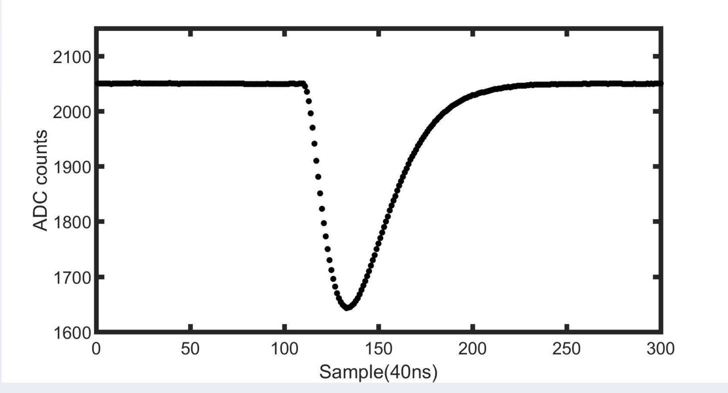

Fig. 4. Typical waveform of ADC output .

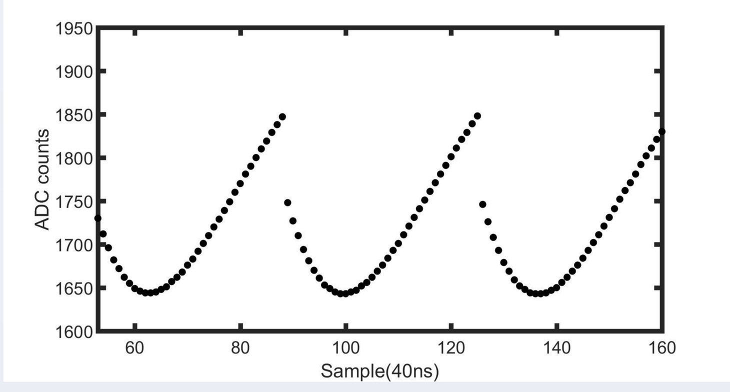

Fig. 5. Over-threshold waveforms.

4. Performances

The analog input was provided by a signal generator. By adjusting the amplitude of the input pulse to MRC, the input-output curve can be plotted, as shown in Fig. 6, and the INL is less than 3% with 5.5 pC range.

By connecting one MRC input channel to ground with a capacitor of different value to simulate the capacitor of the detector, we measured the relationship of output noise and capacitor value as shown in Fig. 7. When the equivalent capacitance is less than 100 pF, the noise is below 0.9 fC.

Fig. 8 shows the noise (RMS) distribution of 8 channels with 1 μs peaking time and 5.5 pC range in room temperature. The noise of all tested channels is less than ~1.25 fC.

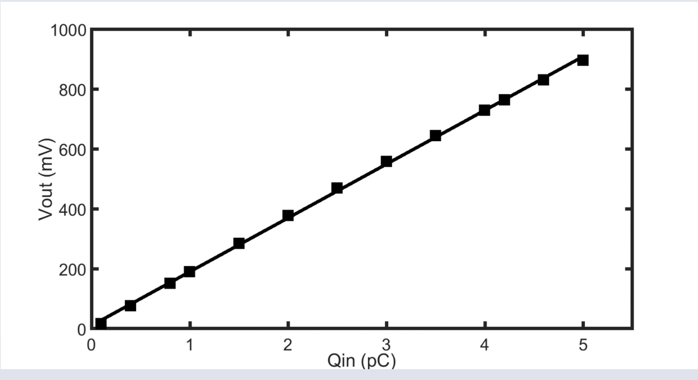

Fig. 6. Input-output curve for a typical channel.

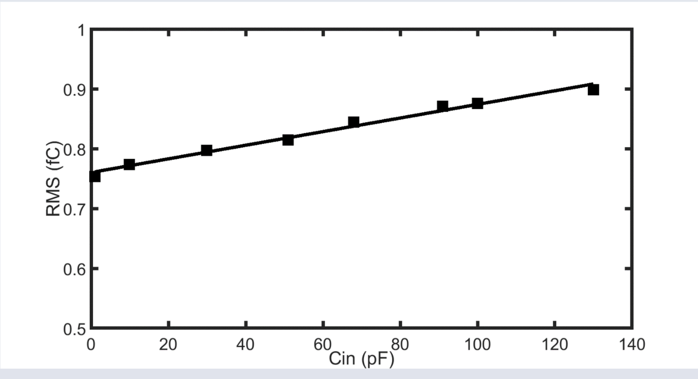

Fig. 7. Noise (RMS) vs capacitor value of a typical channel.

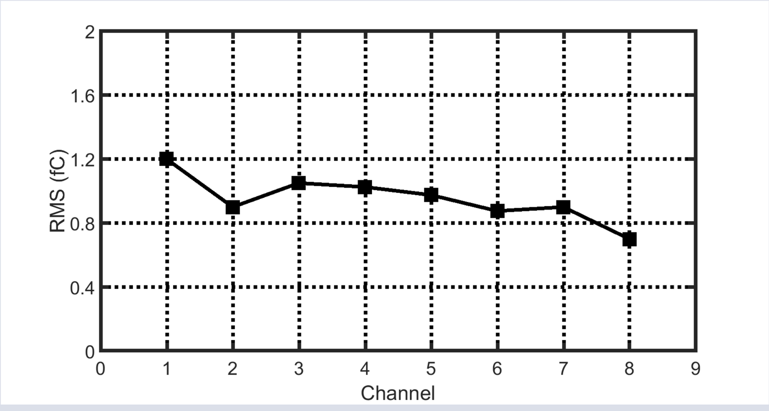

Fig. 8. Noise (RMS) distribution of 8 channels.

5. Test of Triggger Distribution

As shown in Fig. 9, MRC sends trigger signals to DCM and the trigger signals will be distributed to 4 FECs. Fig. 10 shows the trigger delay is 4.6 μs.

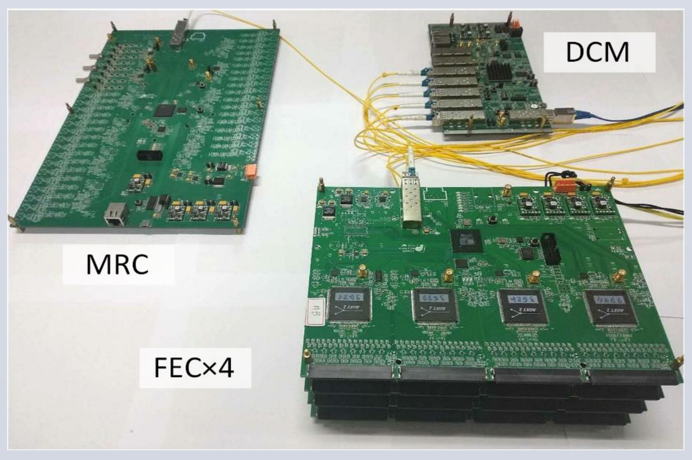

Fig. 9. Photograph of the system.

Fig.10. Trigger delay test.

6. Conclusion

The design and performances of the MRC for the PandaX-III TPC are presented in this poster. And the performances of MRC meet requirements of PandaX-III prototype TPC experiment. Trigger distribution functions well in the system test. The next plan is to conduct prototype TPC joint test by using a MRC and 4 FECs.

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21st IEEE Real Time Conference 2018