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Fixed latency fiber communication for JLAB's Hall B RICH detector

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A fixed latency Serializer-Deserializer(SerDes) is useful in detector electronics for the synchronization and triggering of data acquisition. It is not a common default feature of FPGA transceiver protocol packaging, but it can be custom built by logic in the FPGA fabric.

In this application we have a Xilinx Virtex-5 FPGA driving several GTP fiber transceivers from cards housed in a VXS crate talking to readout boards local to the detector, each hosting a Xilinx Artix-7. This communication runs a 16 bit bus at 125Mhz with a 2.5Gbps line rate.

The transceiver IP cores available on Xilinx parts utilize elastic buffers for various purposes. In order to achieve a fixed latency these buffers must be removed and replaced with custom firmware protocols for communication and link monitoring.

This custom firmware must ensure a stable link on startup, reset or power cycle, and maintain integrity. This includes clock management, word alignment, loss of sync detection, and initial phase alignment.

Description

FPGA SerDes

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Minioral

Yes

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