Preliminary Design of Integrated Digitizer Base for Photomultiplier Tube

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Outline

1. Motivation: Why we design the integrated digitizer base for PMT

   Miniaturization and distribution requirements in physical experiments

2. The design of the integrated digitizer base

   Mechanical / Hardware / Firmware / Software design

3. Application: interfaced with a CLYC (Cs$_2$LiYCl$_6$) scintillator

   Experiment setup and results (PSD figure of merit & energy res. & linearity)

4. Summary and the future work

   Different ADCs for CLYC with PMT

   Preamplifiers and ADCs adapt to the other system

   Clock synchronization based on IEEE 1588 and Synchronized Ethernet
1. Why we design the integrated digitizer base for PMT

- **JUNO** (Jiangmen Underground Neutrino Observatory) will consist of 20,000 tons of liquid scintillator, now surrounded by approximately 43,000 PMTs.
  
  Reference: A. Giaz, Status and perspectives of the JUNO experiment, [arXiv: 1804.03575]

- The **Super-Kamiokande neutrino detection** (mounts more than 11,000 20-inch PMTs)

- The **low-energy neutrino experiment** is planned at CJPL (China Jinping Underground Laboratory). A kiloton scale neutrino detector using the slow liquid scintillator will be deployed.

- The **EJ-335 liquid scintillator** doped with 0.5% gadolinium and deployed in CJPL for the fast neutron background measurement.

1. Why we design the integrated digitizer base for PMT

**Method 1:** Pulse shape discrimination

- Fast (Current Sensitive) Preamplifier
- Charge Sensitive Preamplifier
- Digitizer
- PMT with socket
- Multichannel pulse amplitude analyzer

**Method 2:** Energy Spectrometer Measurement

- CAT-5 Cable
  - Power supply > 10 W
  - Data throughput > 700 Mbps
  - Synchronized precision ~ 50 ns (in theory)

- 50 ohm RF Cable (SYV-50-7-1)
  - Stray capacitances:
    - ~1.0 pF / mm
    - (~2.54 pF / inch)

- Ø = 74 mm (~2.9 inches)
- Weight: 300 g

- Ø = 86 mm (~3.4 inches)
- Weight: 600 g
2. The design of the integrated digitizer base

2.1 Mechanical design
2. The design of the integrated digitizer base

2.2 Hardware design

- High voltage power supply
- Current sensitive preamplifier
- ADC subsystem (No. 1)
  - 500 MSPS
  - 12 bit
- ADC subsystem (No. 2)
  - 1 GSPS
  - 8 bit
- ADC subsystem (No. 3)
  - 1 GSPS
  - 12 bit
- ZYNQ readout module and its carrier
- PoE power management
- User interface
2. The design of the integrated digitizer base

2.2 Hardware design

High voltage power supply

Current sensitive preamplifier

ADC subsystem (No. 1)
500 MSPS 12 bit

ADC subsystem (No. 2)
1 GSPS 8 bit

Board-to-Board Connectors:
FX23 series from Hirose

Current-sensitive preamplifier

MezzoStak

ADC subsystem (No. 3)
1 GSPS 12 bit

ZYNQ readout module and its carrier

PoE power management

User interface

Board-to-Board Connectors:
FX23 series from Hirose
2. The design of the integrated digitizer base

2.2 Hardware design (Current Sensitive Preamplifier)

The rise time distribution under the moderated $^{252}$Cf source. It is measured by an oscilloscope (WaveRunner 8408, 4 GHz BW), which is connected with Anode output directly, coupled with DC 50 ohm.

Rise time × Bandwidth (BW) = 0.35
BW < 70 MHz

This frequency response is from Pspice Simulation, OPA657 (with 1.6 GHz GBP) is used as Transimpedance Amplifier (Current sensitive Amplifier);

$\frac{1}{2\pi R_F C_F} = \frac{1.6 \text{ GHz}}{2\pi \times 1 \text{k}\Omega \times 51.5 \text{ pF}} \approx 70.32 \text{ MHz}$

Counts

\begin{table}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline
Counts & 0 & 50 & 100 & 150 & 200 & 250 \\
\hline
Frequency (MHz) & 1 & 10 & 100 & 1000 \\
\hline
\end{tabular}
\end{table}

\[ f_{-3dB} = \sqrt{\frac{\text{GBP}}{2\pi R_F C_S}} = \sqrt{\frac{1.6 \text{ GHz}}{2\pi \times 1 \text{k}\Omega \times 51.5 \text{ pF}}} \approx 70.32 \text{ MHz} \]

Measured Refer to Texas Instruments

\[ C_S = C_D + C_{CM} + C_{DIFF} \]
\[ = 46.3 + 0.7 + 4.5 \]
\[ = 51.5 \text{ pF} \]
2. The design of the integrated digitizer base

2.2 Hardware design (Power and ADC performance)

### ADC Name

<table>
<thead>
<tr>
<th>ADC Name</th>
<th>DNL / INL test (bit)</th>
<th>ENOB from ADC datasheet (bit)</th>
<th>ENOB test (bit)</th>
<th>typical power consumption (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISLA212P50 (500 MSPS 12 bit, Intersil)</td>
<td>±0.2 / ±0.8</td>
<td>11.27@30MHz</td>
<td>10.7@30MHz</td>
<td>0.823</td>
</tr>
<tr>
<td>HMCAD1511 (1 GSPS 8 bit, ADI)</td>
<td>±0.2 / ±0.6</td>
<td>7.9@125MHz</td>
<td>7.59@125MHz</td>
<td>&lt;0.71</td>
</tr>
<tr>
<td>ADC12B1G (1 GSPS 12 bit, Tsinghua)</td>
<td>±0.5 / ±2.0</td>
<td>10.1@125MHz</td>
<td>9.5@125MHz</td>
<td>&lt;0.8</td>
</tr>
</tbody>
</table>

**Power consumption (W)**

- User interface: 0.4 W
- PoE power: 1.1 W
- ZYNQ readout module: ~1.8 W
- ADC subsystem: ~1.6 W
- Current sensitive...: 0.4 W
- high voltage supply: 0.3 W

**Power consumption (~5.6 W in total)**

![Graph showing PoE power supply efficiency and ripple](image)

The Power efficiency is tested by the DC electronic load (IT8512), and the ripple is measured by an oscilloscope (Tek. MDO4104B-3).
2. The design of the integrated digitizer base

2.3 Firmware design (ZYNQ SoC)

PL: Artix-7 FPGA

Programmable Logic (PL)

Processor System (PS)

| Logic CDMA |
| AXI BRAM Controller |
| AXI BRAM Controller |
| BRAM |
| BRAM |

Data Package (Event Time, Channel, Event no., etc.)

AXI bus

Ring Buffer using True Dual-Port RAM (64-bit width, 1k depth)

Threshold_start

Begin

Event timestamp

waveform_data

count_front

count_back

End

Threshold_stop

4 channel 64-Bit High Performance AXI bus

Up to 200 MHz

More than 700 Mbps TCP/IP Data Stream throughput

Readout Module Based on XC7Z010 or XC7Z020 - CLG400

Utilization (%)
2. The design of the integrated digitizer base
2.4 Software design

ZYNQ PS Embedded Linux (C / C++)

1. Connection established.
The software design includes the development of the application program (client) in Embedded Linux running on the ZYNQ SoC and a program (remoted server) running on Ubuntu Linux or another platform.

2. Parameter configured.
After establishment, the server will read the configuration file, including trigger threshold, length of waveform record, DAC tuning output, and pulse polarity.

3. Triggering and read out.
Waveform data over threshold will be buffered into BRAM 1 at first. When BRAM 1 is full (64 KB size), it will be disabled and BRAM 2 will be enabled. Then, CDMA will transfer BRAM 1 data from PL to PS.

The average CPU usage of the embedded linux on ZYNQ SoC is \(~10\%\).
3. Application: interfaced with a CLYC scintillator

3.1 Experiment setup & 3.2 Results

- CLYC (95% $^6$Li) Ø 25.4mm x 25.4mm hgt.
- Polyethylene
- PMT Hamamatsu 2” Type R6231-100
- Cf-252 9000 Bq

![Diagram of experiment setup with CLYC scintillator interfaced with a PMT.]

- CLYC response (Counts / s) with Moderator (5 cm PE)
- CLYC response (Counts / s) No Moderator
- Thermal neutron (< 1 eV)
- Fast neutron (>1 eV)

![Graph showing PSD ratio vs. Energy (keV).]

- Fast neutron $^{35}$Cl(n,p)$^{35}$S or $^{35}$Cl(n,α)$^{32}$P
- Mainly from thermal neutron $^6$Li(n,α)t
- Gamma ray

![Graph showing PSD ratio vs. Time (ns).]

- Neutron (No. of events: 17006, ratio: 37%)
- Gamma (No. of events: 28371, ratio: 61.7%)
- Noise (No. of events: 623, ratio: 1.35%)

$$PSD\ ratio = \frac{Q_L}{Q_S + Q_L}$$
3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis

The thermal neutrons are detected from $^6$Li(n,α)t reaction, and the fast neutrons from either the $^{35}$Cl(n,p)$^{35}$S or $^{35}$Cl(n,α)$^{32}$P reaction.

$^6$Li (95% enrichment) has a thermal neutron capture cross section of 940 barns and a Gamma Equivalent Energy (GEE) of 3.2 MeV approximately.

For the whole recorded pulse of the neutron and gamma-ray, the PSD FoM is ~3.0.

FoM = \frac{\mu_{\text{neutron}} - \mu_{\text{gamma}}}{FWHM_{\text{neutron}} + FWHM_{\gamma}}
3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis

The fitting results of decay:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Particle</th>
<th>CVL (ns)</th>
<th>Ce³⁺ (ns)</th>
<th>Vₖ (ns)</th>
<th>STE (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>Gamma-ray</td>
<td>49</td>
<td>668</td>
<td>1141</td>
<td>5929</td>
</tr>
<tr>
<td></td>
<td>Neutron</td>
<td>-</td>
<td>599</td>
<td>1339</td>
<td>6173</td>
</tr>
<tr>
<td></td>
<td>Neutron</td>
<td>-</td>
<td>490</td>
<td>1420</td>
<td>6300</td>
</tr>
<tr>
<td>[17]</td>
<td>Gamma-ray</td>
<td>2</td>
<td>50</td>
<td>420</td>
<td>3400</td>
</tr>
<tr>
<td></td>
<td>Neutron</td>
<td>-</td>
<td>-</td>
<td>390</td>
<td>1500</td>
</tr>
</tbody>
</table>

[17] K. Li, X. Zhang, Q. Gui, P. Jin, G. Tian, "Characterization of the new scintillator Cs₂LiYCl₆:Ce³⁺

- Four mechanisms are included:
  - direct electron-hole capture (Ce³⁺)
  - binary Vₖ-electron diffusion (Vₖ)
  - self-trapped exciton (STE) emission
  - core-valence luminescence (CVL)

- The fitting differences may be caused by the different signal sampling rate or the Ce³⁺ doping concentration.
3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis

Hypothesis:
The pulse energy will be collected completely if the integral time is 20 μs (more than 3 times of STE decay).

Use 40,000 pulse events.

\[ \gamma_{\text{neutron}} = 0.40 e^{-\frac{t}{590}} + 0.21 e^{-\frac{t}{1339}} + 0.41 e^{-\frac{t}{6173}} \]

\[ \gamma_{\text{gamma}} = 0.53 e^{-\frac{t}{49}} + 0.20 e^{-\frac{t}{668}} + 0.07 e^{-\frac{t}{1141}} + 0.18 e^{-\frac{t}{5929}} \]
3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis

- The 20-μs integral length is used to obtain the pulse energy.
- The energy calibration is done by the linear fitting and the GEE of the thermal neutron is estimated to be ~3180 keV.
- The correlation coefficient $R^2$ is better than 0.9999.
4. Summary and the future work

4.1 Summary

- **Design**
  - This integrated digitizer base is designed for various applications with PMTs coupled with different detectors.
  - A single category-5 cable is used for **power supply and data transmission**. The power consumption of the total system is ~5.6 W. A 70 MHz bandwidth preamplifier, 500 MSPS 12-bit ADC board, and a readout module based ZYNQ SoC are designed.

- **Application**
  - The integrated digitizer PMT base is tested with a CLYC scintillator.
  - The **PSD method** is used to discriminate between the neutron, gamma-ray, and noise. The decay of the pulse shape of the normalized neutron and gamma-ray is fitted by several exponential formulas.
  - We assume that the **total energy** is collected by a pulse integral of 20 μs, which is more than 3 times the STE (~6 μs). A 12-μs pulse integral can obtain more than 90% of the total energy and the energy resolution is better than 5% at 662 keV. The linearity is better than 0.9999 from 122 keV to ~3.2 MeV.
  - The **PSD FoM** is ~3.0 for the whole recorded pulse of the neutron and gamma-ray.
4. Summary and the future work

4.2 The future work

- **Different ADC subsystems**
  ADCs with different sampling speeds and vertical resolution will be used in this integrated digitizer base. The influences due to sampling speeds, resolution of ADC, the integral length on PSD FoM, and energy resolution will be analyzed.

<table>
<thead>
<tr>
<th>ADC subsystem (No. 1, this work)</th>
<th>ADC subsystem (No. 2)</th>
<th>ADC subsystem (No. 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 MSPS  12 bit</td>
<td>1 GSPS  8 bit</td>
<td>1 GSPS  12 bit</td>
</tr>
</tbody>
</table>

- **Other detectors**
  This integrated digitizer base will also be interfaced with the liquid scintillator with the dual R5912-02 PMTs from Hamamatsu. It is a neutron detector deployed in CJPL (China Jinping Underground Laboratory) for neutron background measurement.
4. Summary and the future work

4.2 The future work

- Clock synchronization based on IEEE 1588 and Synchronized Ethernets

A commercial IEEE 1588 grandmaster is used to generate precise timestamp to every slave node while a commercial Ethernet switch with IEEE 1588 support is used.

With the SyncE capability, the recovered clock from Ethernet PHY chip is used for input of dedicated PLL to generate the clock of logic unit implemented in the programmable logic of ZYNQ SoC of the integrated PMT base.

About 50 ns accuracy clock will be realized and it is adequate for the neutron gamma discrimination application, which needs several microseconds coincident requirement.
Thank you!
Physics

- The **low-energy neutrino experiment (in plan)** at CJPL (China Jinping Underground Laboratory).

- **Goal:** This project is aiming to build a **kiloton scale neutrino detector** at Jinping underground lab, using the slow liquid scintillator technology to separate prompt Cherenkov light and slow scintillation light. We hope to provide precise measurement on solar neutrinos and geo-neutrinos.

Energy res.

\[
N(\mu, \sigma^2) = N(228.6, 8.6^2)
\]

Energy resolution (%) = \[\frac{\text{FWHM}}{\mu}\]  
= \[2.355 \times \frac{\sigma}{\mu}\]  
= \[2.355 \times 8.6 / 228.6\]  
= 8.86%
Boards

Board-to-Board Connectors: FX23 series from Hirose
PoE End-Span method

Split data and power lines
The resource of utilization of PL:

<table>
<thead>
<tr>
<th>Resource</th>
<th>Utilization</th>
<th>Available</th>
<th>Utilization (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUT</td>
<td>6911</td>
<td>53200</td>
<td>12.99</td>
</tr>
<tr>
<td>LUTRAM</td>
<td>323</td>
<td>17400</td>
<td>1.86</td>
</tr>
<tr>
<td>FF</td>
<td>10238</td>
<td>106400</td>
<td>9.62</td>
</tr>
<tr>
<td>BRAM</td>
<td>36</td>
<td>140</td>
<td>25.71</td>
</tr>
<tr>
<td>IO</td>
<td>41</td>
<td>125</td>
<td>32.80</td>
</tr>
<tr>
<td>BUFG</td>
<td>7</td>
<td>32</td>
<td>21.88</td>
</tr>
<tr>
<td>PLL</td>
<td>1</td>
<td>4</td>
<td>25.00</td>
</tr>
</tbody>
</table>

Board of current sensitive preamplifier
- Amplifier
- PMT signal
- PMT Socket
- Board of ADC subsystem
  - RF switch
  - Buffer
  - Amplifier
  - Diff Amplifier
    - ADC (500MSPS 12-bit)
    - VOCM
    - 500MHz Diff clock
    - 100MHz
  - DAC
    - ADF4360-7
  - VCO
    - Crystal Oscillator
    - ADF4360-7
    - SPI
  - SPI
- Board of ZYNQ SoC and its carrier
  - Readout Module Based on XC7Z010 or XC7Z020 - CLG400
  - ZYNQ
  - Programmable Logic FPGA
    - Up to 200 MHz
  - Dual Cortex-A9 866 MHz
- Board of PoE power management
  - PoE power management
  - Ethernet Transformer
  - Cable
- Test pulse
  - User Interface (contain MCU)
- HV control
- Board of User Interface
- PoE power management
- Ethernet Transformer
- Cable
- User Interface

External DDR Memory
- M0
- S0
- M1
- S1
- M2
- S2
- M3
- S3
- FIFO
- FIFO
- FIFO
- FIFO
- SPI
- FCLK0
- M_GP0
- S_HP0
- PS
- DDR Memory Controller
- BRAM 1
- Logic CDMA
- BRAM 2
- AXI Interconnect
- AXI BRAM Controller 1
- AXI BRAM Controller 2
- 84-Bit
- 32-Bit

Total structure
IEEE802.3af -> IEEE802.3at (PoE plus)

<table>
<thead>
<tr>
<th>Feature/standard</th>
<th>802.3af (802.3at type 1)</th>
<th>802.3at type 2 (POE+)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power of power supply [W]</td>
<td>15.4</td>
<td>30.00*</td>
</tr>
<tr>
<td>Minimum power available for the powered</td>
<td>12.95</td>
<td>25.5*</td>
</tr>
<tr>
<td>device [W]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage of power supply [V]</td>
<td>44...57</td>
<td>50...57</td>
</tr>
<tr>
<td>Supplying voltage available at the powered</td>
<td>37...57</td>
<td>42.5...57</td>
</tr>
<tr>
<td>device [V]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max current [mA]</td>
<td>350</td>
<td>600</td>
</tr>
<tr>
<td>Ethernet compatibility</td>
<td>10BASE-T, 100BASE-TX and 1000BASE-T</td>
<td>10BASE-T, 100BASE-TX and 1000BASE-T</td>
</tr>
<tr>
<td>Range [m]</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Cabling</td>
<td>UTP/FTP min. cat. 3</td>
<td>UTP/FTP min. cat. 5</td>
</tr>
</tbody>
</table>

Two modes, A and B, are available. PoE can also be used on 1000BASE-T Ethernet, in which case there are no spare pairs and all power is delivered using the phantom technique.
Mode A delivers power on the data pairs of 100BASE-TX or 10BASE-T.
Mode B delivers power on the spare pairs.
The range can be longer if repeaters are used.