Preliminary Design of Integrated Digitizer Base for Photomultiplier Tube

Authors: Tao Xue, Jinfu Zhu, Guanghua Gong, Liangjun Wei, Jianmin Li

Speaker: Jinfu Zhu

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Outline

1. Motivation: Why we design the integrated digitizer base for PMT

   Miniaturization and distribution requirements in physical experiments

2. The design of the integrated digitizer base

   Mechanical / Hardware / Firmware / Software design

3. Application: interfaced with a CLYC (Cs_2LiYCl_6) scintillator

   Experiment setup and results (PSD figure of merit & energy res. & linearity)

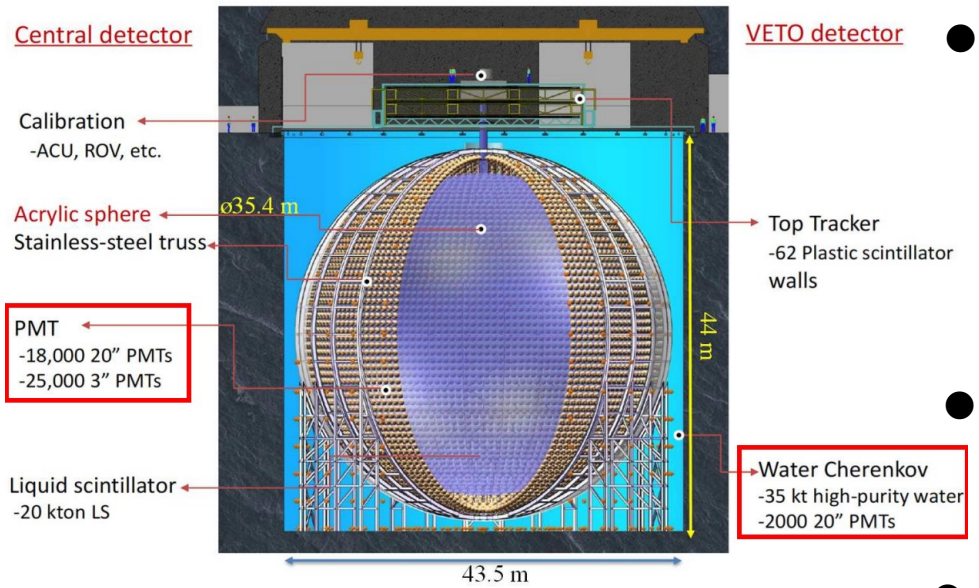
4. Summary and the future work

   Different ADCs for CLYC with PMT

   Preamplifiers and ADCs adapt to the other system

   Clock synchronization based on IEEE 1588 and Synchronized Ethernet

1. Why we design the integrated digitizer base for PMT



- JUNO (Jiangmen Underground Neutrino Observatory) will consist of 20,000 tons of liquid scintillator, now surrounded by approximately 43,000 PMTs.

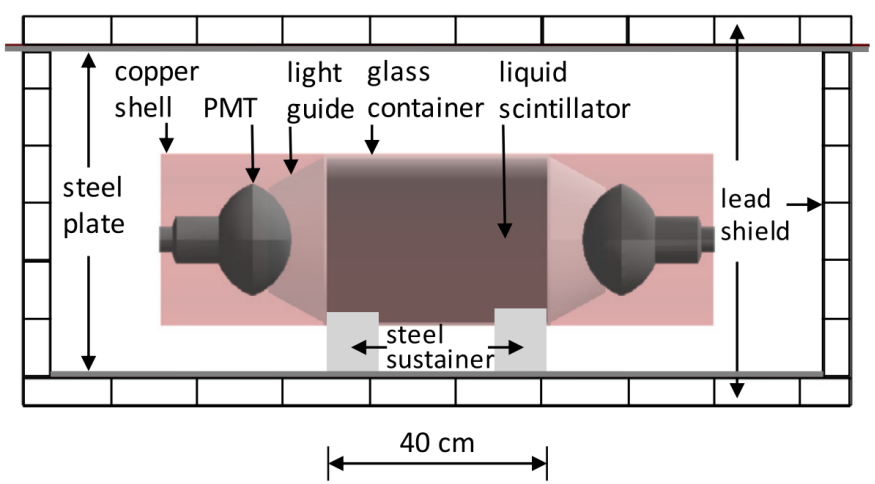
  Reference: A. Giaz, Status and perspectives of the JUNO experiment, [arXiv: 1804.03575]

- The Super-Kamiokande neutrino detection (mounts more than 11,000 20-inch PMTs) …

- The low-energy neutrino experiment is planned at CJPL (China Jinping Underground Laboratory). A kiloton scale neutrino detector using the slow liquid scintillator will be deployed.

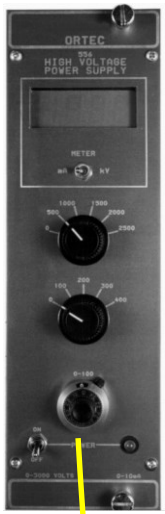
- The EJ-335 liquid scintillator doped with 0.5% gadolinium and deployed in CJPL for the fast neutron background measurement.

  Reference: Q. Du et al., Measurement of the fast neutron background at the China Jinping Underground Laboratory, Nucl. Instrum Meth. A 889 (2018) 105 [arXiv:1706.06831v2]



1. Why we design the integrated digitizer base for PMT

***Method 1**: Pulse shape discrimination*



High-Voltage Power Supply

①

Fast (Current Sensitive) Preamplifier

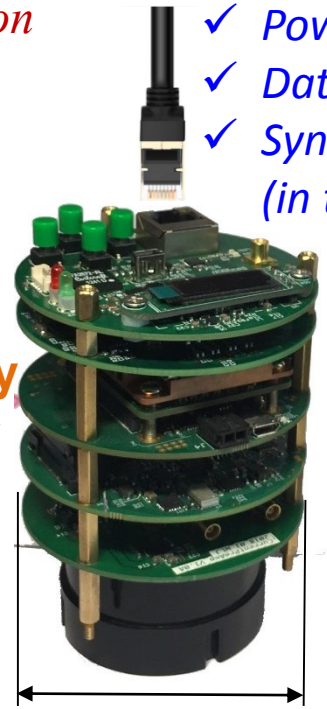
Charge Sensitive Preamplifier

Digitizer

simplify

CAT-5 Cable

- ✓ *Power supply > 10 W*
- ✓ *Data throughout > 700 Mbps*
- ✓ *Synchronized precision ~ 50 ns (in theory)*



Ø = 74 mm
(~2.9 inches)
Weight: 300 g

Ø = 86 mm
(~3.4 inches)
Weight: 600 g

PMT with socket

②

Multichannel pulse amplitude analyzer

50 ohm RF Cable (SYV-50-7-1)

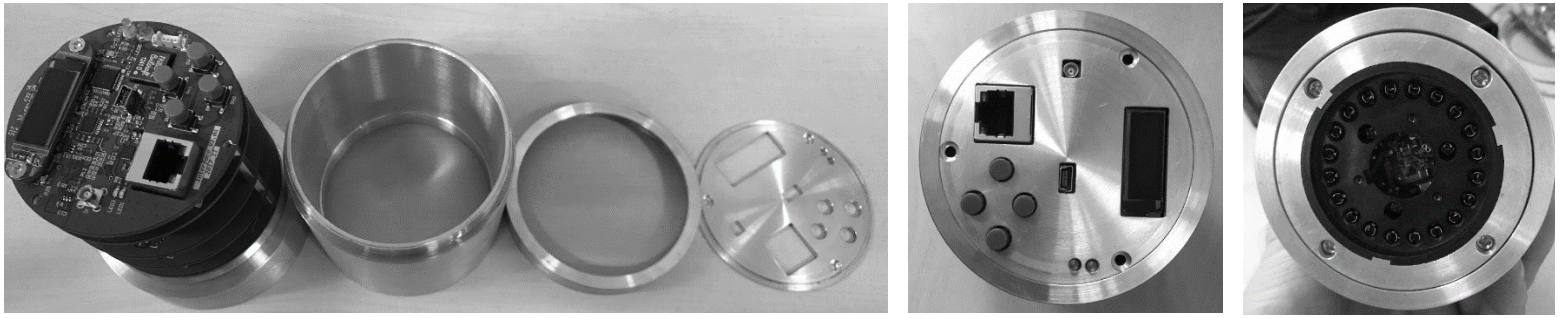
- stray capacitances:

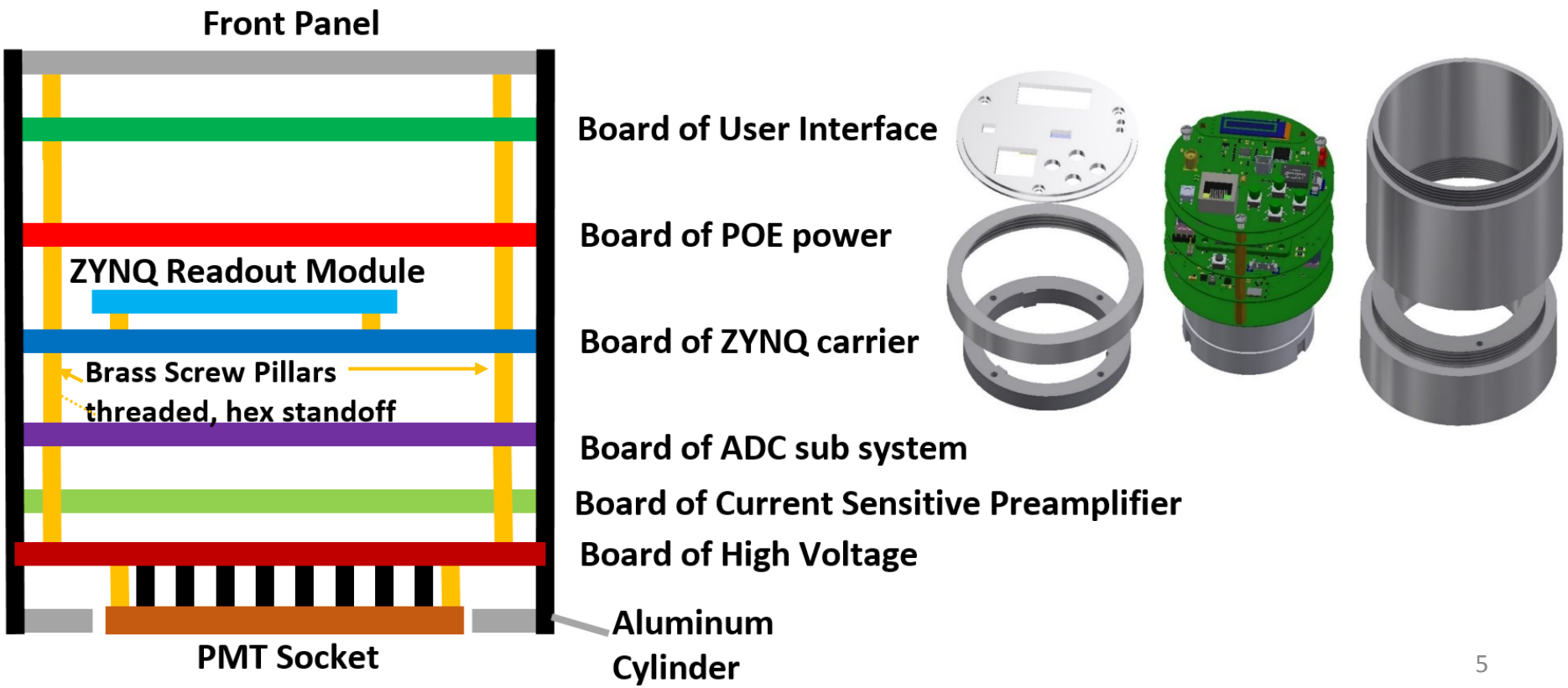
~1.0 pF / mm
(~2.54 pF / inch)

***Method 2**: Energy Spectrometer Measurement*

2. The design of the integrated digitizer base

2.1 Mechanical design

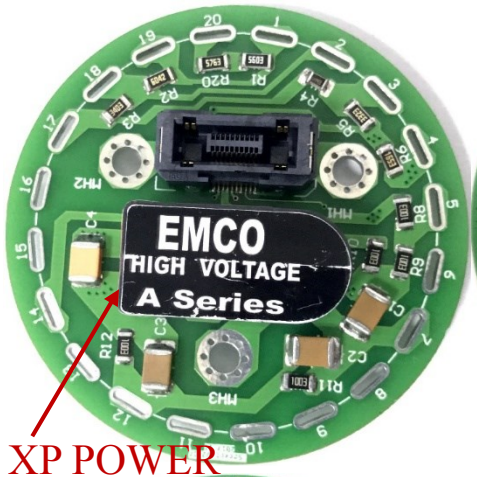




2. The design of the integrated digitizer base

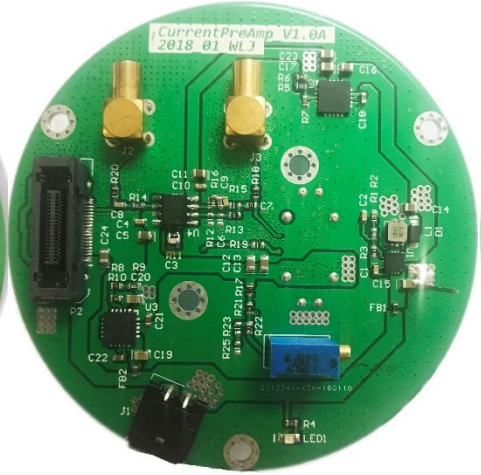
2.2 Hardware design

High voltage power supply

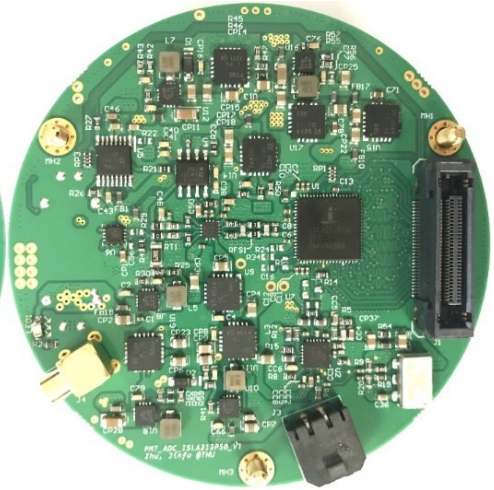


XP POWER

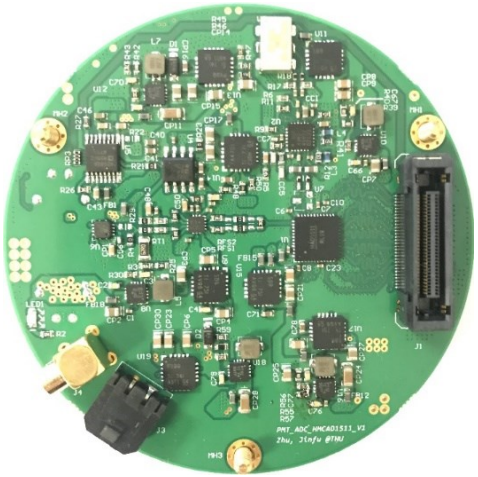
Current sensitive preamplifier

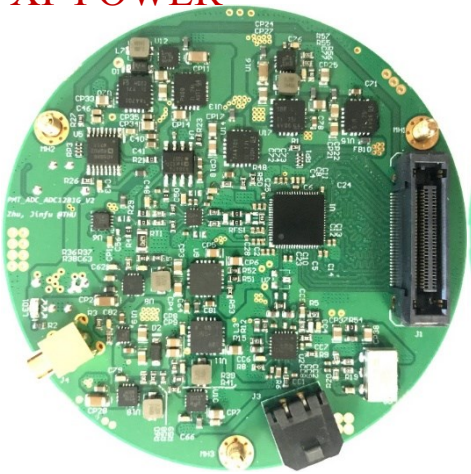


ADC subsystem *(No. 1)*
500 MSPS 12 bit

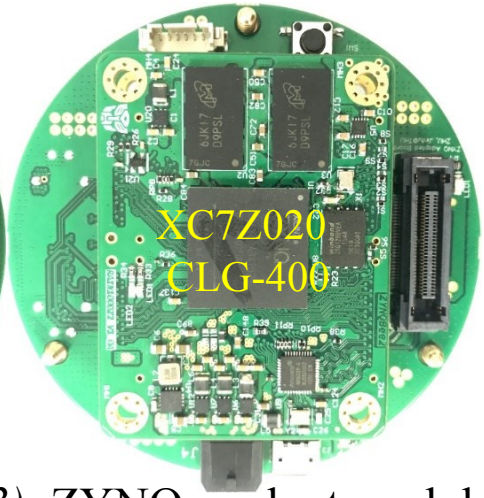


ADC subsystem *(No. 2)*
1 GSPS 8 bit





ADC subsystem *(No. 3)*
1 GSPS 12 bit



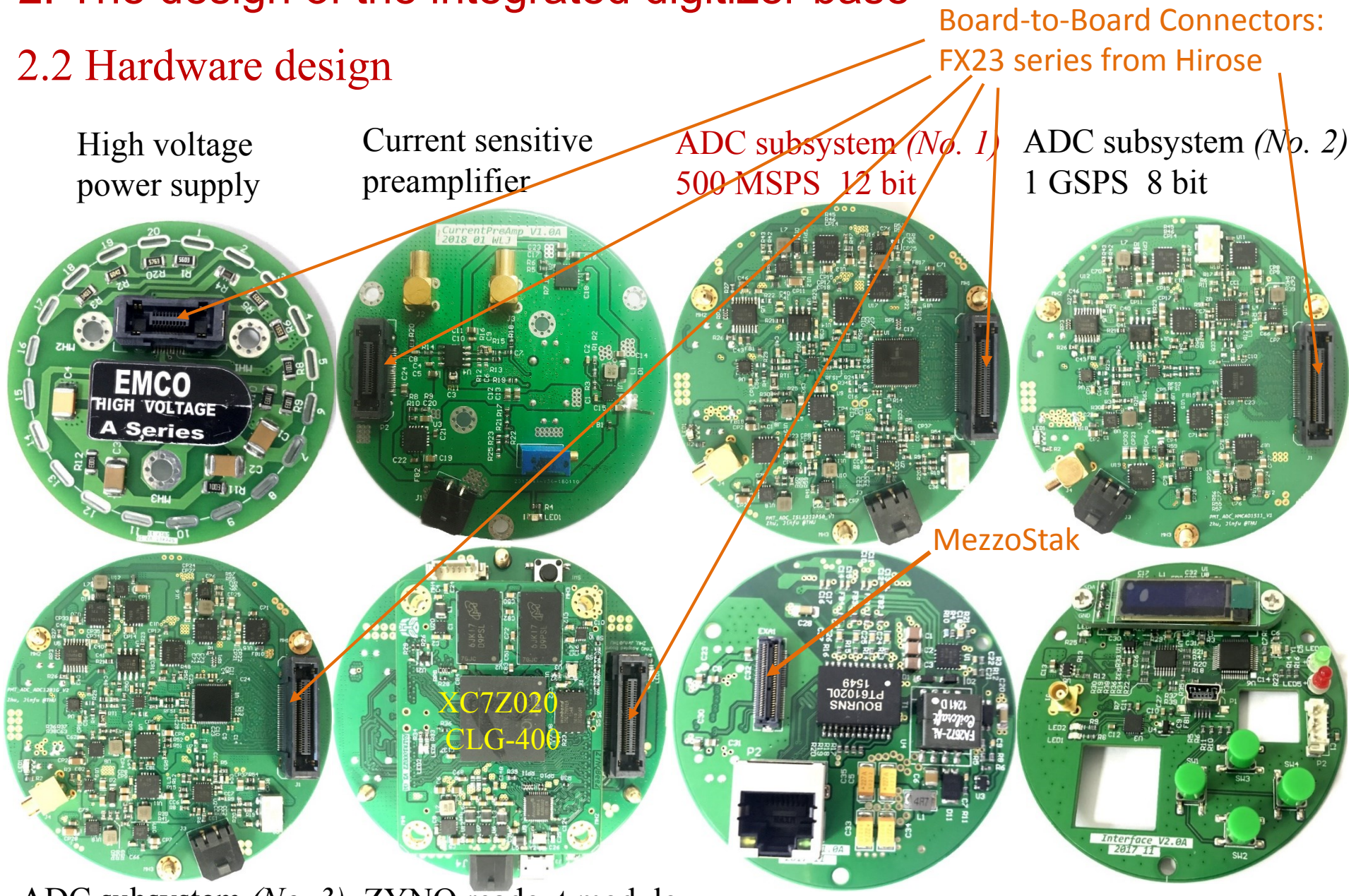
ZYNQ readout module and its carrier

PoE power management

User interface

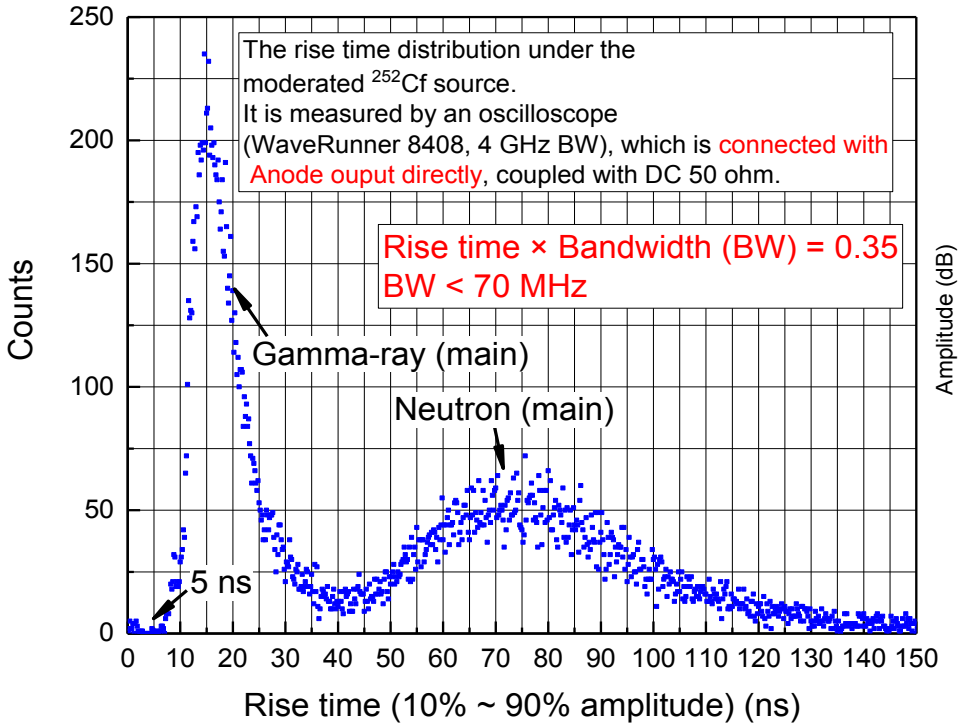
2. The design of the integrated digitizer base

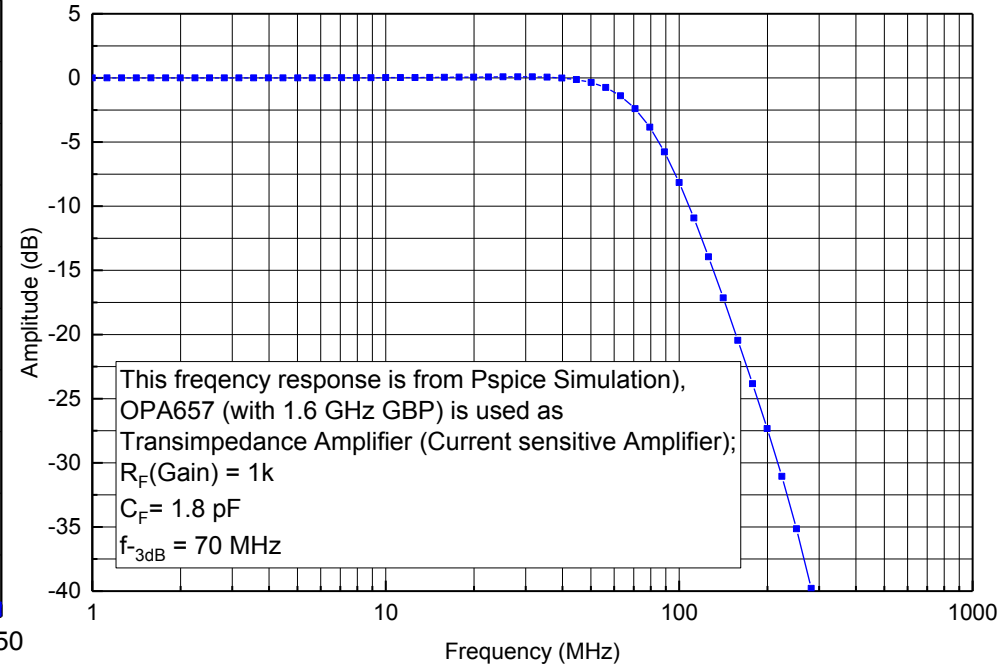
2.2 Hardware design

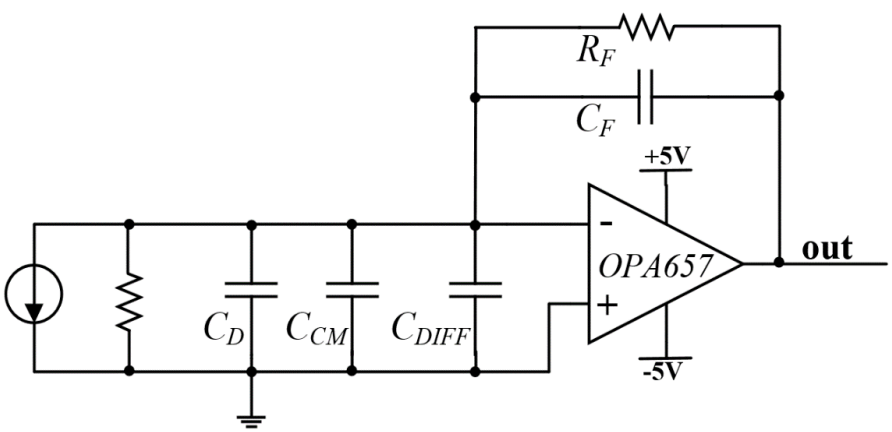


2. The design of the integrated digitizer base

2.2 Hardware design (Current Sensitive Preamplifier)







$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_S}} = \sqrt{\frac{1.6\ G}{2\pi * 1k * 51.5\ p}} \approx 70.32\ MHz$$

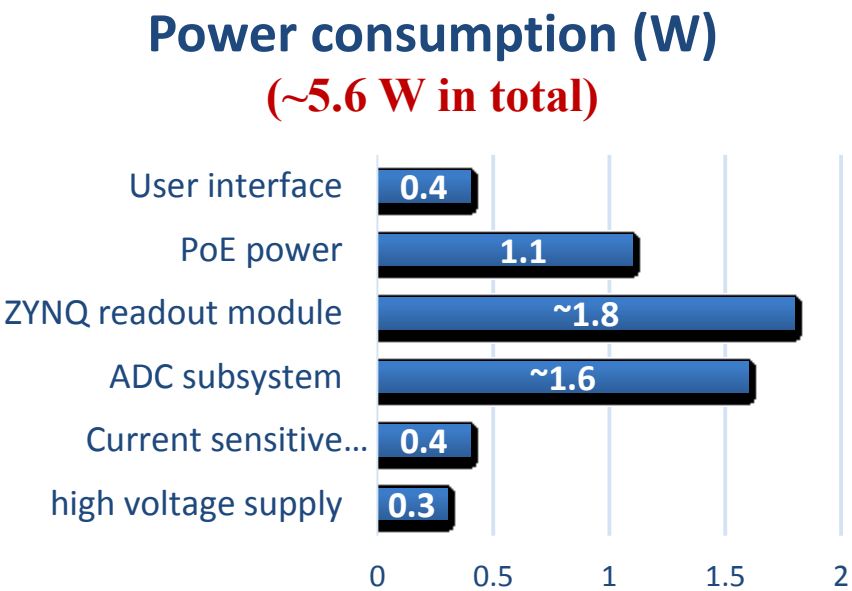
Measured Refer to Texas Instruments

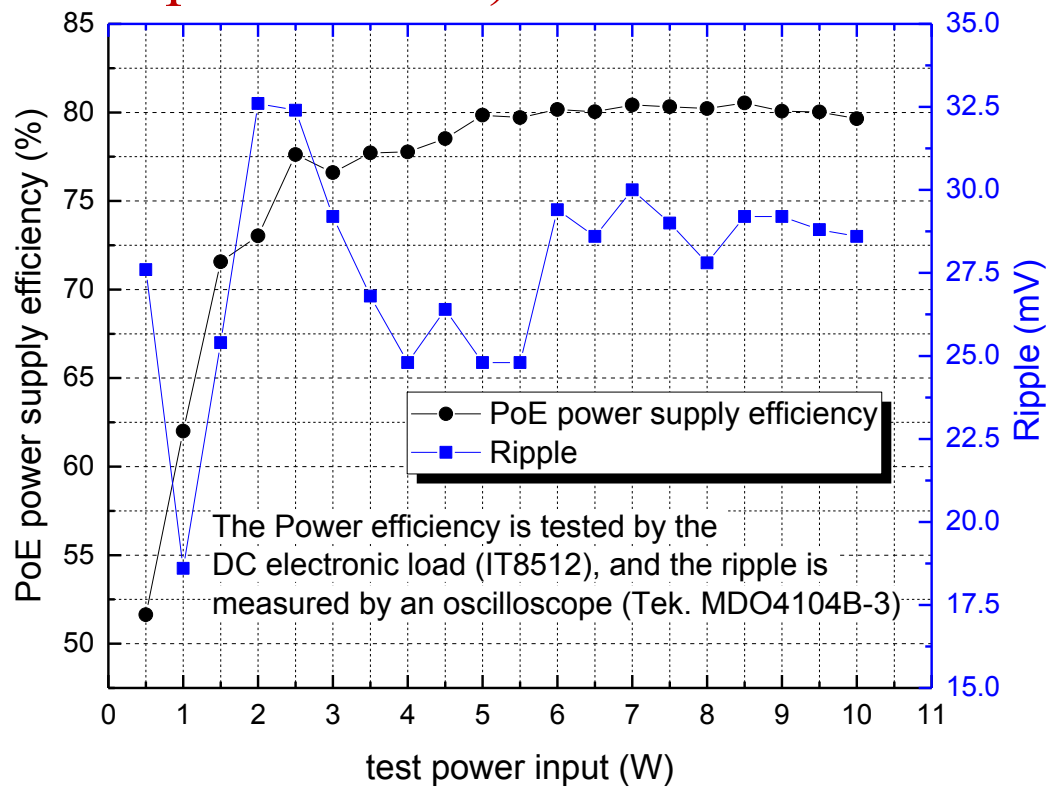
$$C_S = C_D + C_{CM} + C_{DIFF}$$
$$= 46.3 + 0.7 + 4.5$$
$$= 51.5\ pF$$

2. The design of the integrated digitizer base

2.2 Hardware design (Power and ADC performance)

Si3402 (from Silicon Labs)

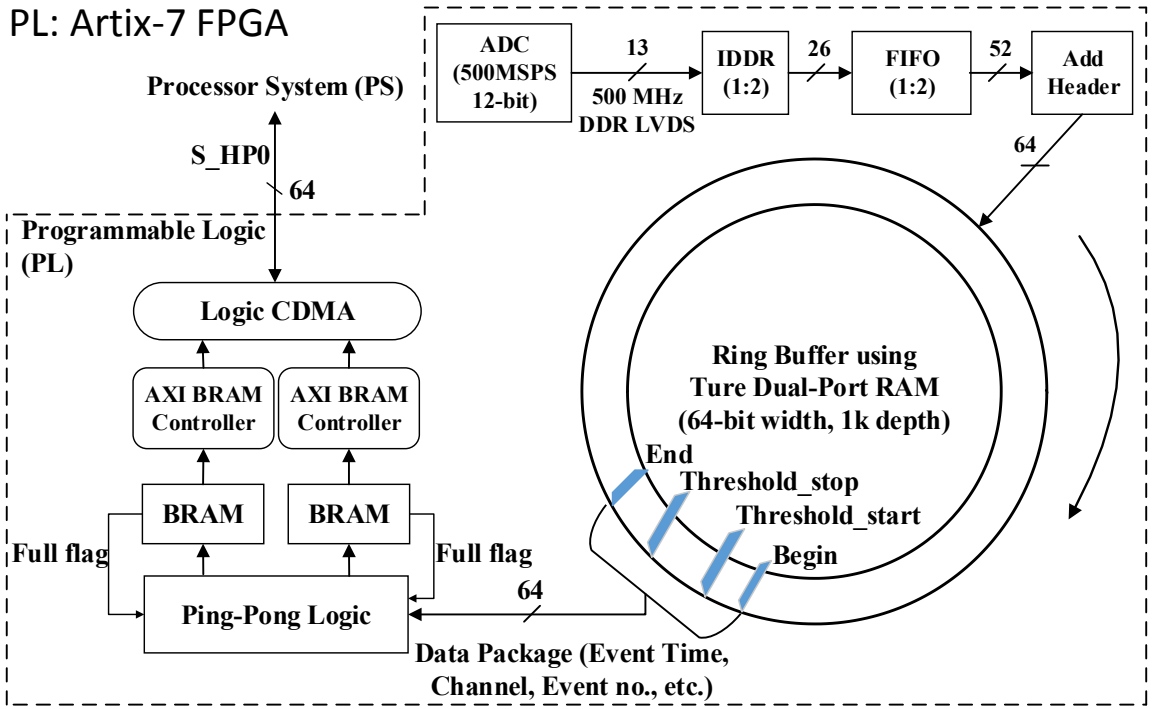


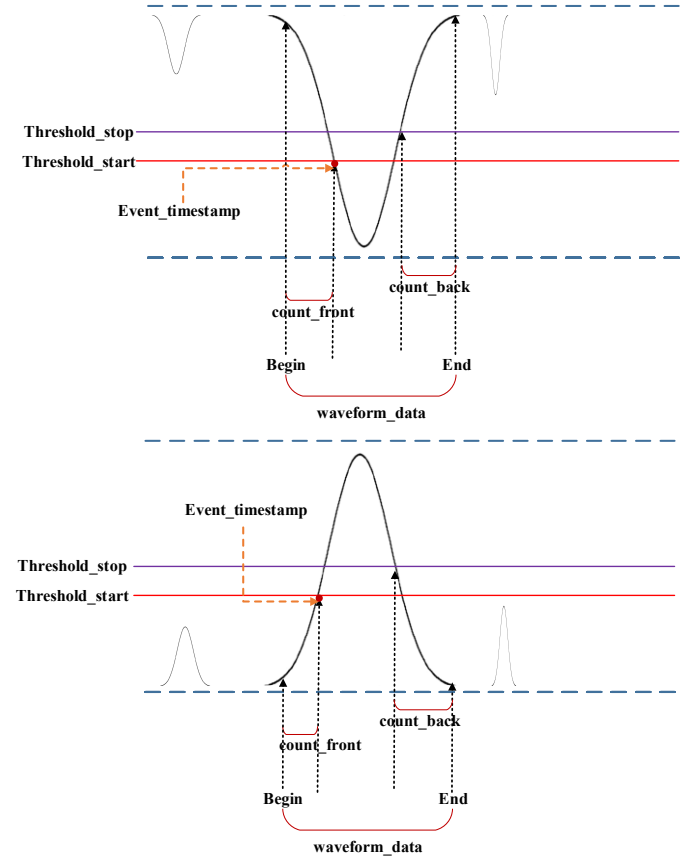


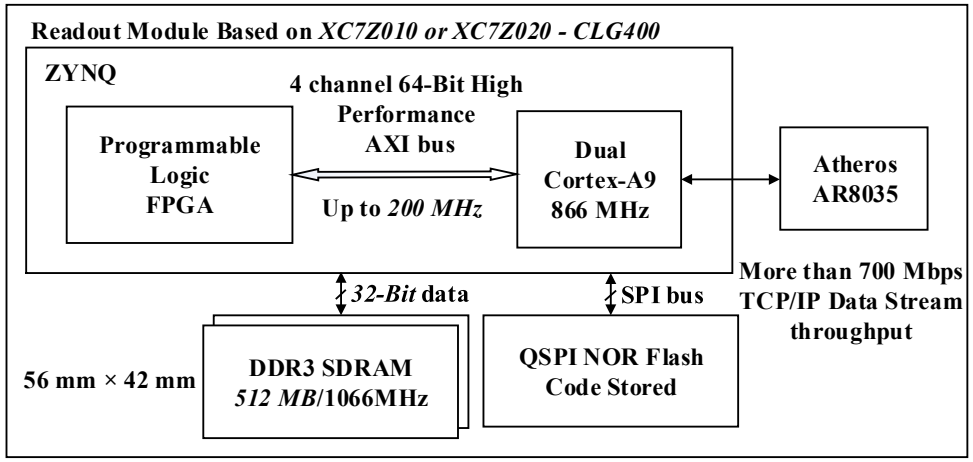
ADC Name	DNL / INL test (bit)	ENOB from ADC datasheet (bit)	ENOB test (bit)	typical power consumption (W)
ISLA212P50 (500 MSPS 12 bit, Intersil)	±0.2 / ±0.8	11.27@30MHz	10.7@30MHz	0.823
HMCAD1511 (1 GSPS 8 bit, ADI)	±0.2 / ±0.6	7.9@125MHz	7.59@125MHz	<0.71
ADC12B1G (1 GSPS 12 bit, Tsinghua)	±0.5 / ±2.0	10.1@125MHz	9.5@125MHz	< 0.8

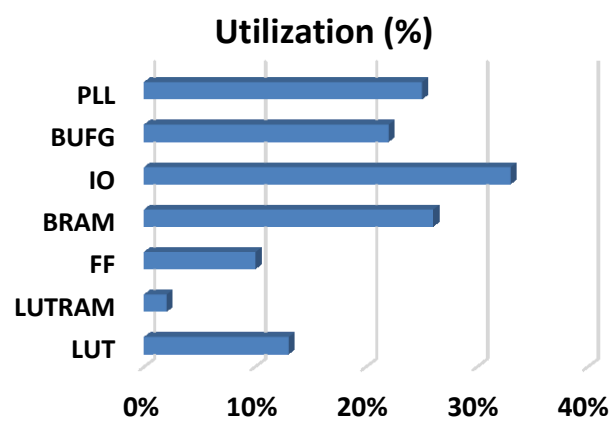
2. The design of the integrated digitizer base

2.3 Firmware design (ZYNQ SoC)



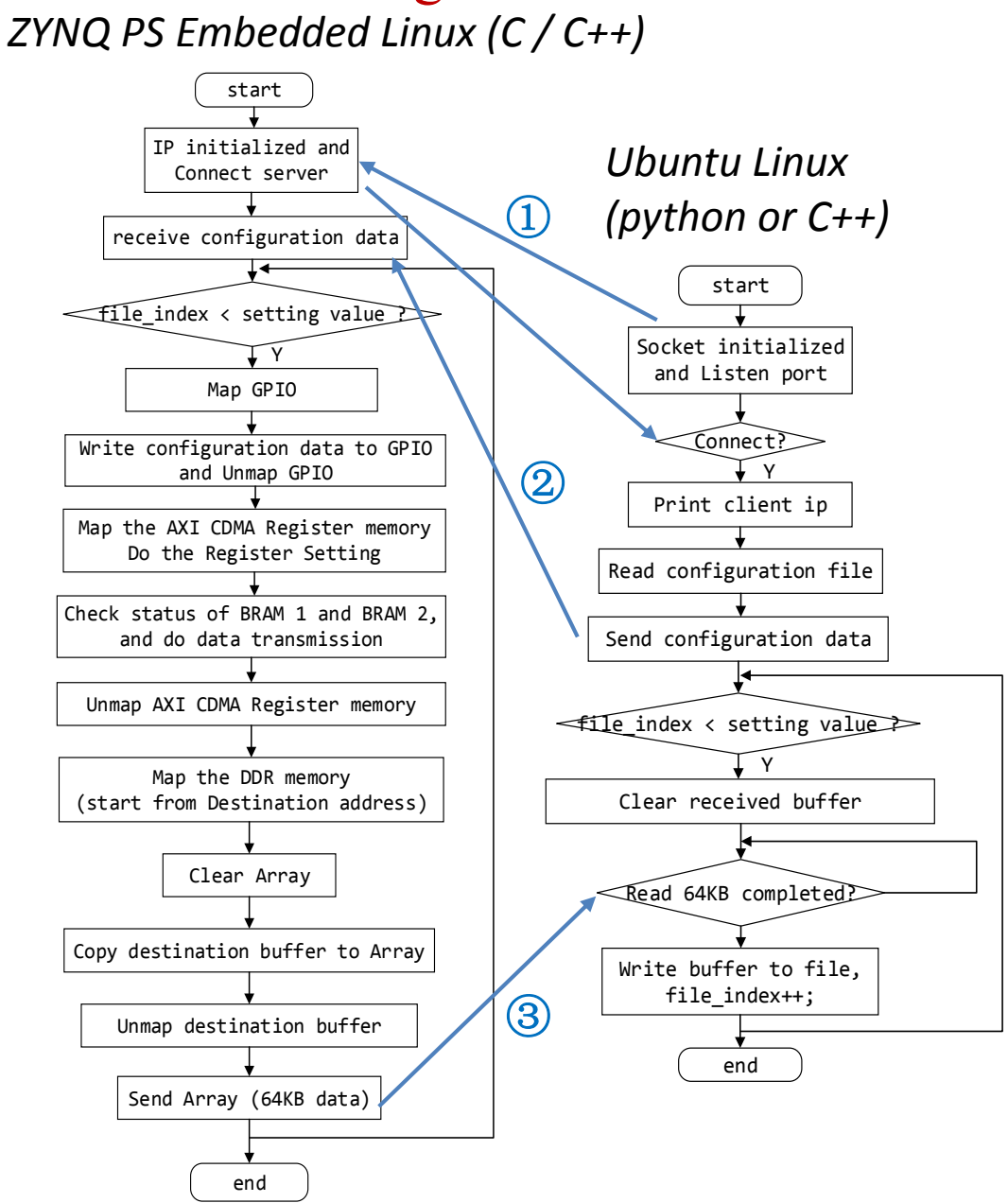






2. The design of the integrated digitizer base

2.4 Software design



1. Connection established.

The software design includes the development of the application program (client) in Embedded Linux running on the ZYNQ SoC and a program (remoted server) running on Ubuntu Linux or another platform.

2. Parameter configured.

After establishment, the server will read the configuration file, including trigger threshold, length of waveform record, DAC tuning output, and pulse polarity.

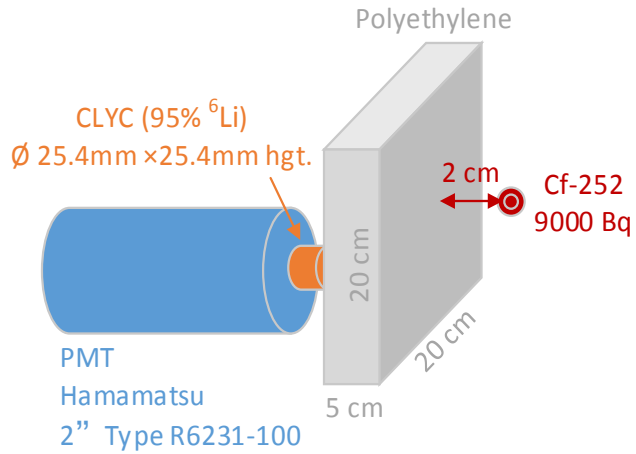
3. Triggering and read out.

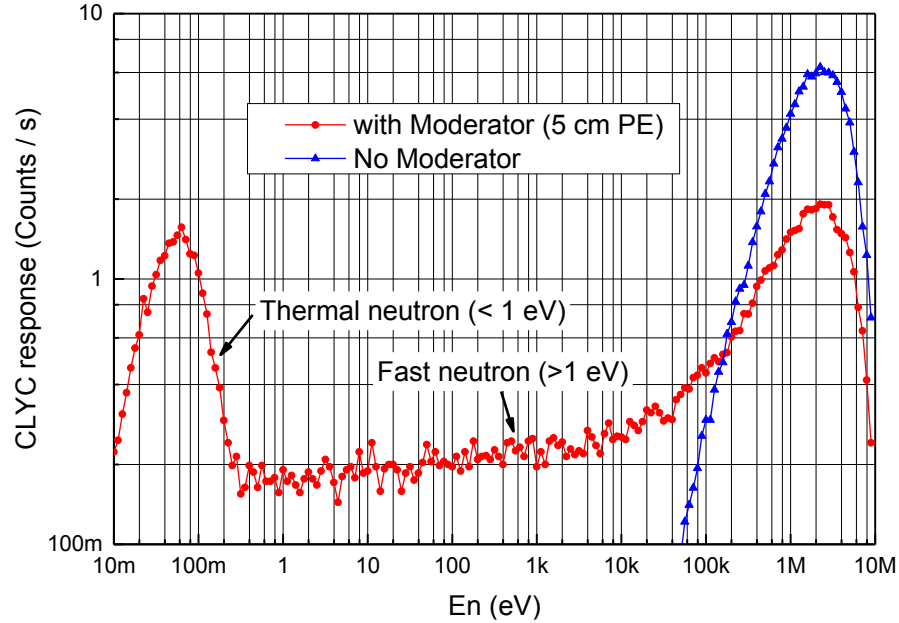
Waveform data over threshold will be buffered into BRAM 1 at first. When BRAM 1 is full (64 KB size), it will be disabled and BRAM 2 will be enabled. Then, CDMA will transfer BRAM 1 data from PL to PS.

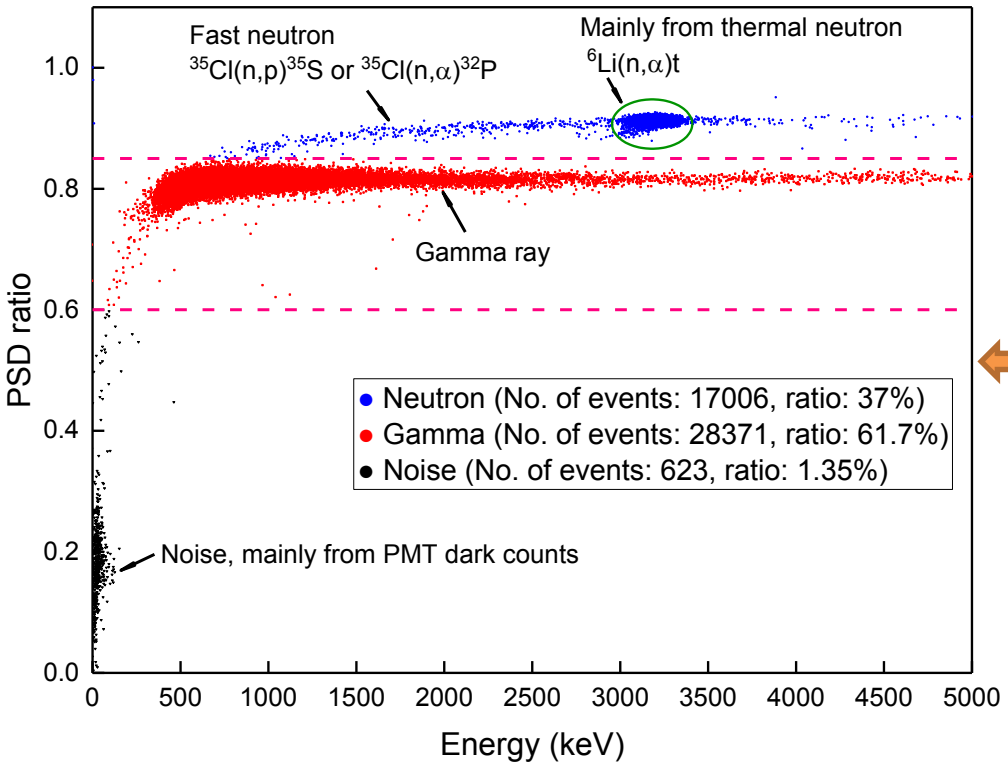
The average CPU usage of the embedded linux on ZYNQ SoC is ~10%.

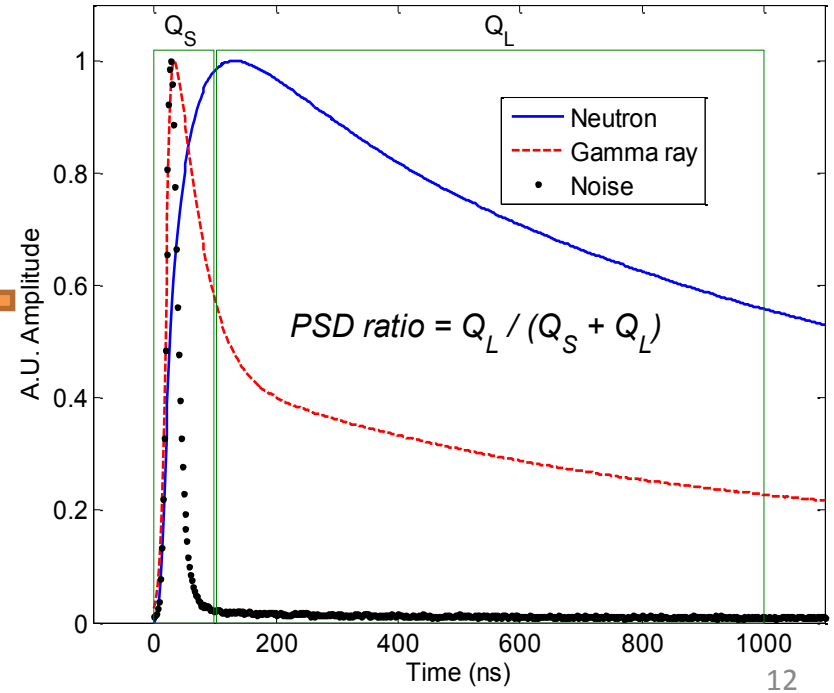
3. Application: interfaced with a CLYC scintillator

3.1 Experiment setup & 3.2 Results





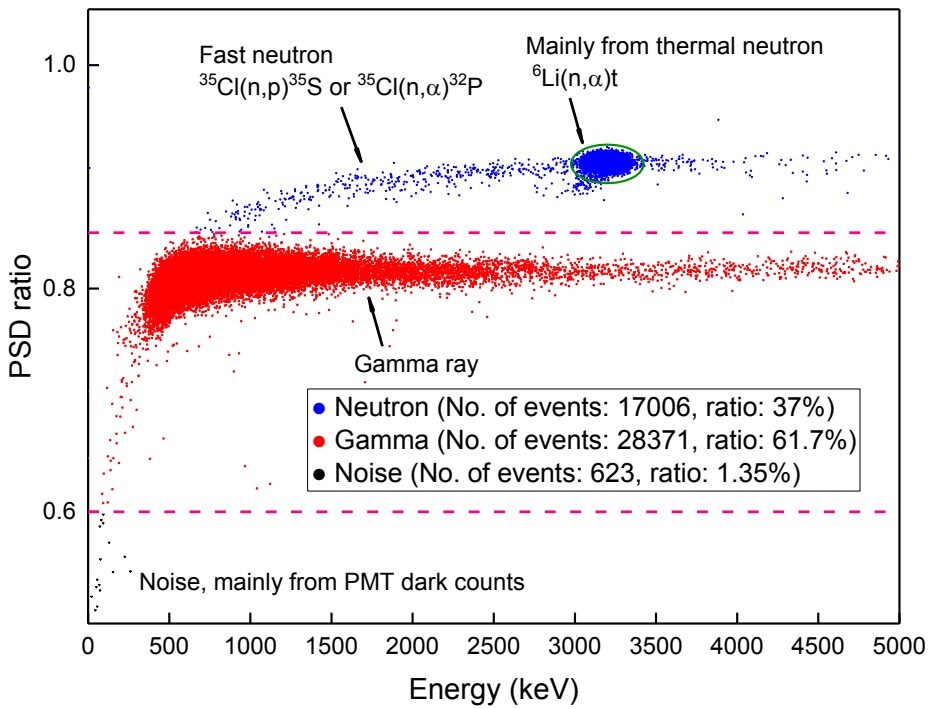


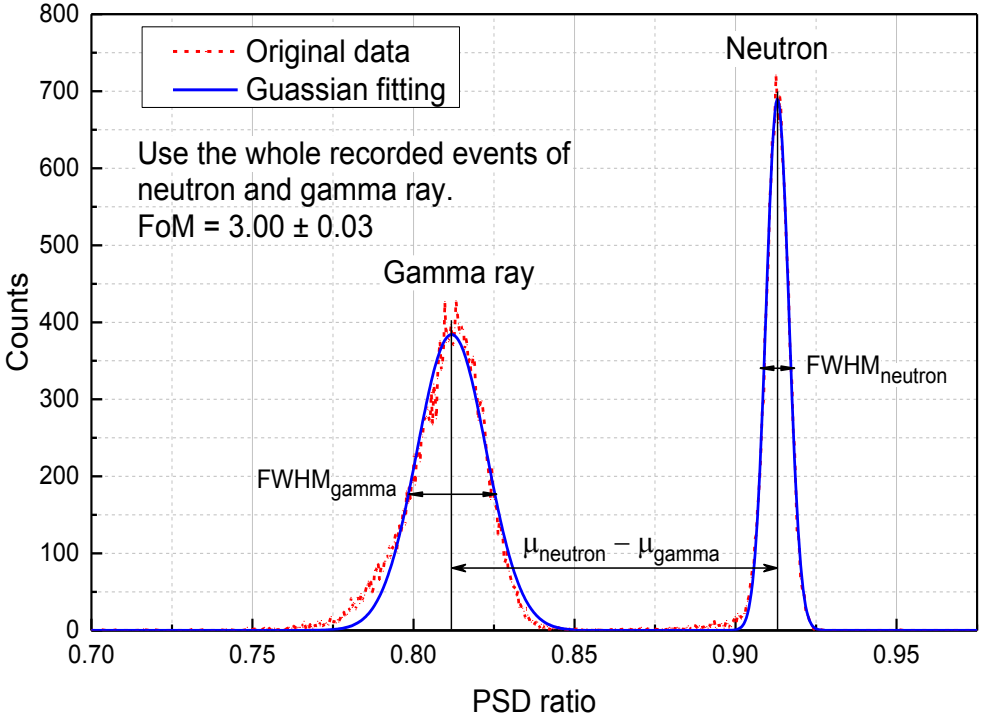


3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis

$$FoM = \frac{\mu_{neutron} - \mu_{gamma}}{FWHM_{neutron} + FWHM_{gamma}}$$

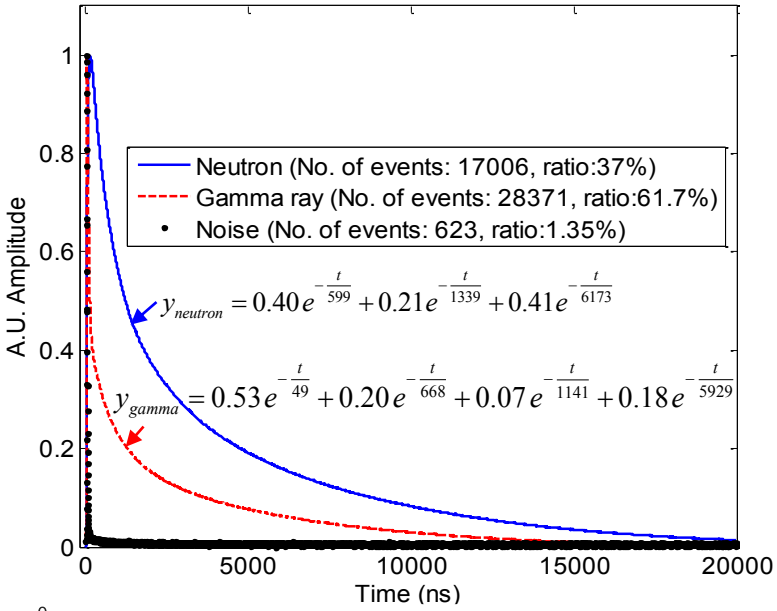




- The thermal neutrons are detected from $^{6}Li(n,\alpha)t$ reaction, and the fast neutrons from either the $^{35}Cl(n,p)^{35}S$ or the $^{35}Cl(n,\alpha)^{32}P$ reaction.
- ^{6}Li (95% enrichment) has a thermal neutron capture cross section of 940 barns and a Gamma Equivalent Energy (GEE) of 3.2 MeV approximately.
- For the whole recorded pulse of the neutron and gamma-ray, the PSD FoM is ~3.0.

3. Application: interfaced with a CLYC scintillator

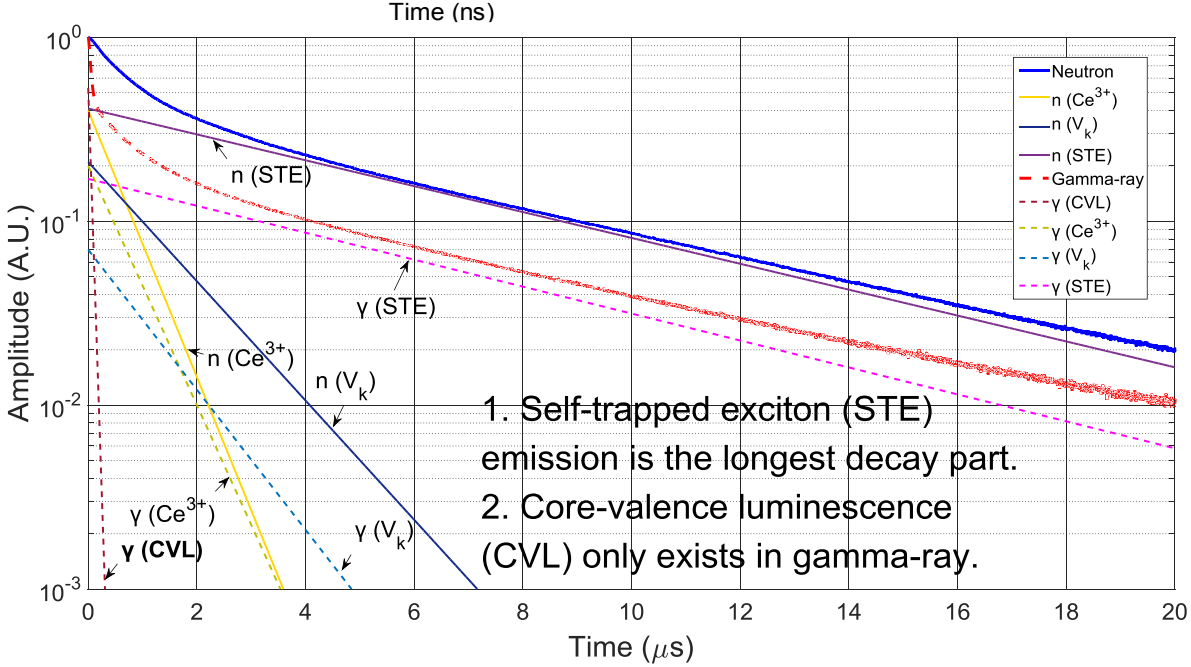
3.2 Results and Analysis



THE FITTING RESULTS OF DECAY.

Reference	Particle	CVL (ns)	Ce^{3+} (ns)	V_k(ns)	STE(ns)
This work	Gamma-ray	49	668	1141	5929
	Neutron	-	599	1339	6173
[15]	Gamma-ray	48	280	730	5240
	Neutron	-	490	1420	6300
[17]	Gamma-ray	2	50	420	3400
	Neutron	-	-	390	1500

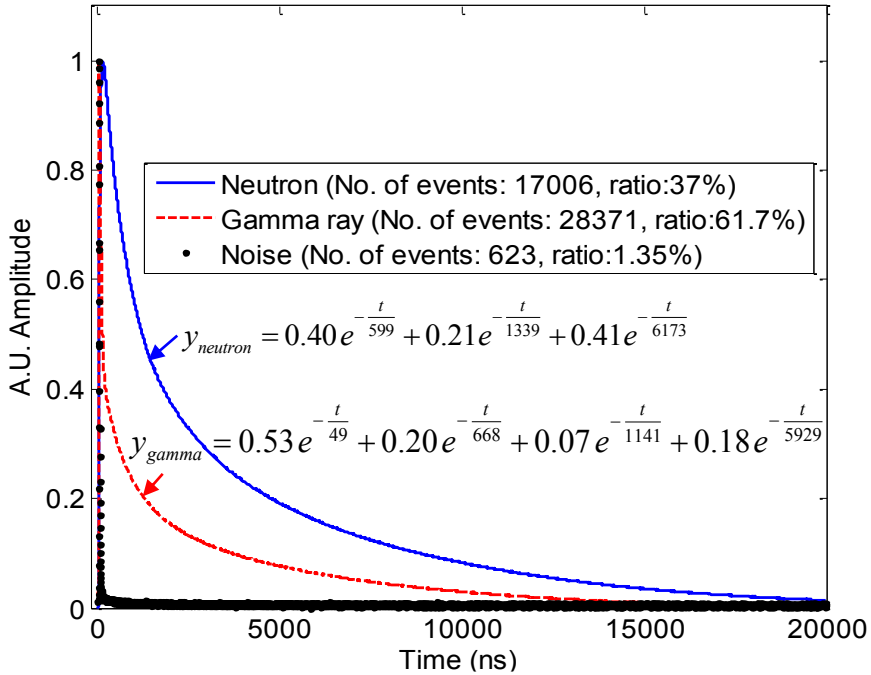
[15] N. D'Olympia et al., " Pulse-shape analysis of CLYC for thermal neutrons, fast neutrons, and gamma-rays.
[17] K. Li, X. Zhang, Q. Gui, P. Jin, G. Tian, " Characterization of the new scintillator $Cs_2LiYCl_6:Ce^{3+}$

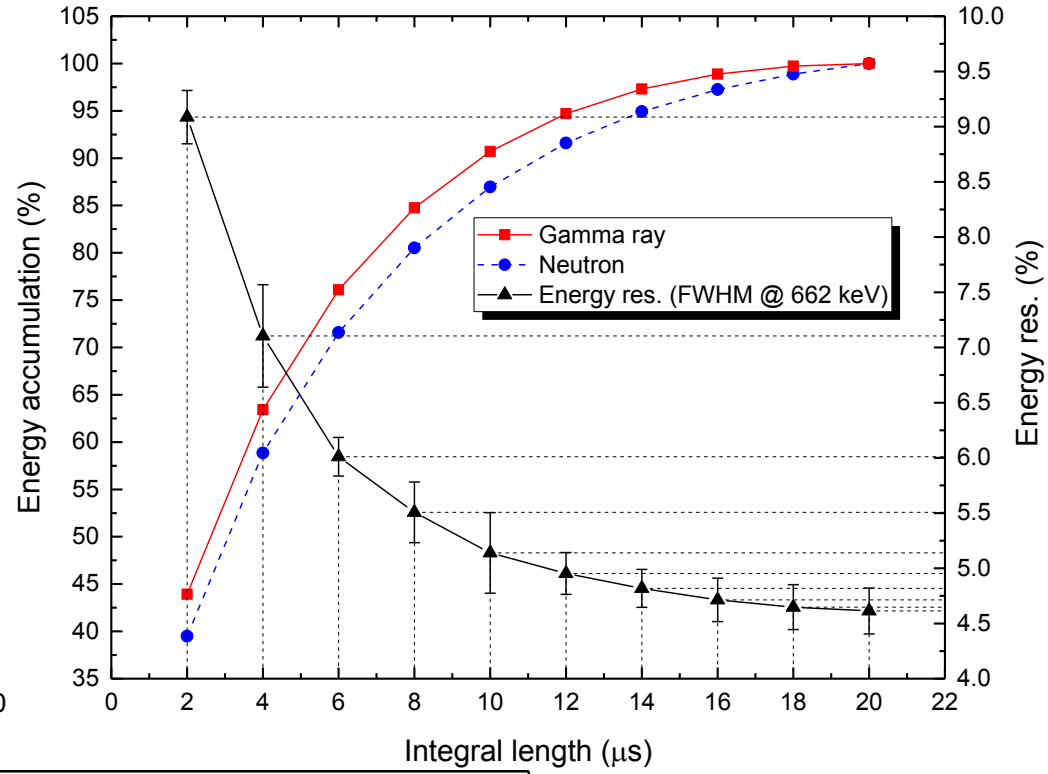


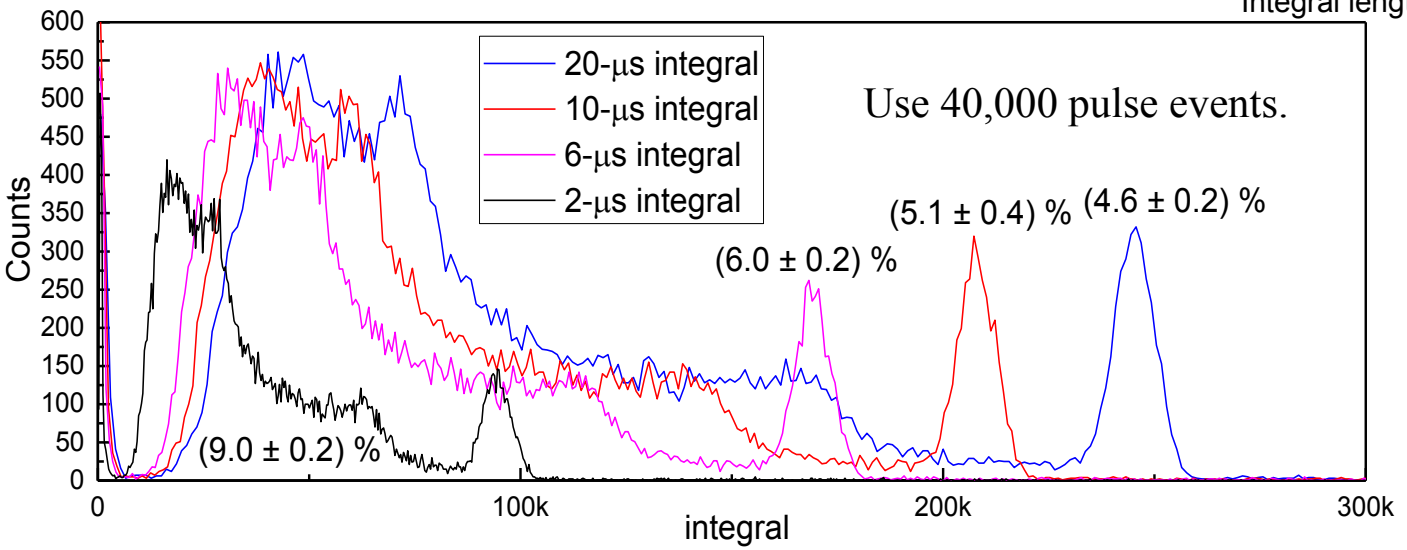
- Four mechanisms are included:
  - direct electron-hole capture (Ce^{3+})
  - binary V_k-electron diffusion (V_k)
  - self-trapped exciton (STE) emission
  - core-valence luminescence (CVL)
- The fitting differences may be caused by the different signal sampling rate or the Ce^{3+} doping concentration.

3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis



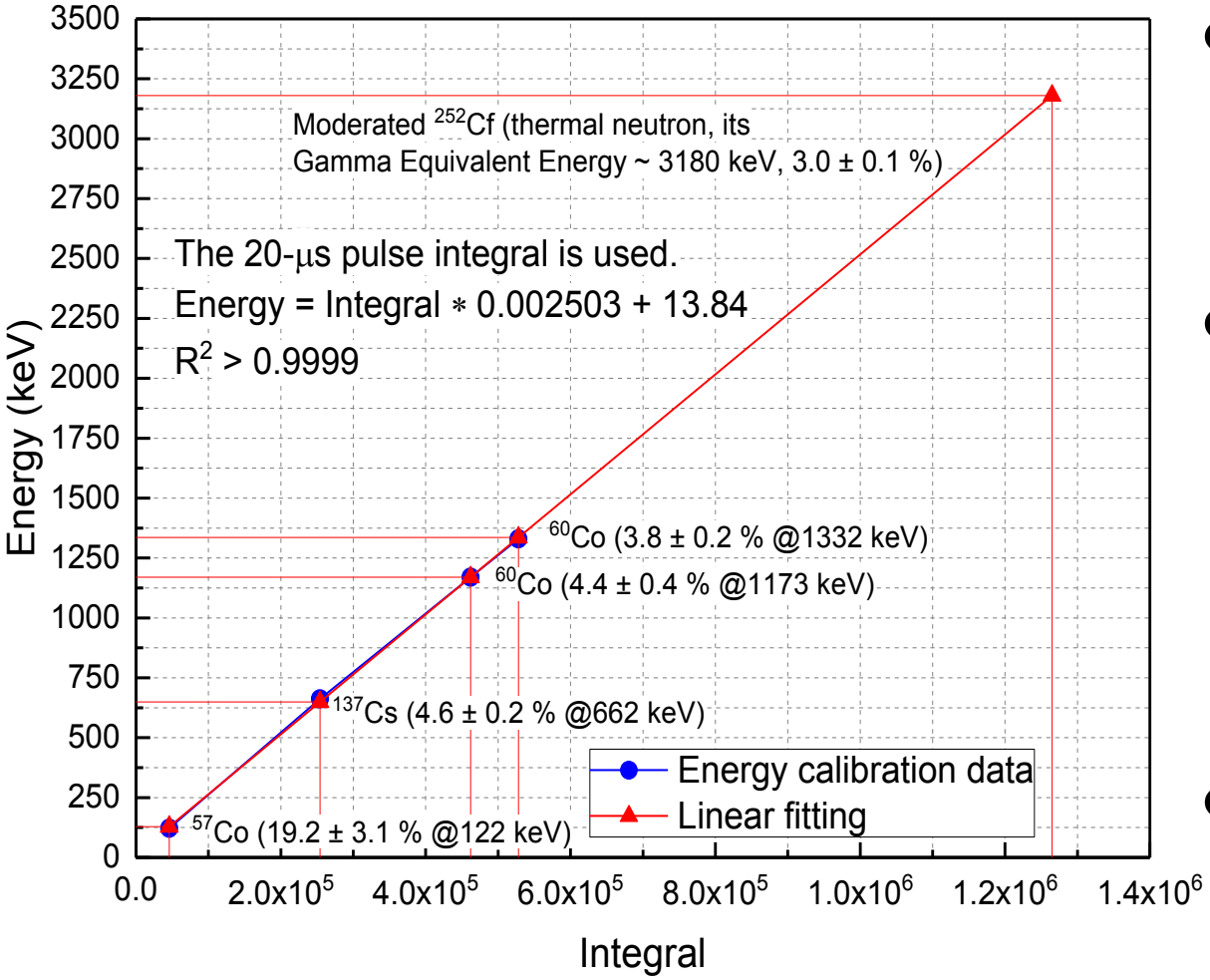




- Hypothesis:
The pulse energy will be collected completely if the integral time is 20 μs (more than 3 times of STE decay).

3. Application: interfaced with a CLYC scintillator

3.2 Results and Analysis



- The 20-μs integral length is used to obtain the pulse energy.
- The energy calibration is done by the linear fitting and the GEE of the thermal neutron is estimated to be ~3180 keV.
- The correlation coefficient R^2 is better than 0.9999.

4. Summary and the future work

4.1 Summary

- Design

✓ This integrated digitizer base is designed for various applications with PMTs coupled with different detectors.

✓ A single category-5 cable is used for power supply and data transmission. The power consumption of the total system is ~5.6 W. A 70 MHz bandwidth preamplifier, 500 MSPS 12-bit ADC board, and a readout module based ZYNQ SoC are designed.

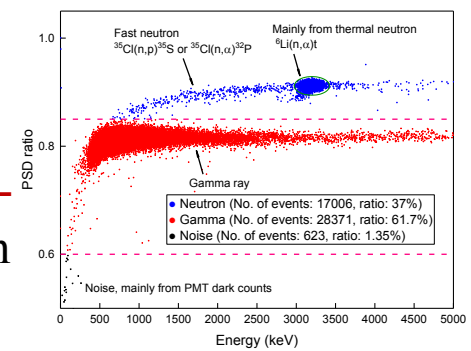
- Application

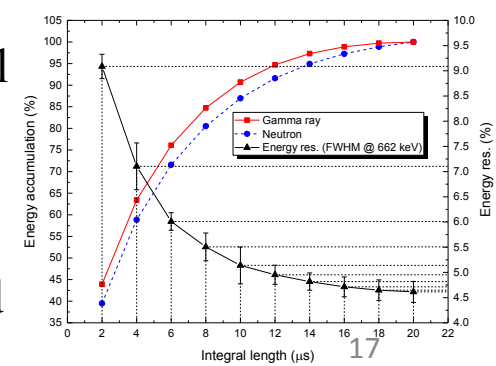
✓ The integrated digitizer PMT base is tested with a CLYC scintillator.

✓ The PSD method is used to discriminate between the neutron, gamma-ray, and noise. The decay of the pulse shape of the normalized neutron and gamma-ray is fitted by several exponential formulas.

✓ We assume that the total energy is collected by a pulse integral of 20 μs, which is more than 3 times the STE (~6 μs). A 12-μs pulse integral can obtain more than 90% of the total energy and the energy resolution is better than 5% at 662 keV. The linearity is better than 0.9999 from 122 keV to ~3.2 MeV.

✓ The PSD FoM is ~3.0 for the whole recorded pulse of the neutron and gamma-ray.





4. Summary and the future work

4.2 The future work

- Different ADC subsystems

ADCs with different sampling speeds and vertical resolution will be used in this integrated digitizer base. The influences due to sampling speeds, resolution of ADC, the integral length on PSD FoM, and energy resolution will be analyzed.

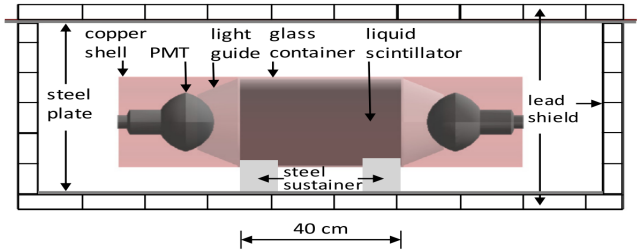
ADC subsystem *(No. 1, this work)*
500 MSPS 12 bit

ADC subsystem *(No. 2)*
1 GSPS 8 bit

ADC subsystem *(No. 3)*
1 GSPS 12 bit

- Other detectors

This integrated digitizer base will also be interfaced with the liquid scintillator with the dual R5912-02 PMTs from Hamamatsu. It is a neutron detector deployed in CJPL (China Jinping Underground Laboratory) for neutron background measurement.



中国锦屏地下实验室
China Jinping Underground Laboratory
CJPL
清华大学 · 雅砻江流域水电开发有限公司

4. Summary and the future work

4.2 The future work

- Clock synchronization based on IEEE 1588 and Synchronized Ethernets

A commercial IEEE 1588 grandmaster is used to generate precise timestamp to every slave node while a commercial Ethernet switch with IEEE 1588 support is used.

With the SyncE capability, the recovered clock from Ethernet PHY chip is used for input of dedicated PLL to generate the clock of logic unit implemented in the programmable logic of ZYNQ SoC of the integrated PMT base.

About 50 ns accuracy clock will be realized and it is adequate for the neutron gamma discrimination application, which needs several microseconds coincident requirement.

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China Jinping Underground Laboratory
CJPL
清华大学 · 雅砻江流域水电开发有限公司

Thank you !

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

21st IEEE Real Time Conference
June 9-15, 2018
Colonial Williamsburg, Virginia, USA

Jefferson Lab
Thomas Jefferson National Accelerator Facility

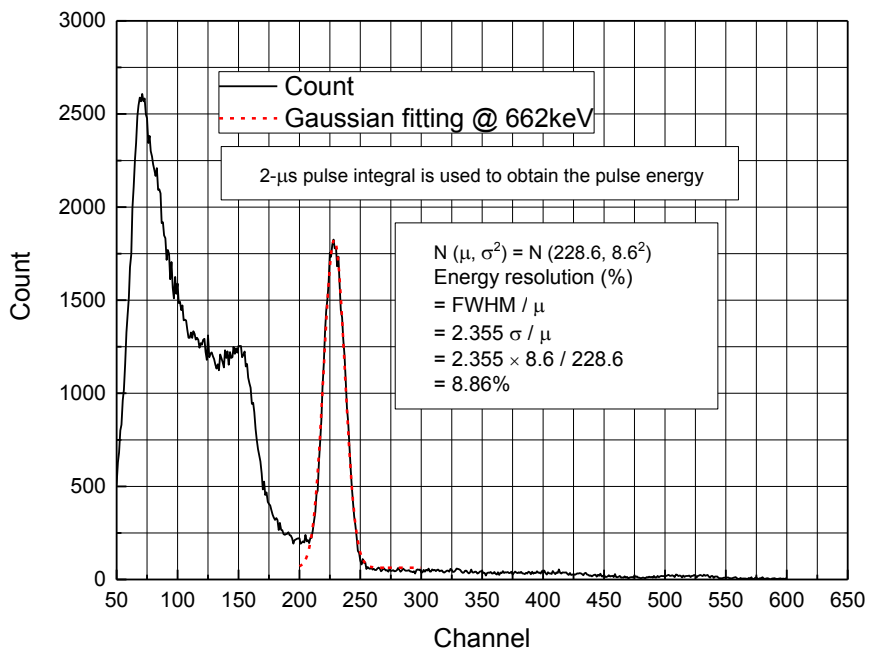
Appendix

Physics

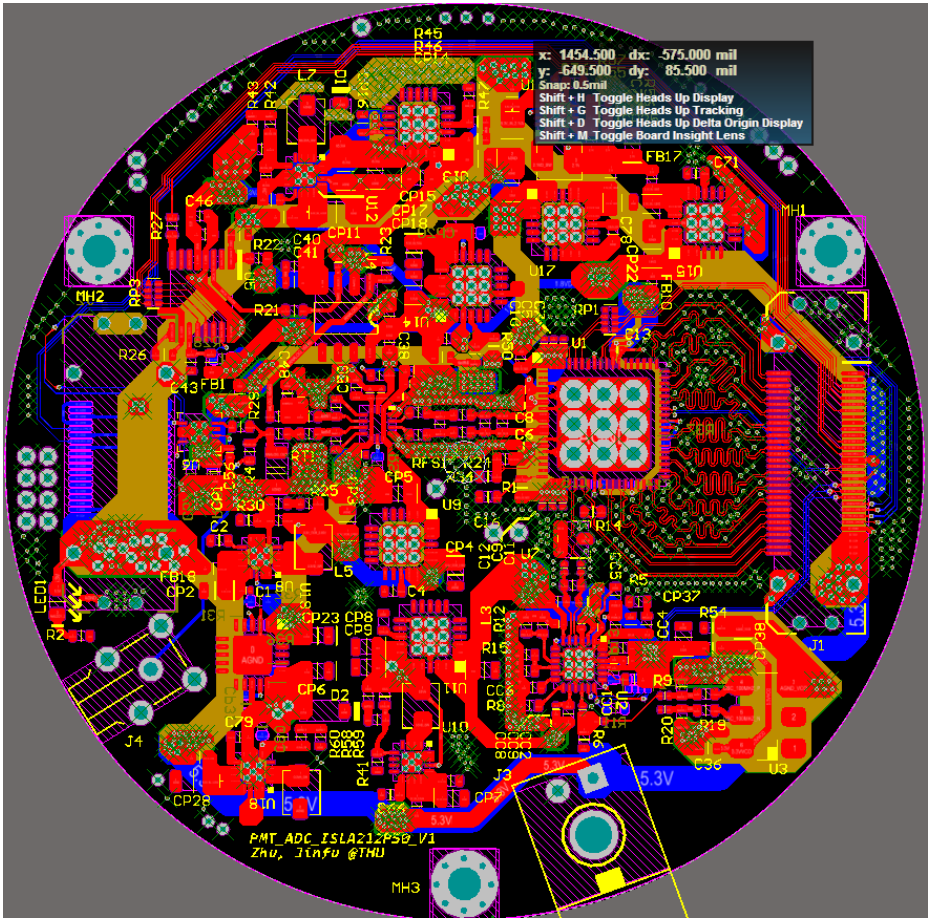
- The low-energy neutrino experiment (in plan) at CJPL (China Jinping Underground Laboratory).

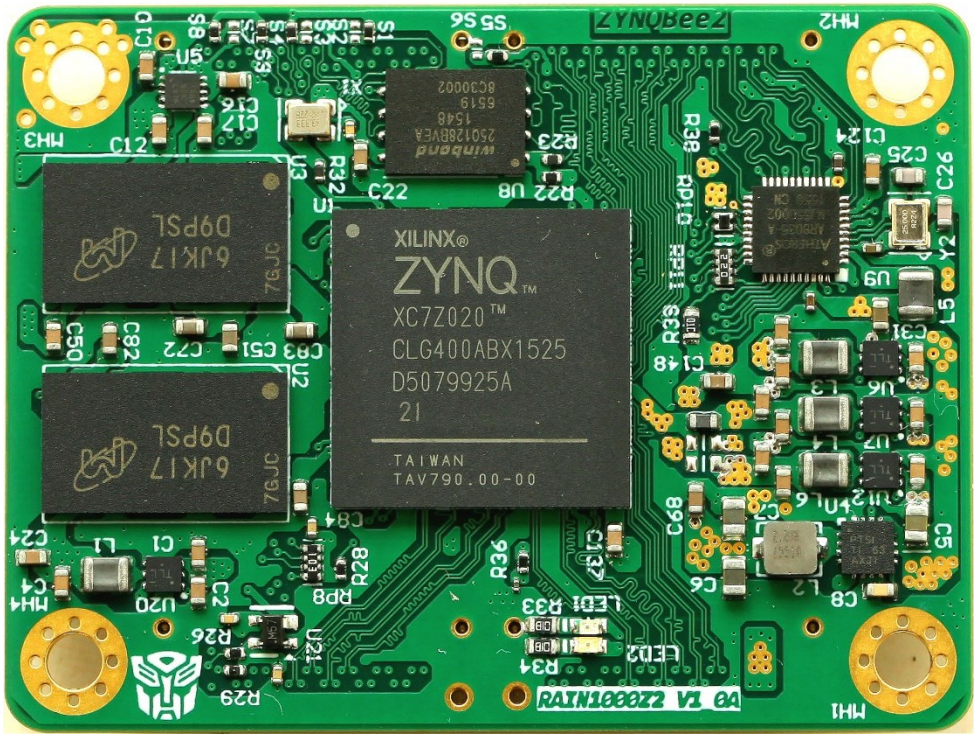
- Goal: This project is aiming to build a kiloton scale neutrino detector at Jinping underground lab, using the slow liquid scintillator technology to separate prompt Cherenkov light and slow scintillation light. We hope to provide precise measurement on solar neutrinos and geo-neutrinos.

Energy res.



Boards

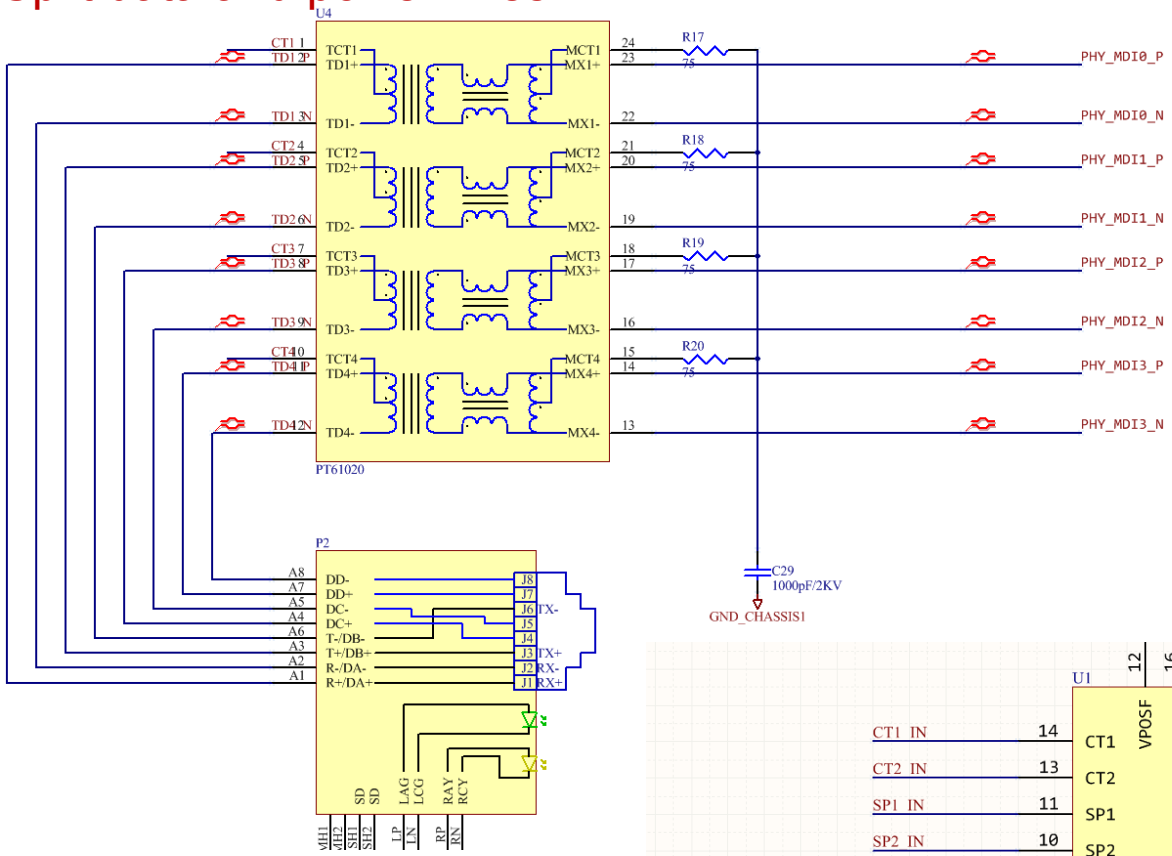

x: 1454.500 dx: -575.000 mil
y: -649.500 dy: 85.500 mil
Snap: 0.5mil
Shift + H Toggle Heads Up Display
Shift + G Toggle Heads Up Tracking
Shift + D Toggle Heads Up Delta Origin Display
Shift + M Toggle Board Insight Lens
PMT_ADC_ISLA212P50_V1
Zhu, Jinfu @THU

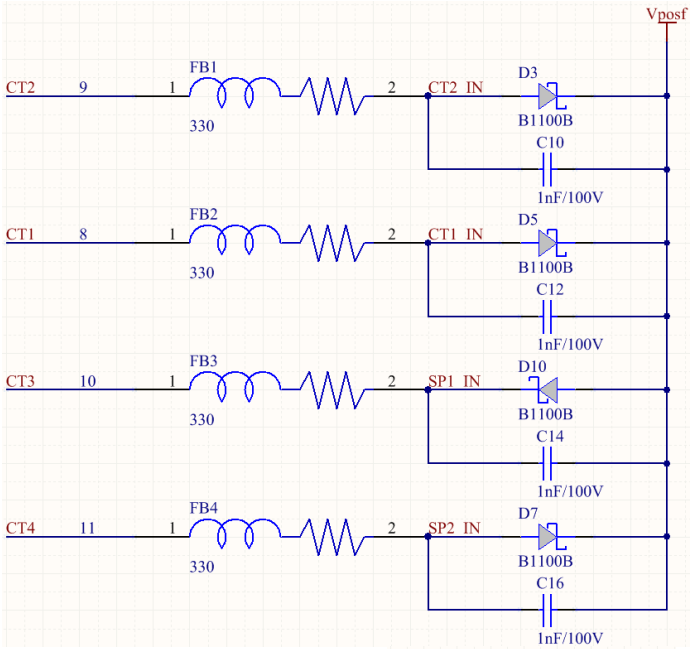

ZYNQBee2
XILINX®
ZYNQ™
XC7Z020™
CLG400ABX1525
D5079925A
21
TAIWAN
TAV790.00-00
RAIN100022 V1 0A

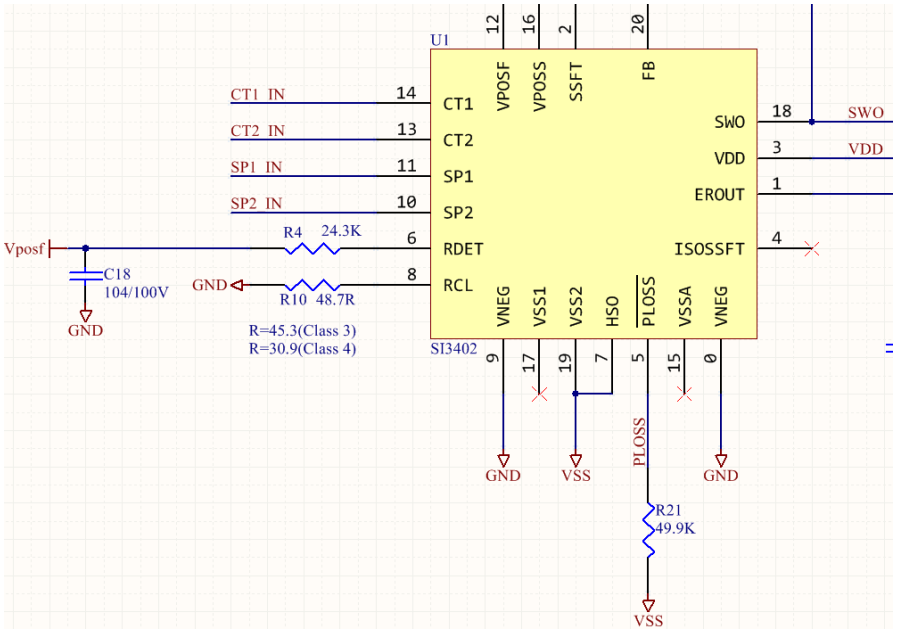
Board-to-Board Connectors:
FX23 series from Hirose

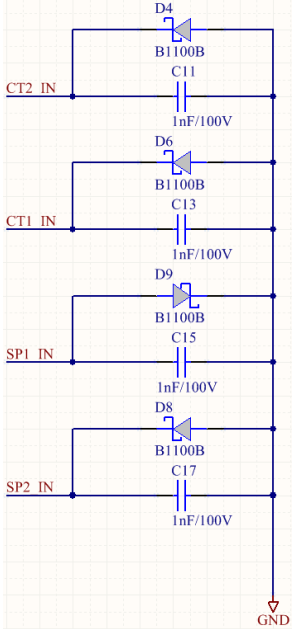
PoE End-Span method

Split data and power lines





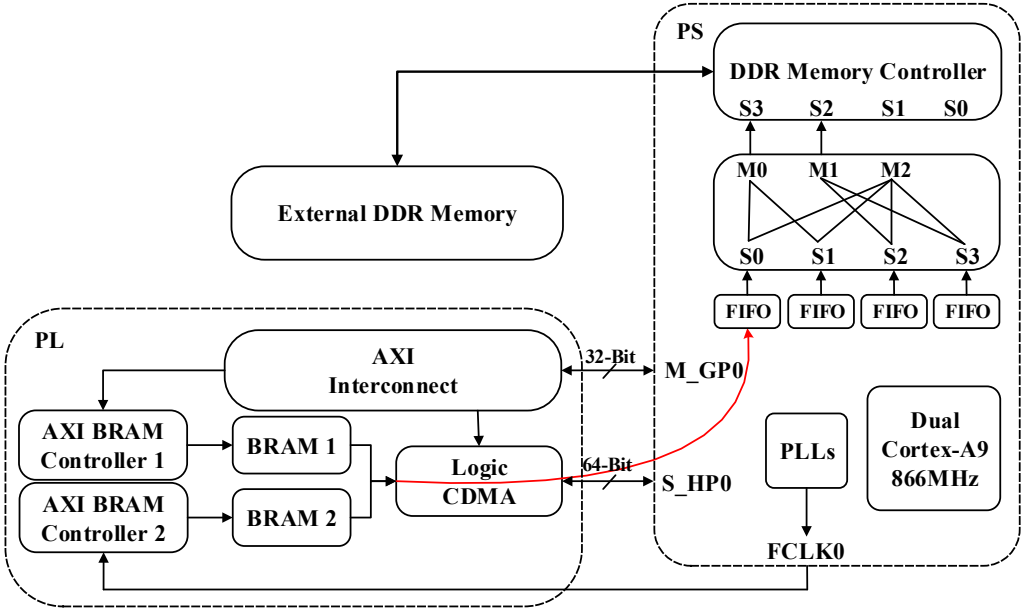


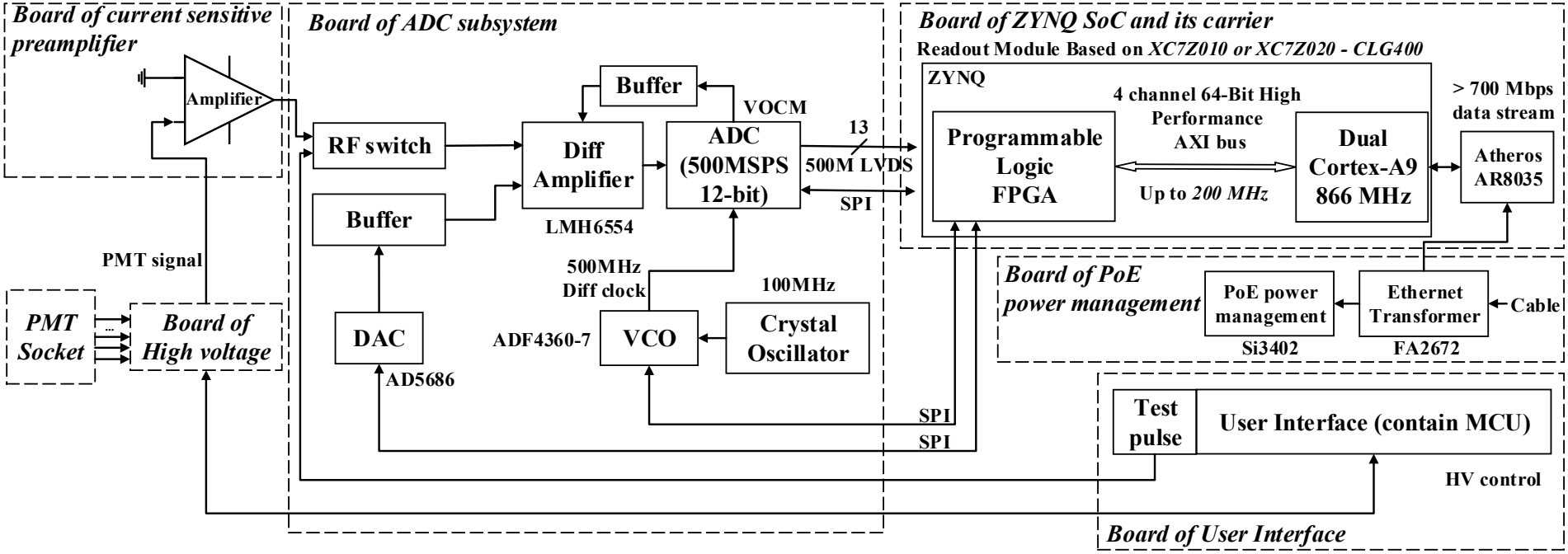


Total structure

THE RESOURCE OF UTILIZATION OF PL.

Resource	Utilization	Available	Utilization (%)
LUT	6911	53200	12.99
LUTRAM	323	17400	1.86
FF	10238	106400	9.62
BRAM	36	140	25.71
IO	41	125	32.80
BUFG	7	32	21.88
PLL	1	4	25.00





IEEE802.3af -> IEEE802.3at(PoE plus)

Feature/standard	*802.3af (802.3at type 1)*	*802.3at type 2 (POE+)*
Output power of power supply [W]	*15.4*	*30.00**
Minimum power available for the powered device [W]	*12.95*	*25.5**
Output voltage of power supply [V]	*44...57*	*50...57*
Supplying voltage available at the powered device [V]	*37...57*	*42.5...57*
Max current [mA]	*350*	*600*
Ethernet compatibility	*10BASE-T, 100BASE-TX and 1000BASE-T*	*10BASE-T, 100BASE-TX and 1000BASE-T*
Range [m]	*100*	*100*
Cabling	*UTP/FTP min. cat. 3*	*UTP/FTP min. cat. 5*

Two modes, A and B, are available. PoE can also be used on 1000BASE-T Ethernet, in which case there are no spare pairs and all power is delivered using the phantom technique.

Mode A delivers power on the data pairs of 100BASE-TX or 10BASE-T.

Mode B delivers power on the spare pairs.

The range can be longer if repeaters are used.