Real-Time Redundancy for the 1.3 GHz Master Oscillator of the European-XFEL

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12.06.2018, Williamsburg

Introduction

- European XFEL
  - DESY
    - Hamburg, Germany
  - Over 3.4 km long facility
  - Stringent requirements for reference signal
    - Femtosecond short- and long-term stability
- Complex synchronisation system
  - 1.3 GHz master oscillator
  - RF/optical reference distribution system

Motivation

- Reference signal usage
  - Generation of derived frequency signals
    - Eg. LO or ADC clock signals
  - PLL and frequency dividers
    - Well defined time relations

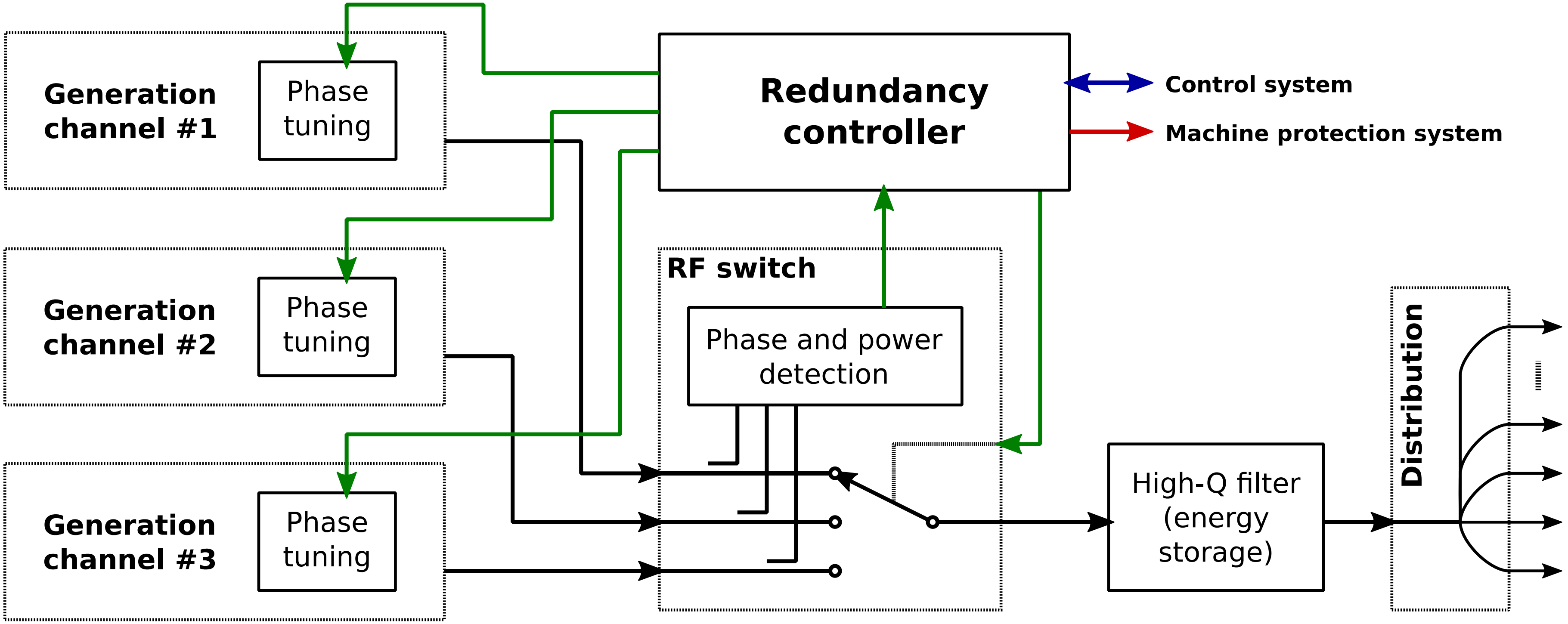
- Reference signal disturbances
  - Cycle-slips
  - Time relations change
  - New set-points required

Motivation

- Reference disturbances vs accelerator availability
  - Disturbances: ns–μs
  - Accelerator: potentially hours
- Performance vs reliability
  - Stringent performance requirements
    - Reduced choice of components and solutions
  - Failures were observed
    - In previous systems
    - During development
- Existing solution – hot spare
  - Switching after failure

System concept

- Generation channels
- Redundancy module



Failure detection

- Issue
  - Disturbances of phase and/or amplitude
- Detection
  - Monitoring of phase and amplitude
  - All *important* failures detectable
- „*Unimportant*" failure
  - Phase noise degradation
    - No immediate action needed

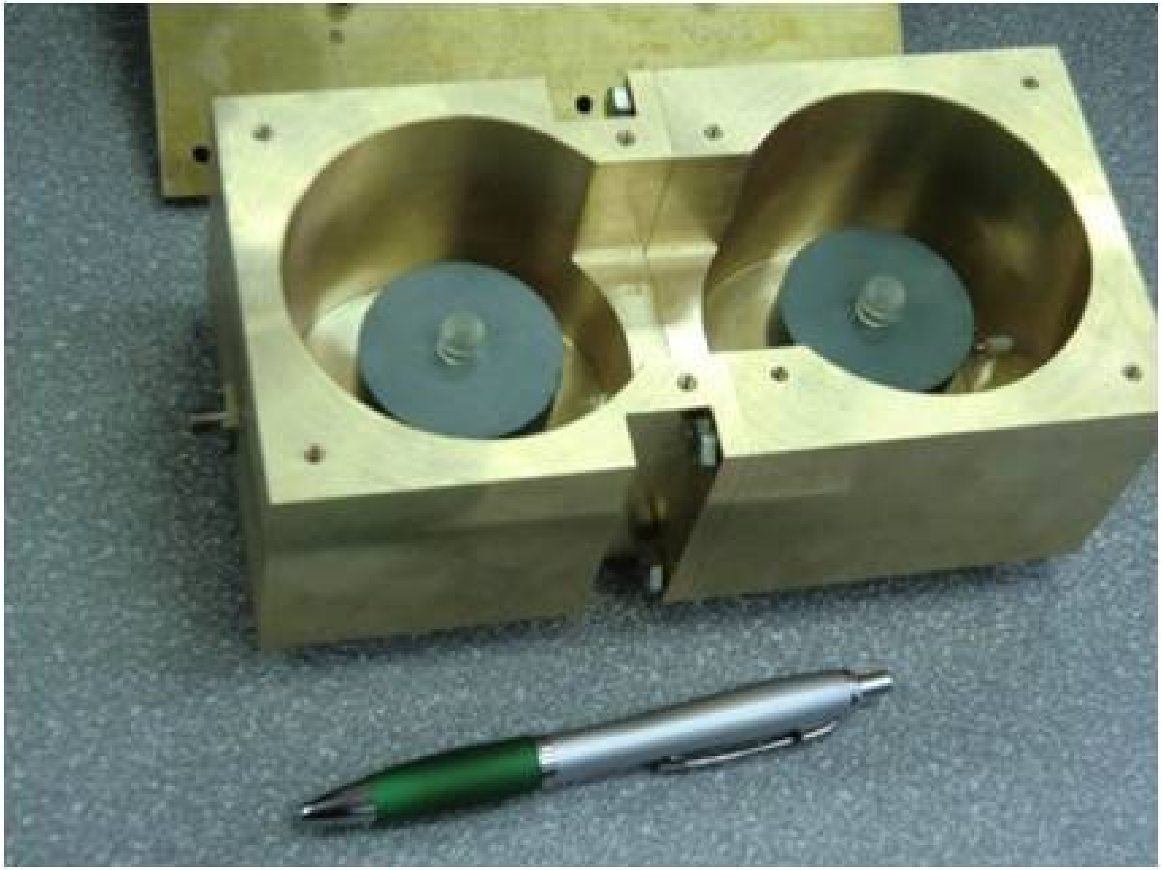
Maintaining signal continuity

- Energy storage in high-Q filter
- Switching between generation channels
  - 40 dBm signals
  - Within tens of ns
- Phase alignment
  - Closed loop synchronisation
    - Integrating controller
  - Vector modulator as phase shifter
    - Infinite shift range

Hardware – Filter

- Dual dieletric resonators
  - Q-factor >10^4

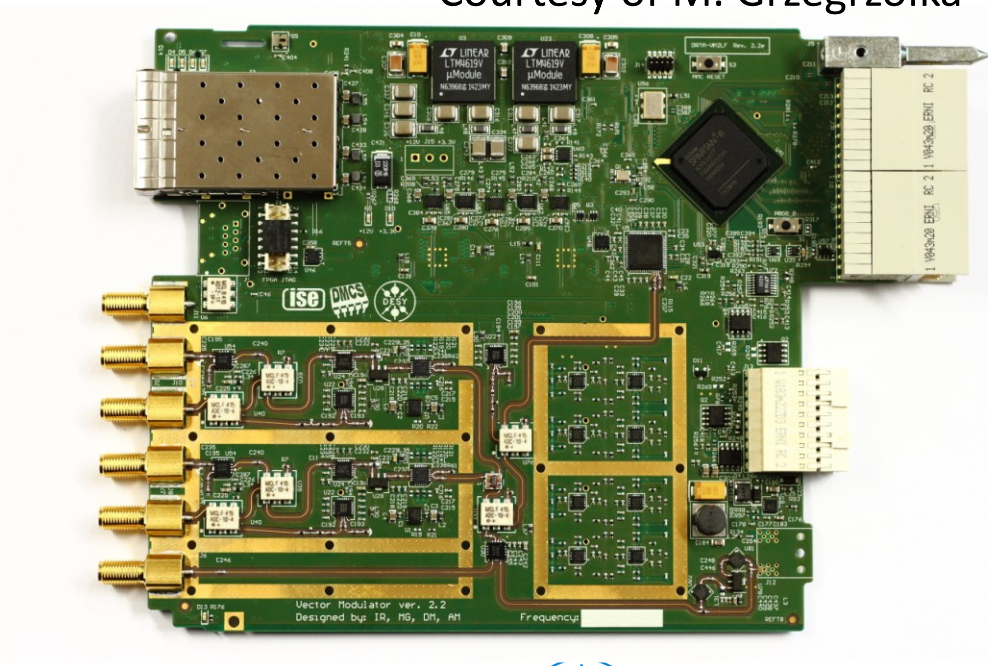
Courtesy of A. Abramowicz



Hardware – Vector Modulator

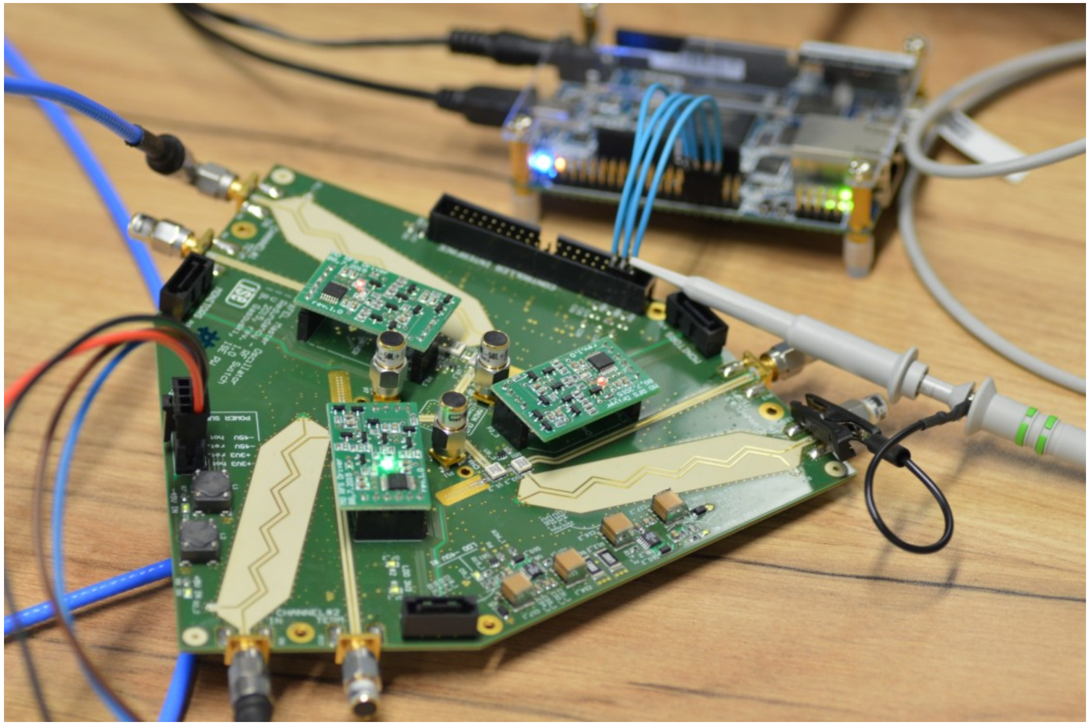
- DRTM-VM2LF
  - Used in European-XFEL LLRF
- Modified: reduced baseband bandwitdth
  - Improved phase noise performance

Courtesy of M. Grzegrzółka



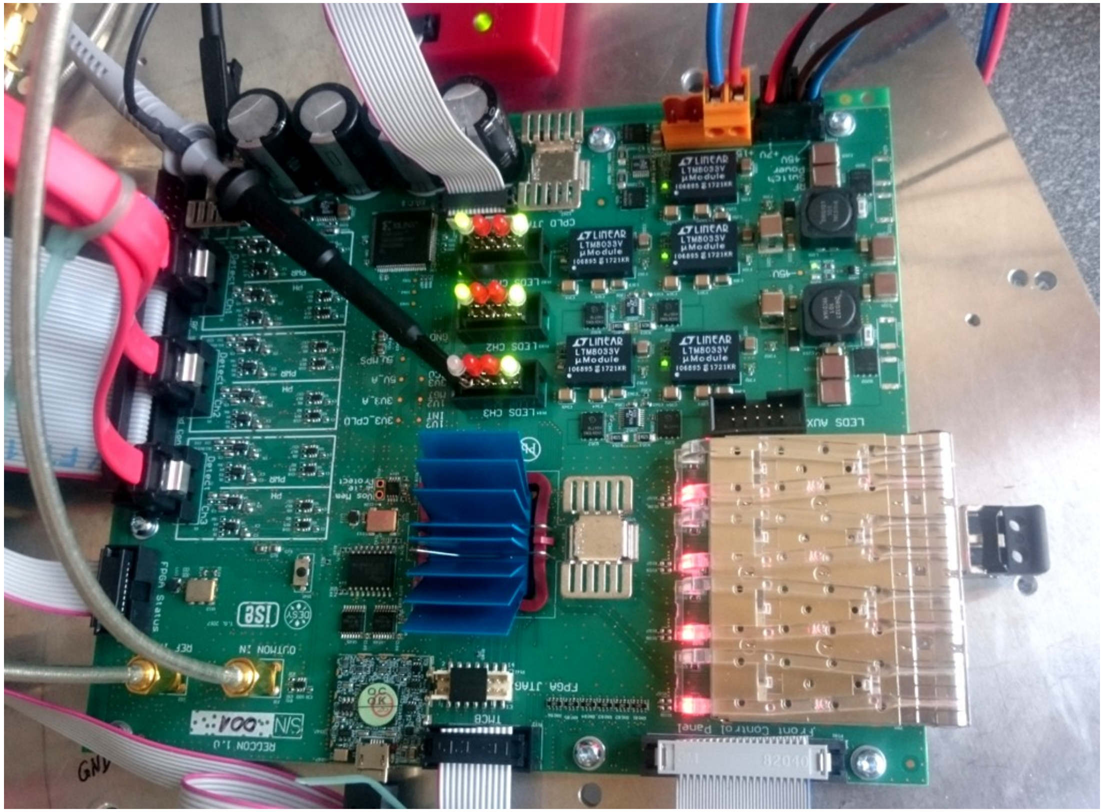
Hardware – RF Switch Module

- Three-way RF Switch
  - +43 dBm power handling
  - < 50 ns switching latency

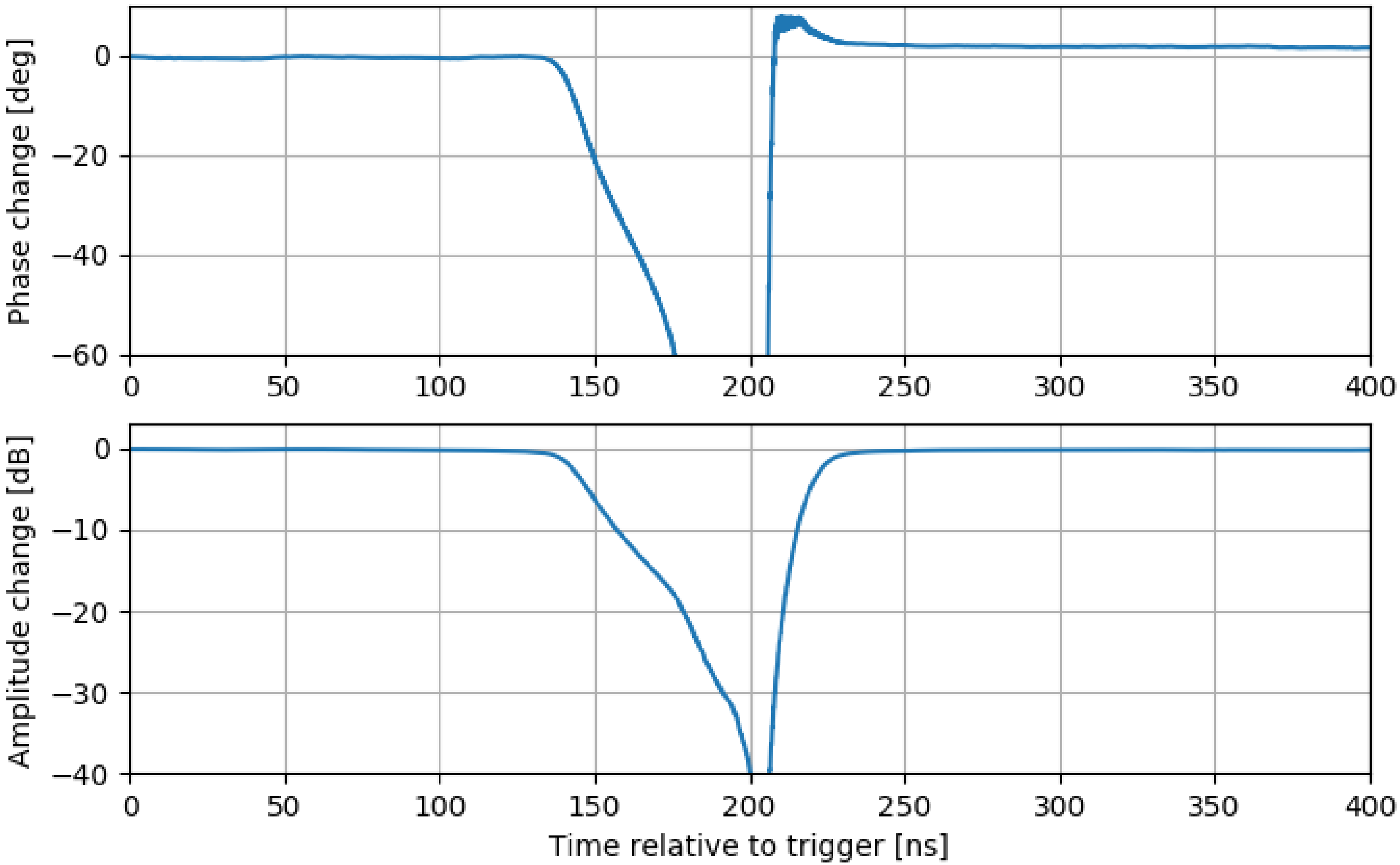


Hardware – Redundancy Controller

- CPLD – low-latency decision logic
  - Triple modular redundancy
- FPGA
  - Synchronisation
  - Supervision
  - Interfacing
  - Control
  - Diagnostics



Test results – power dip (before filter)



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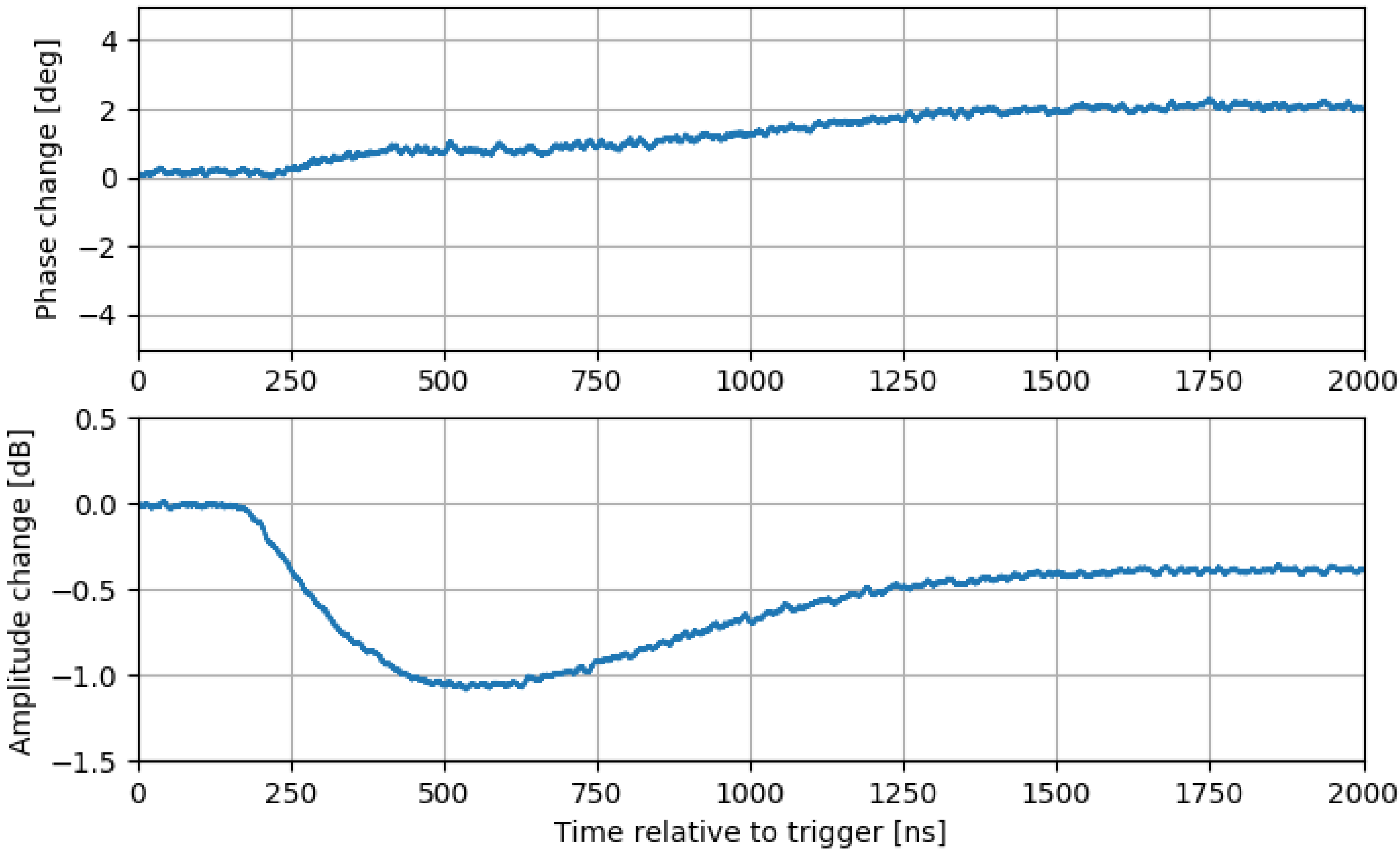
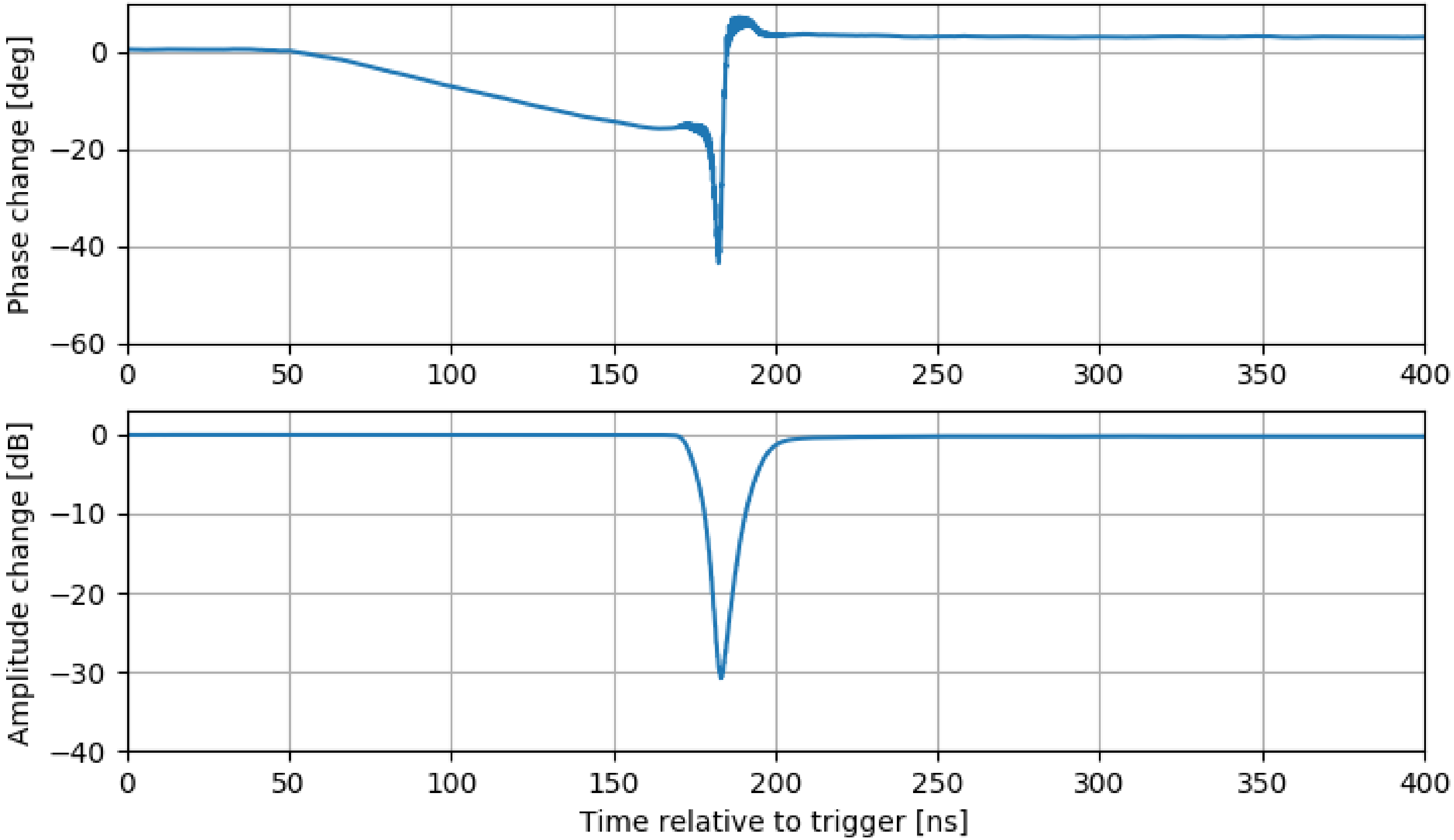
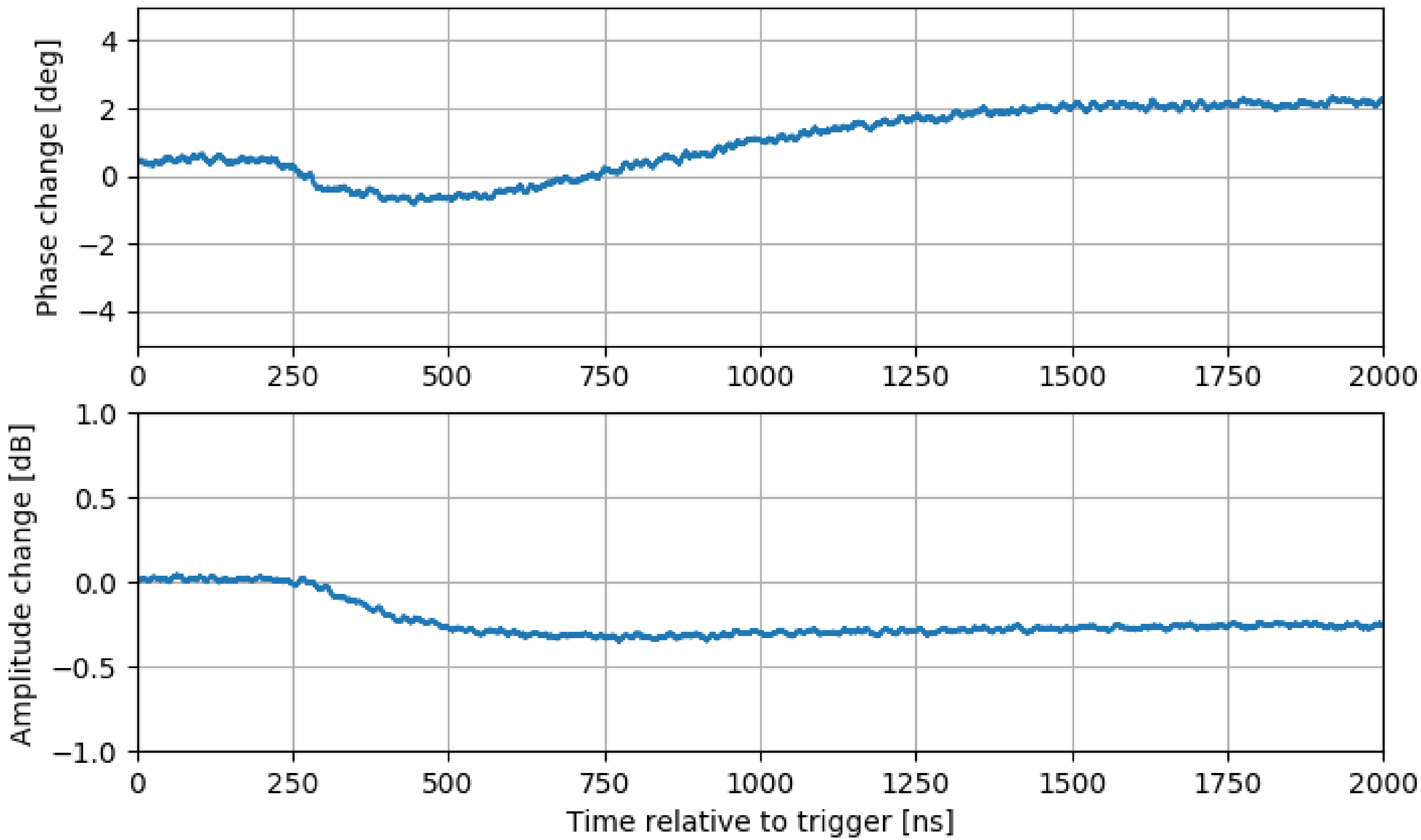


Test results – phase change (before filter)



Test results – phase change (after filter)



Current status

- All hardware modules ready and tested
- Parts of firmware still missing
  - Synchronisation
  - Auto-calibration
- Testing in progress
  - Low-power signals
  - Manual synchronisation
  - Successful reaction to artificially induced failures

Conclusion and plans

- Succesful reaction to failure proven
- Further development and tests
  - High-power signals (+41 dBm)
  - Firmware development
  - Improvement of detection accuracy

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ISE

DESY

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