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Timing and clocking scheme in the upgraded LHCb detector

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In 2019, the LHCb experiment at CERN will undergo a major upgrade where its detector electronics and the entire readout system will be replaced. The goal is to read-out all events at the full LHC frequency of 40 MHz, reaching a total data rate of ˜40 Tb/s. In this context, a new timing, trigger and fast readout control system has been developed: its main tasks are to distribute centrally the clock, the timing information and to synchronize all elements in the readout system: from the very last Front-End ASIC to the building of events to be stored.

A proper clocking scheme is therefore paramount to make sure that the electronics of the entire readout system is well synchronized with the LHC timing and with the global LHCb upgraded detector. In this paper, the clock scheme as currently used in the upgrade of the LHCb experiment is described in detail, with particular emphasis on the mechanisms, both in FPGA and in hardware design, employed to ensure fixed latency of the clock, deterministic control over the fine phase, low jitter and a narrow frequency spectrum. Measurements for the validation of the scheme are also enclosed.

Description

system timing/clock

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