A Driver ASIC for Scientific CCD Detectors Using 180nm Technology

Jie Gao, Dong-xu Yang, Yi Feng, Guang-yu Zhang, Wen-qing Qu, Jian-min Wang, Hong-fei Zhang, Jian Wang*

State Key Laboratory of Technologies of Particle Detection and Electronics, Modern Physics Department, University of Science and Technology of China

*Email: wangjian@ustc.edu.cn, IEEE Senior Member

1.Introduction

Charge-coupled devices (CCD) have been widely used in astronomical telescopes since the 1970s result from their excellent quantum efficiency and low noise etc . A large scale mosaic CCD detector system usually requires a driver with varieties of clocks and biases, while complicated logic control timing is required, which becomes a technical difficulty in the design of CCD detector system. The CCD detector system must be driven by a massive electronic system, which is often built with discrete components.

In order to achieve the driver function for several types of scientific CCD detector, and decreasing the size of electronics of CCD detector system, an Application-specified Integrated Circuit (ASIC) was designed. It is used for CCD driver and called BCDA (Bias Clock Driver ASIC), provides multi-channel clocks and bias voltage.

The first version design of BCDA has been finished, and the 180 nm BCDlite technology of Global Foundries is selected to implement the design. In a $4\ \mathrm{mm} \times 4\ \mathrm{mm}$ bare chip, six channels of clock circuits, four channels of Bias circuits and some other test circuits are implanted. The layout of BCDA is shown in Fig 1.

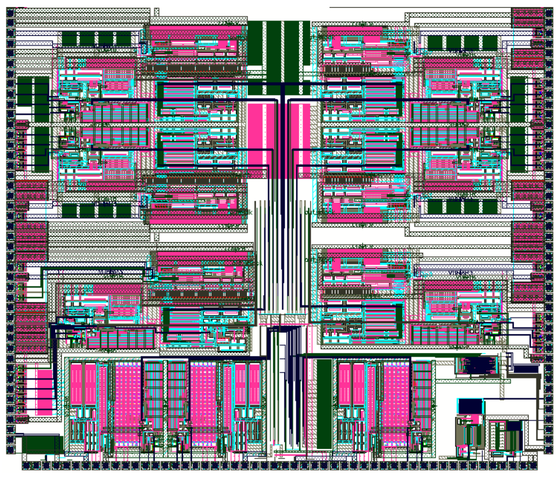

Fig 1. The layout of BCDA

2.Driver ASIC Design

The scheme of BIAS circuits is shown in Fig 2. The output current of an 8-bit current-steering DAC generates an voltage drop on an off-chip resistor, R_1, which is also connected to the positive terminal of the off-chip high-voltage amplifier, ranging from 1.3 – 6 V. Thus the output voltage of the off-chip amplifier is from 8 – 30 V. The reference circuit of DAC is generated by an on-chip low-voltage amplifier and an off-chip high-precision resistor, R_0, so that the reference current is not affected by the technology process.

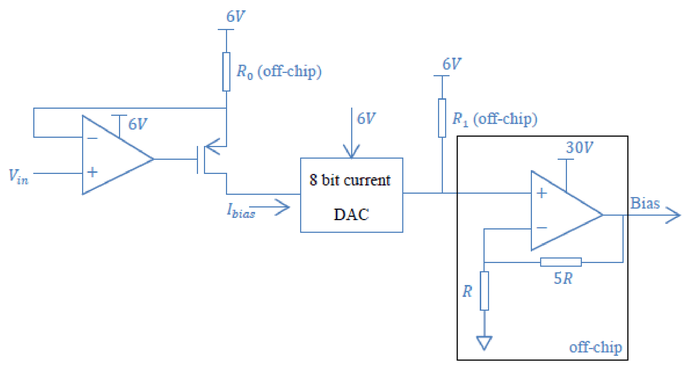

Fig 2. The scheme of BIAS circuits

The scheme of CLOCK circuits is shown in Fig 3. There are two types of CCD clocks, one is parallel clock which is slow and heavily loaded, and the other is serial clock which is fast and light loaded. The designs of two clocks are the same except the output driver capacity. A clock switch with the range of upper's rail voltage from 0V to 16V is designed to generate the clocks. The structure of the voltage generation of upper's rail is same as BIAS circuits shown in Fig 2. The input of the clock switch is single-end LVCMOS signal, which is converted to differential clock signal by an internal single-to-differential circuit. The output current of an 8-bit current-steering DAC is used as tail current of the clock switch to change the driving capability.

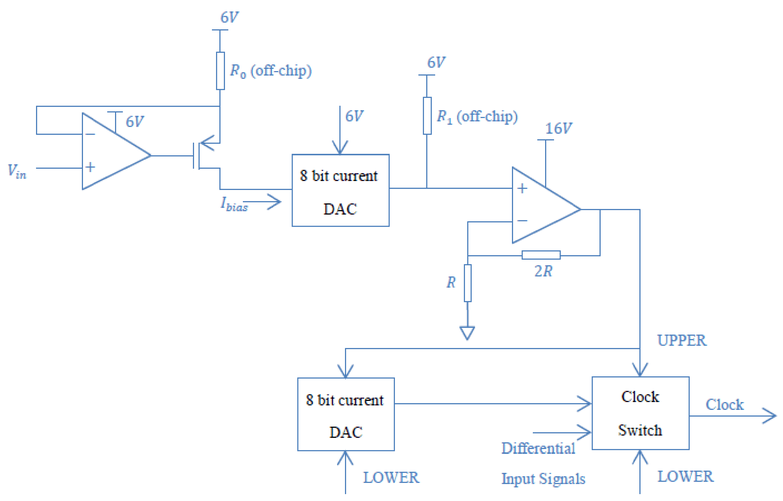

Fig 3. The scheme of CLOCK circuits

3.Test Result

The tests have been done. The ASIC is shown in Fig 4.

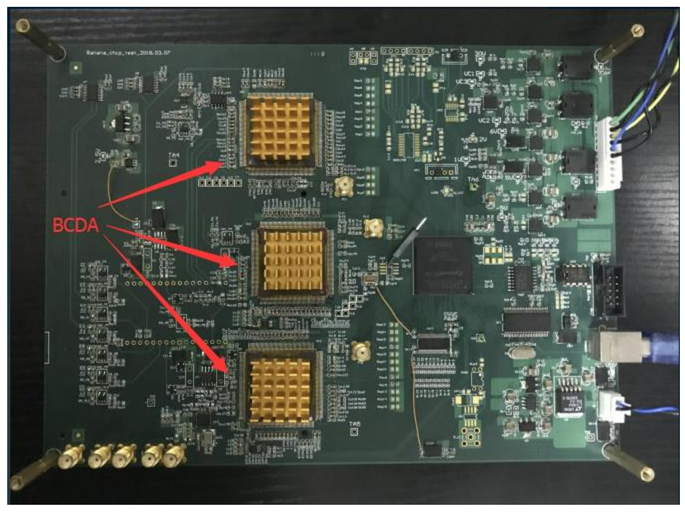

Fig 4. BCDA test system

Fig 5 shows the results of one of the 10 DACs. All 8-bit DACs for BIAS and CLOCKs work as expected with excellent linearity, stability.

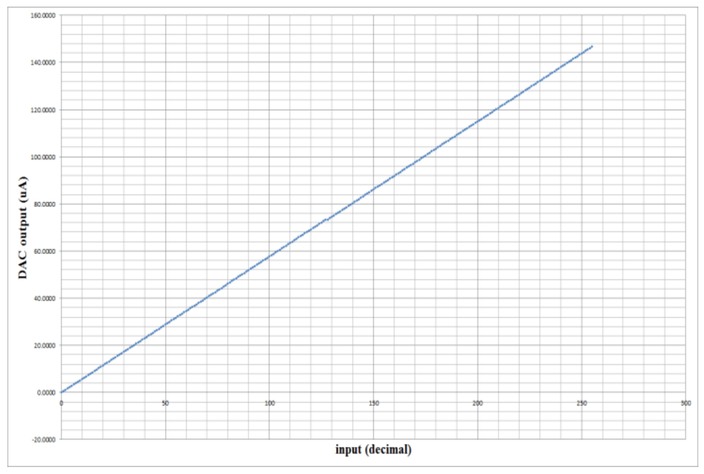

Fig 5. The Results of 8-bit DAC test, Output Current vs. Input Code

The waveform shape of the CLOCKs, including the rise time, the fall time and the switching speed, will directly affect the readout speed and full well capacity of CCD47-20 and CCD230-84. Fig 6 shows the results of CLOCKs with the heaviest load and maximum driving capability.

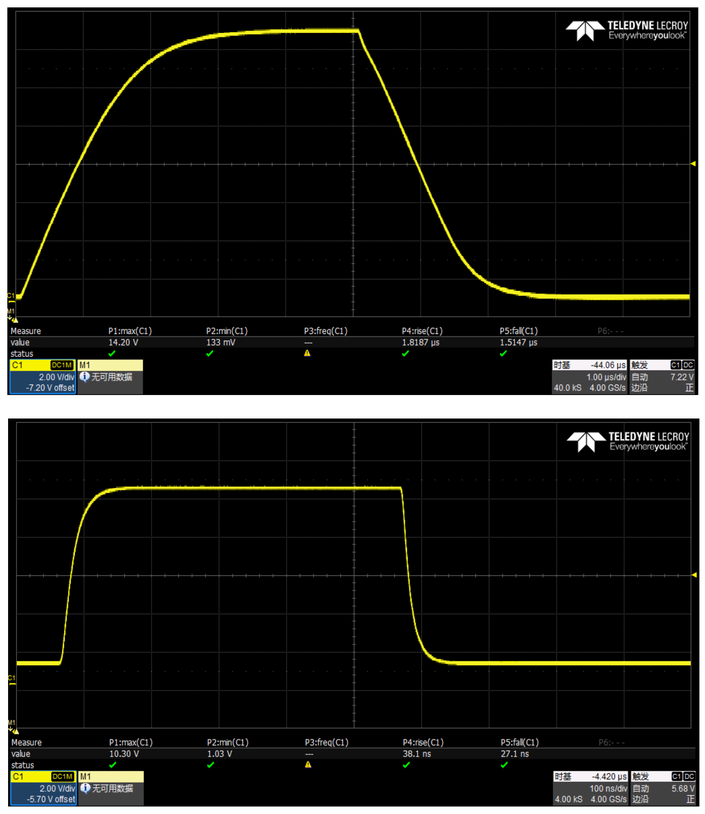

Fig 6. The Results of CLOCKs test, Parallel Clock (upper) and Serial Clock (bottom)

Bibliography

1. Amico P, Beletic J W, Beletic J E. Scientific Detectors for Astronomy[J]. Astrophysics & Space Science Library, 2004.
2. Leskovar B, Lo C C. A Wide-Band Measuring System for Studying Charge-Coupled Device Characteristics[J]. IEEE Transactions on Nuclear Science, 2011, 26(1):449-454.
3. Gradl D A. 250 MHz CCD driver[J]. IEEE Journal of Solid-State Circuits, 2003, 16(2):100-101.
4. Woodhouse G F W, Waltham N R, French M J, et al. The use of ASIC Thecnology in the Development of Compact, Low-Power CCD Cameras[J]. 2004.