Pulsar3a: Next Generation ATCA Full Mesh General Purpose FPGA Based Processing Board

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Outline

- Motivation and general R&D goals
- ATCA background
- Pulsar2a and Pulsar2b
- New Pulsar3a
  - Motivation and challenges
  - Hardware subsystem changes
  - Preliminary results
- Conclusion and next steps

Pulsar Board R&D Goals

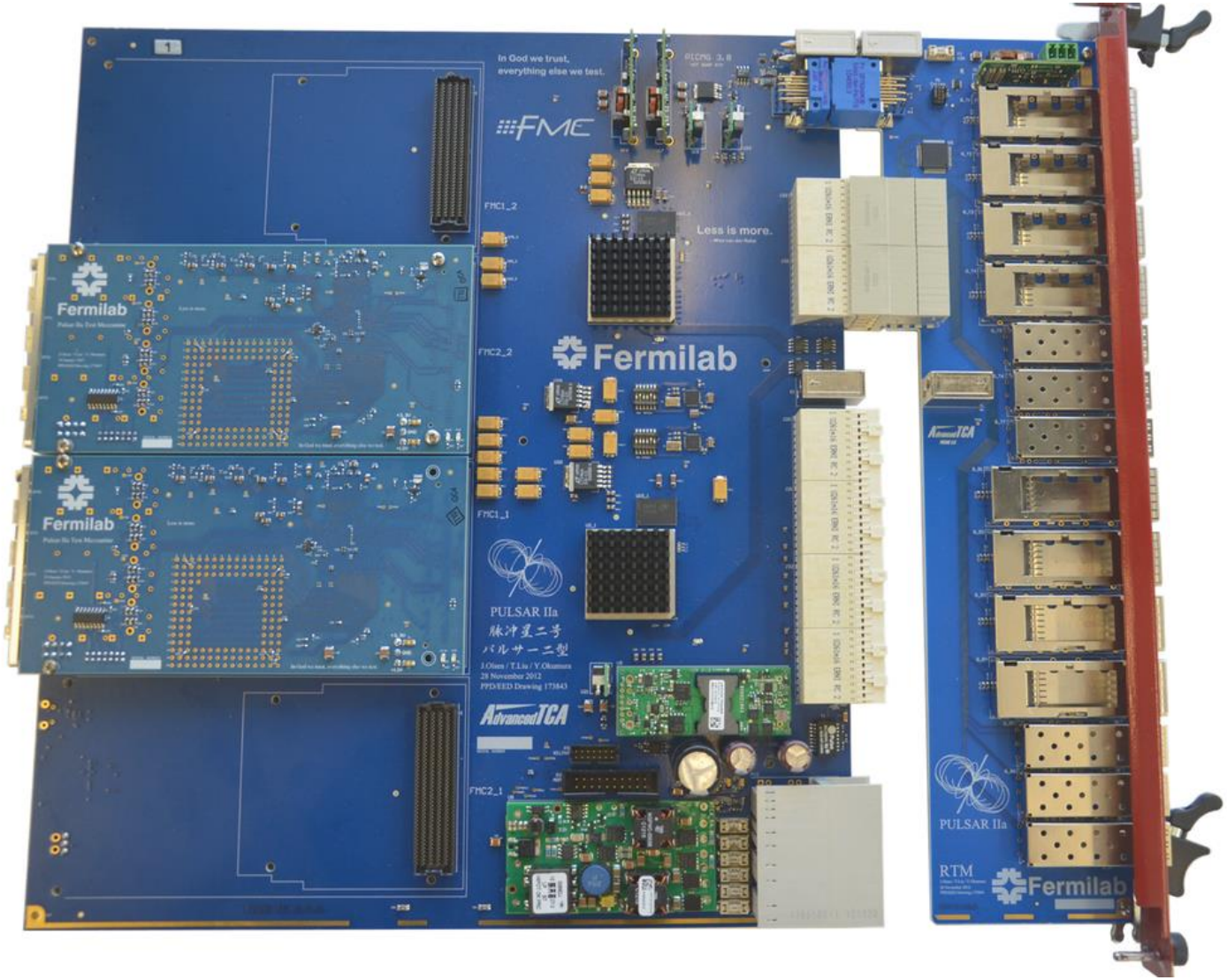
The Pulsar is a custom **ATCA full mesh** enabled **FPGA-based** processor board which has been **designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth interconnections**. Initially motivated by silicon-based tracking trigger R&D needs for LHC experiments, the Pulsar is uniquely positioned as a **flexible general-purpose platform ideally suited to situations where multiple processing engines need to be tightly coupled.**

- ATCA platform, full mesh backplane
- Scalable, flexible, interconnected
- High bandwidth interconnects
- FPGA based, general purpose
- Multiple processors, tightly coupled
- Blur the distinction between FPGAs

ATCA Background

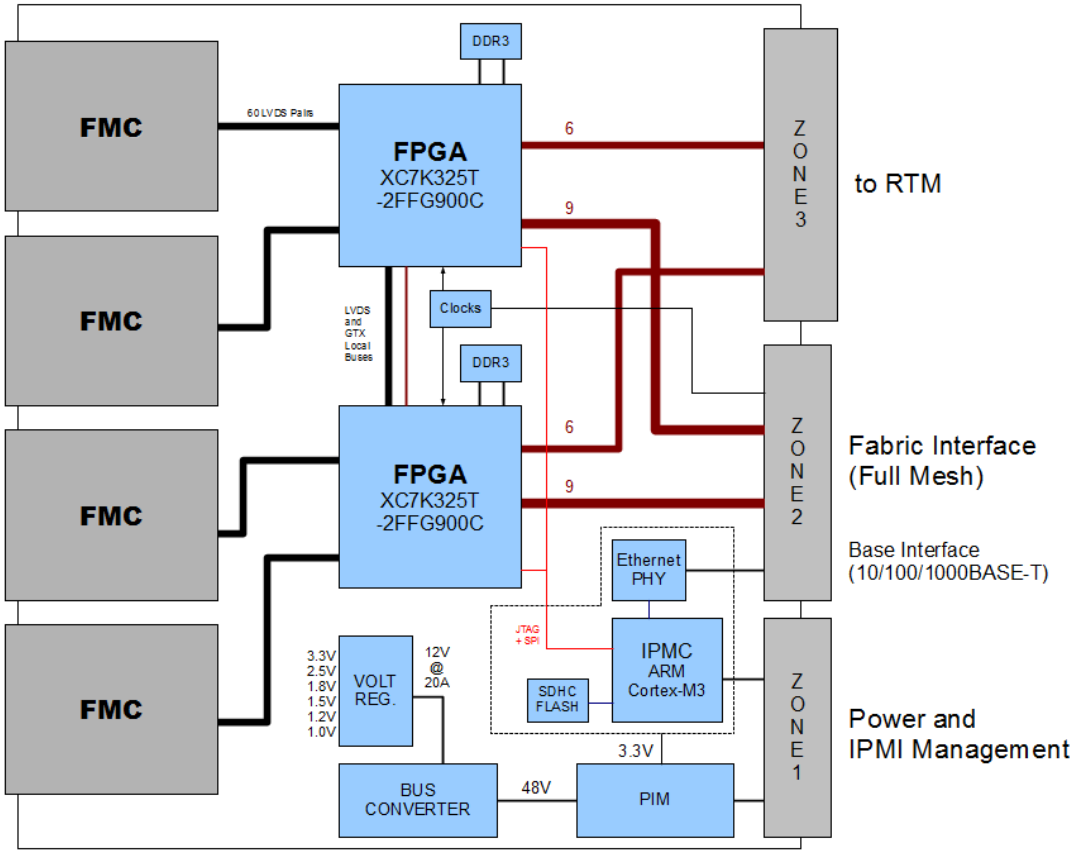
- Advanced **Telecommunications** Computing Architecture
  - High availability
  - Redundant 48V power
  - Redundant control
  - Hot swap everything
- Unique full mesh backplane
  - 4 lanes between all slots
  - 10G – 40G – 100G
- Large 8U x 280mm form factor
- High power 300W+ per slot
- IPMI management of intelligent field replaceable units

Pulsar2a (2012-2013)

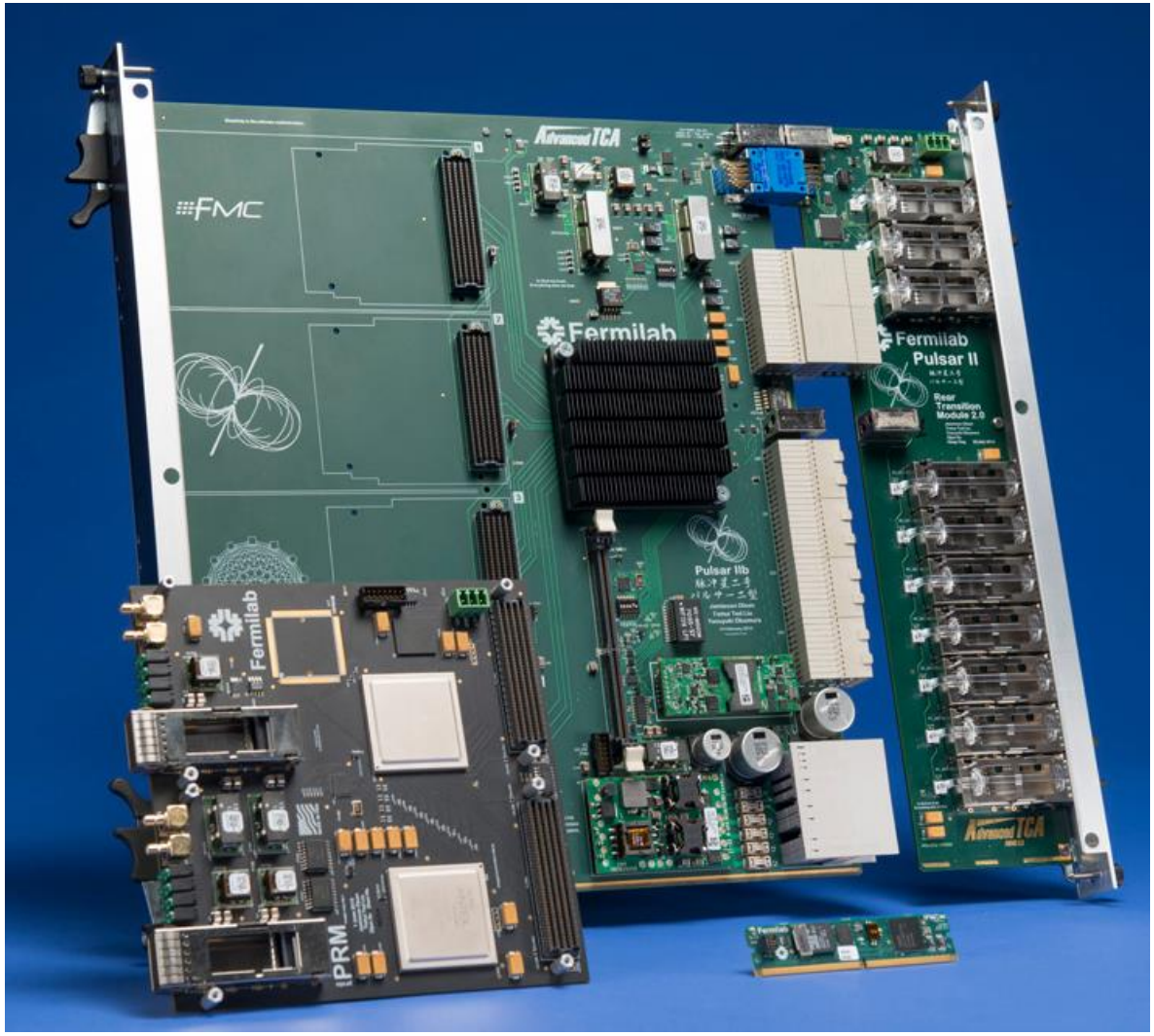


Pulsar2a Results

- R&D goals met:
  - First experience with 7 series FPGAs and Vivado toolchain
  - Backplane and RTM GTX links working at 6Gbps
  - LVDS working at 400MHz / 800Mbps DDR
  - Switching regulators working OK
  - Basic IPMC software working with shelf manager
  - No mechanical issues

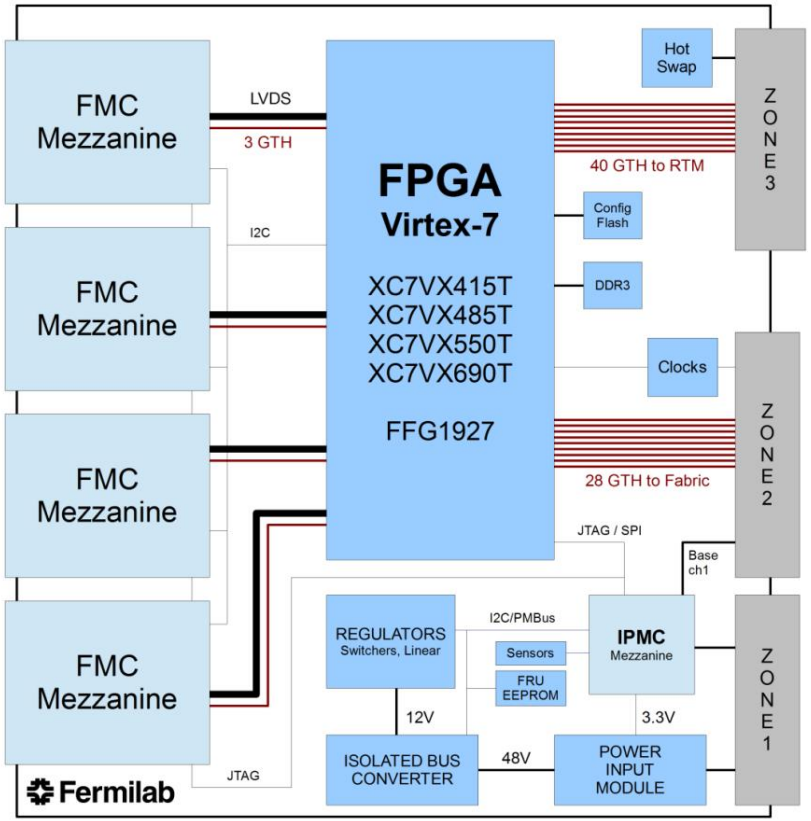


Pulsar2b (2014)



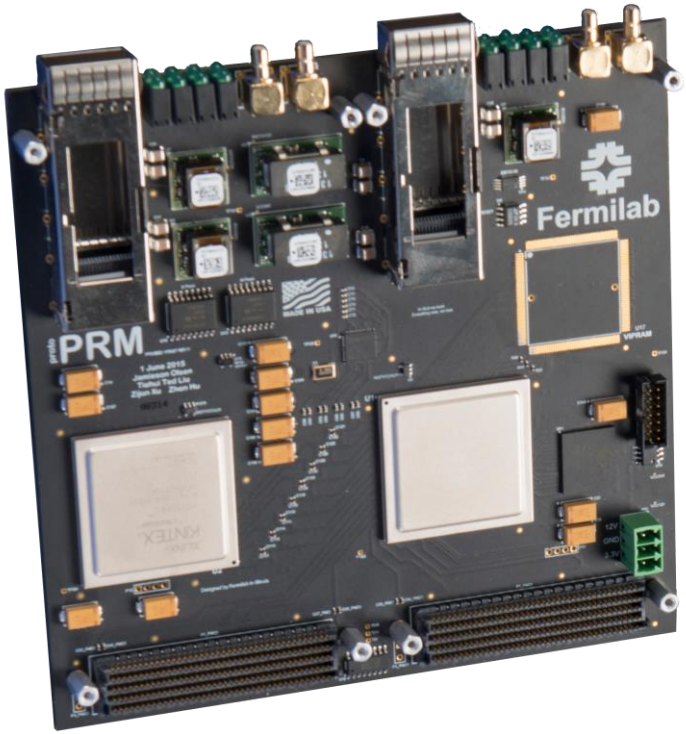
Pulsar2b Results

- Gained experience with a large Virtex-7 FPGA (690T)
- Successfully tested GTH transceivers to 10Gbps
  - RTM optics
  - Full Mesh Backplane (many different vendors!)
  - FMC Mezzanines
- New IPMC module
  - Continue developing IPMI software
  - Network interface (telnet, ftp, etc.)
  - Xilinx Virtual Cable protocol

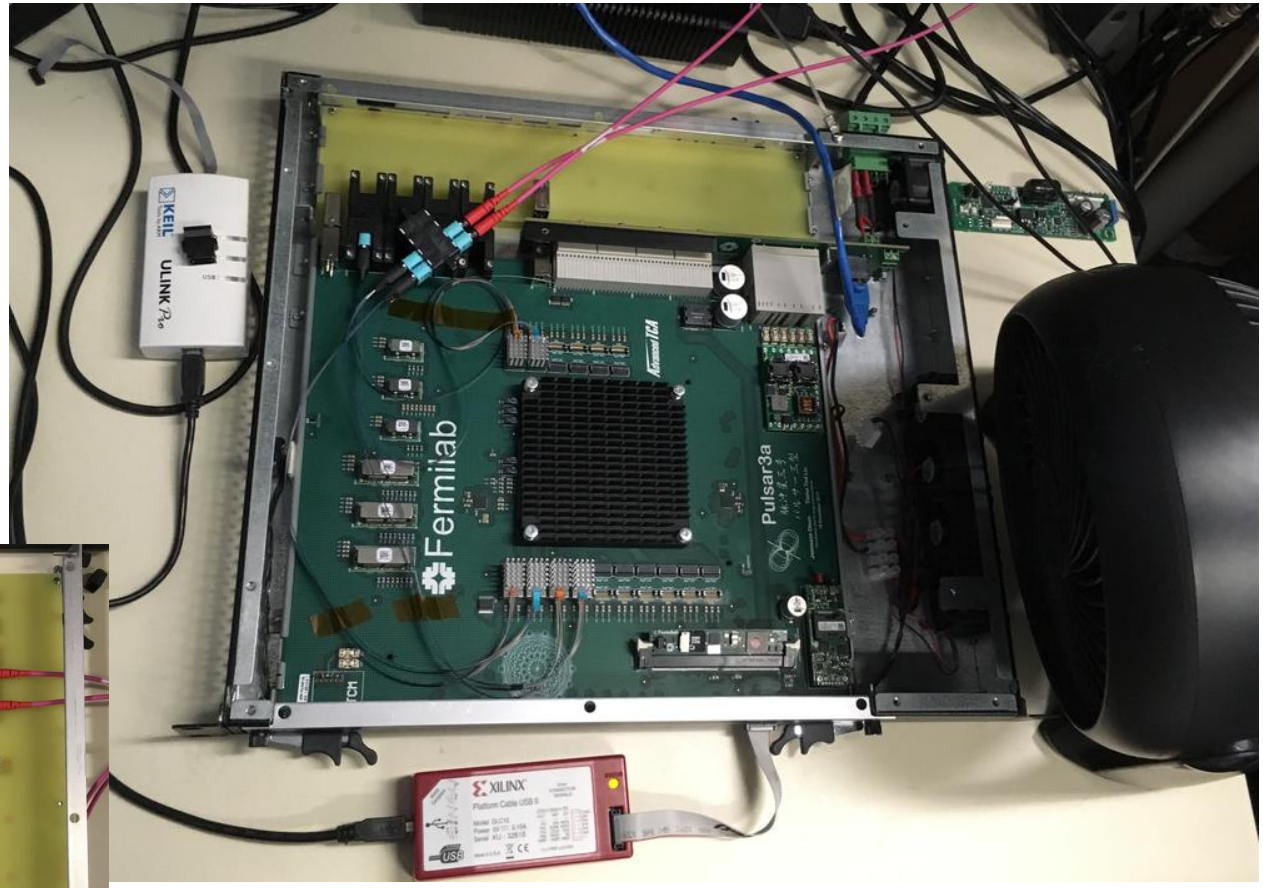


Pulsar2a/2b Expansion: Mezzanine Cards

- Single and Double wide FMC mezzanine cards
- Test high speed interfaces (LVDS, MGT) to Pulsar boards
- Expand processing power (2 x KU060 FPGAs)
- Standalone test platform for Pattern Recognition Associative Memory Devices
  - ASIC
  - FPGA
- Track finder board in the demonstration system
  - Zhen's talk on Monday



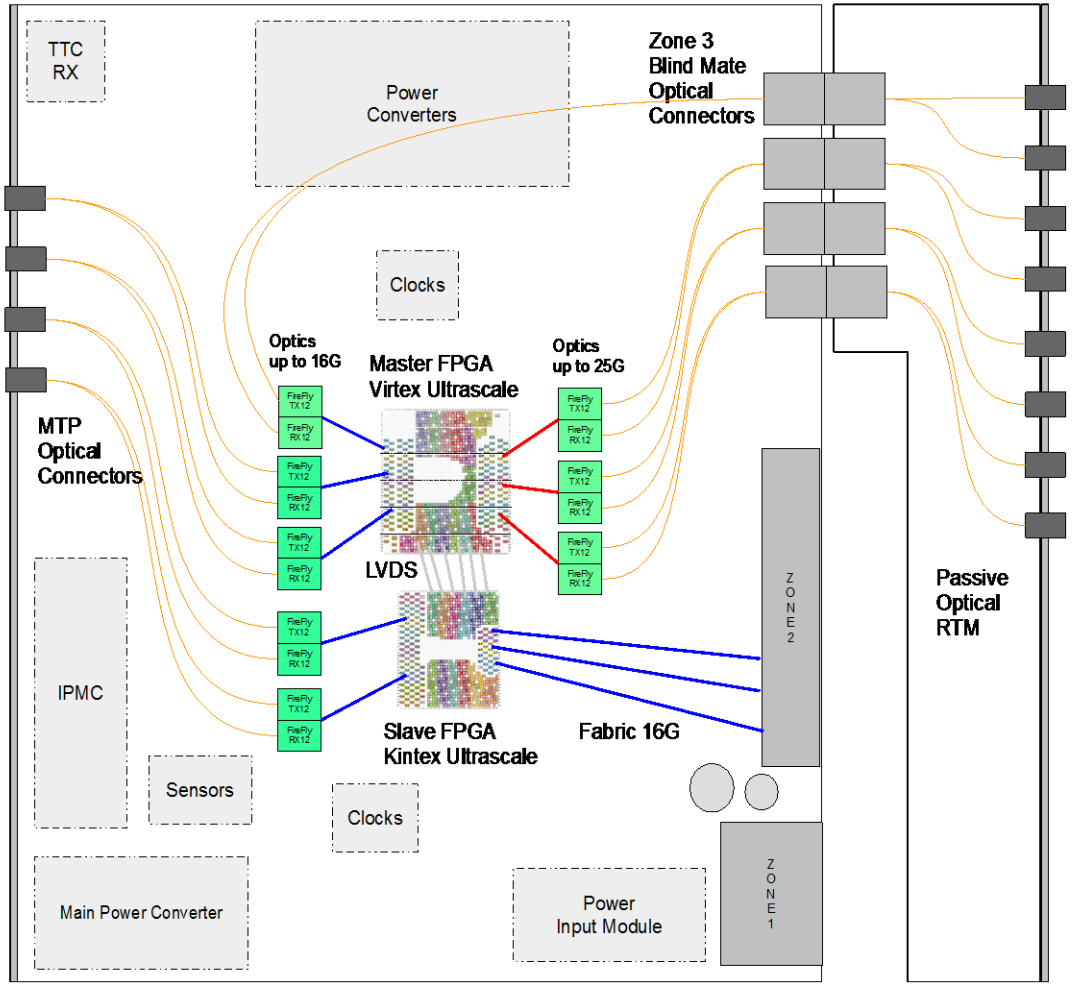
Pulsar3a (2017-2018)



CMS L1 tracking trigger R&D

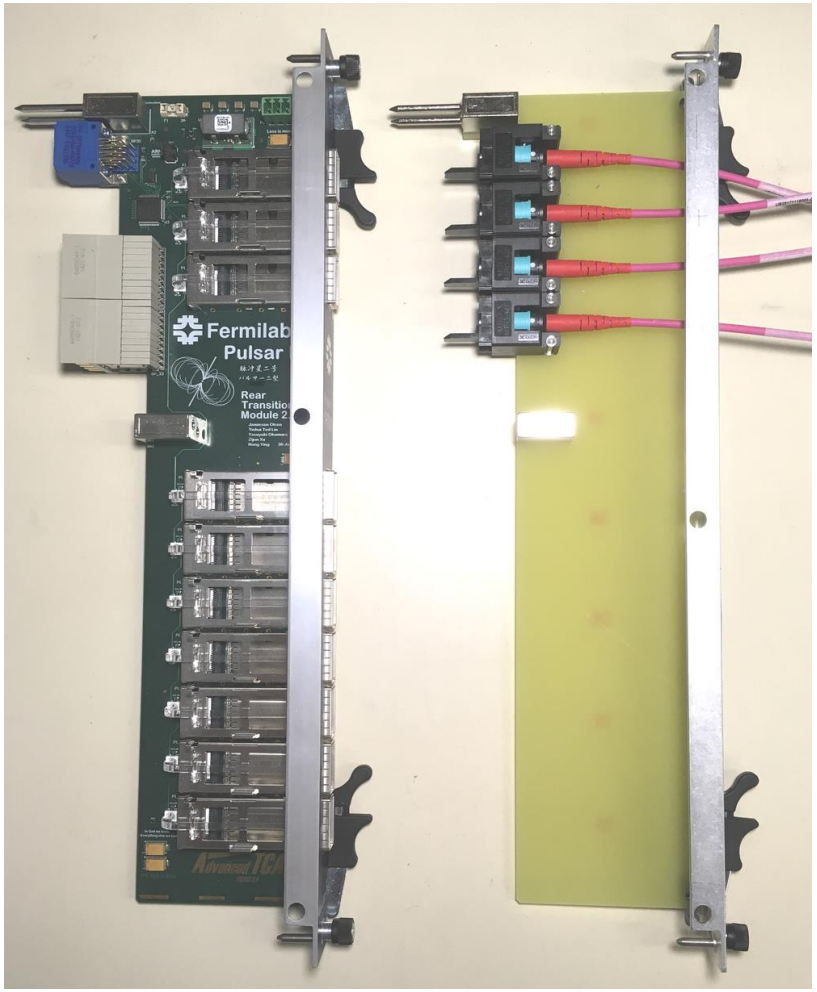
Pulsar3a: Improvements over Pulsar2b

- Fiber I/O bandwidth
  - 40 → 96 links
  - 10G → 16G/25G
- Full mesh backplane bandwidth
  - 10G → 16G
- Increased overall bandwidth
  - 1Tbps → 2Tbps
- LVDS local bus
- Logic resources
  - 690k LC → up to 5M LC
- Board simplification
  - Passive RTM
  - Mezzanines removed



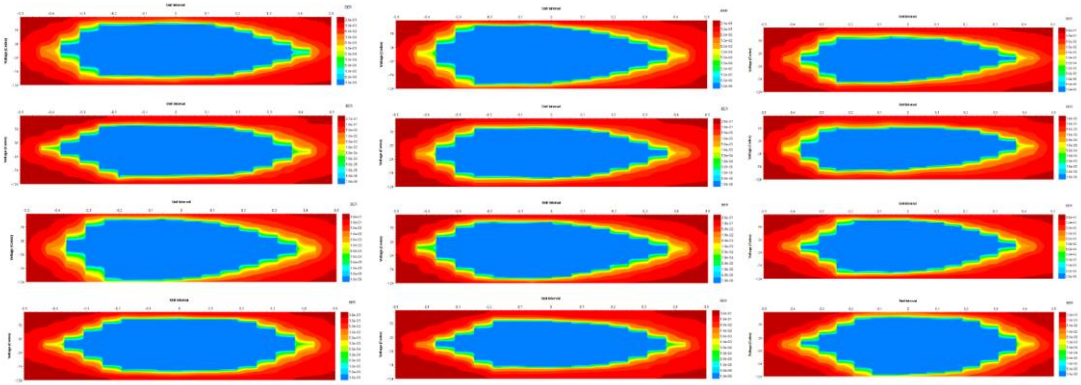
Pulsar3a: Rear Transition Module

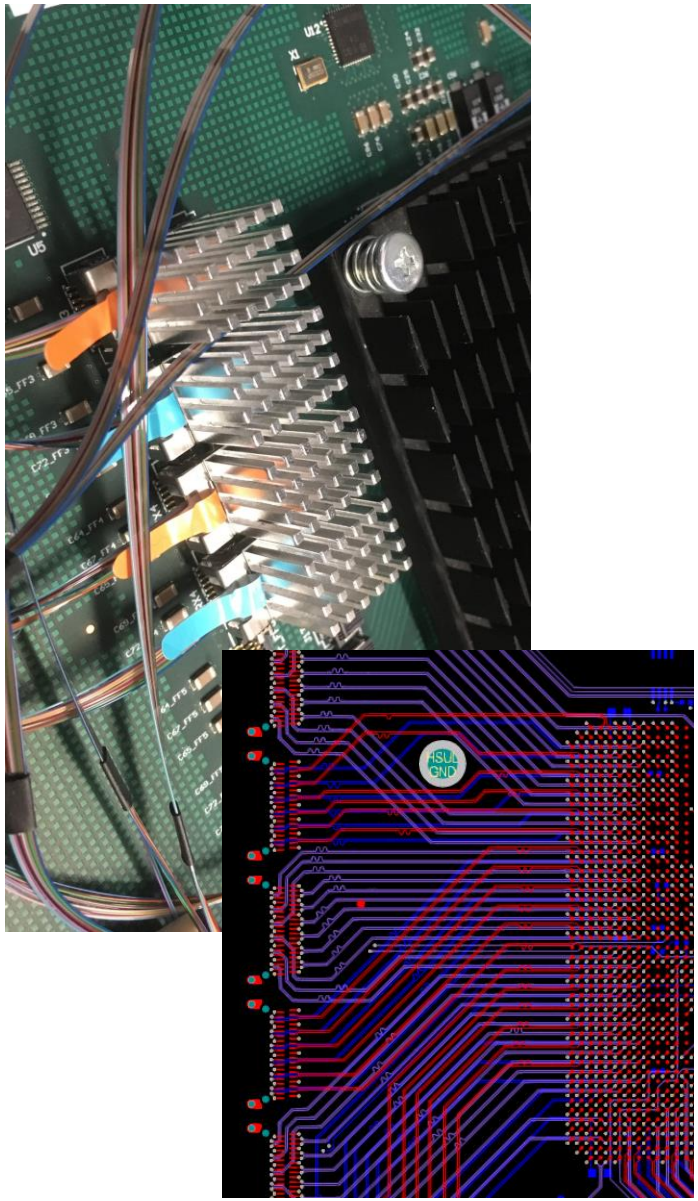
- Pulsar2a and Pulsar2b: optics on RTM
  - SFP+ and QSFP+ modules up to 10Gbps per lane
  - MMC microcontroller required
  - Hot swap, e-keying, other misc. IPMI stuff
  - Added complexity to IPMC software
  - Long high speed traces + Zone-3 connectors
- Pulsar3a: optics move inboard
  - Passive optical RTM uses Molex blind mate MTP connectors
  - Much shorter traces on Pulsar3a



Pulsar3a: Optics

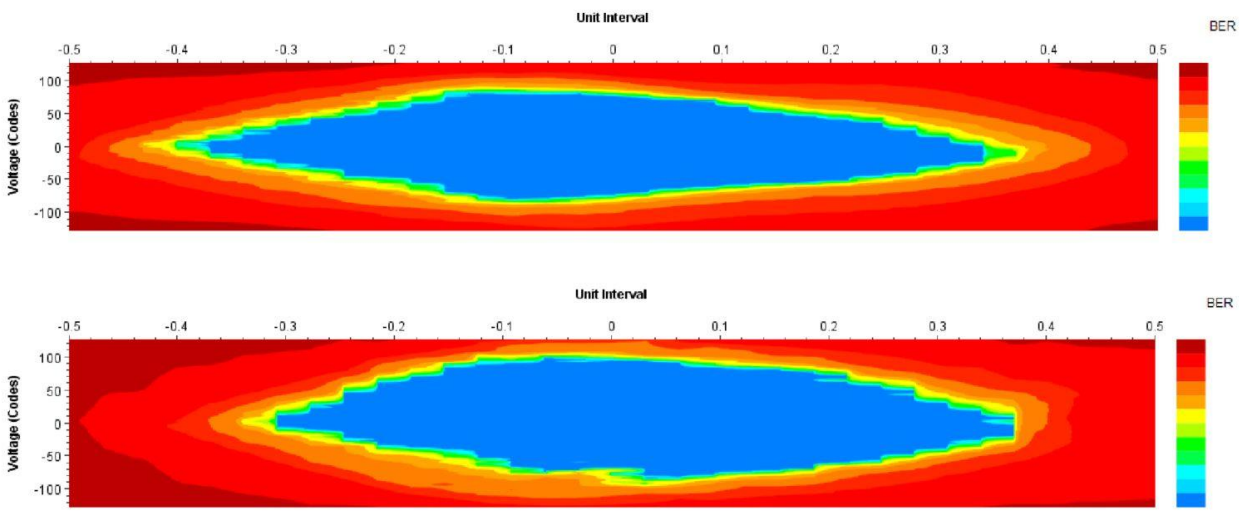
- SAMTEC Firefly x12 optical modules
- Up to 14Gbps per lane
- Preliminary results show RX margin looks good at 12.5Gbps PRBS7 with default settings
- BER $<10^{-14}$
- Ready for 28Gbps Firefly modules
  - 36 GTY transceivers up to 25Gbps
- Optical full mesh with external passive mixer box / patch panel



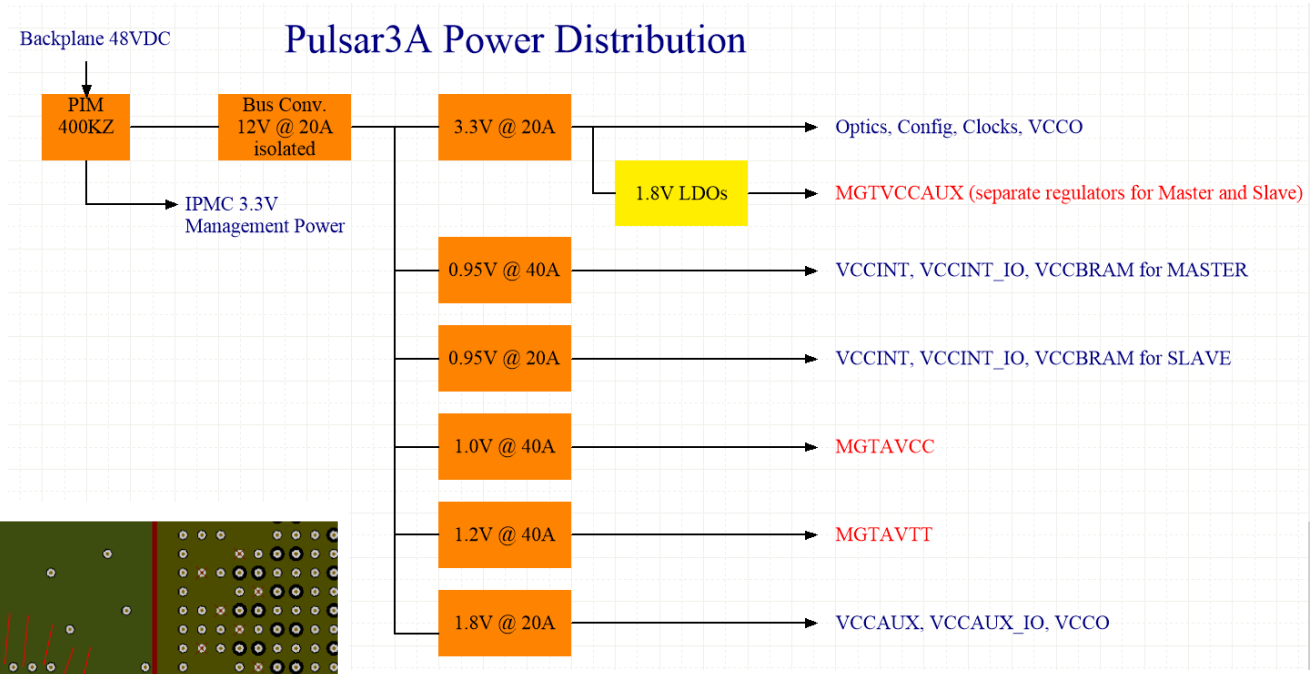


Pulsar3a: Backplane Fabric Interface

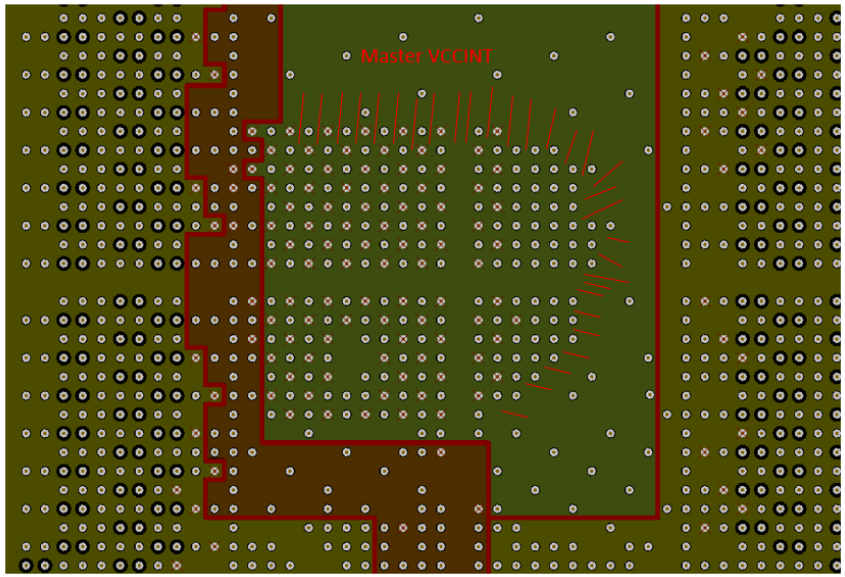
- Slave FPGA drives most full mesh channels
  - GTH transceivers up to 16Gbps in KU115 -2 speed grade
- Preliminary results look promising at 15.625Gbps
  - Loopback with Mini-backplane
  - Tests Pulsar3a PCB traces and backplane connectors
- Start backplane testing as soon as board #2 is ready

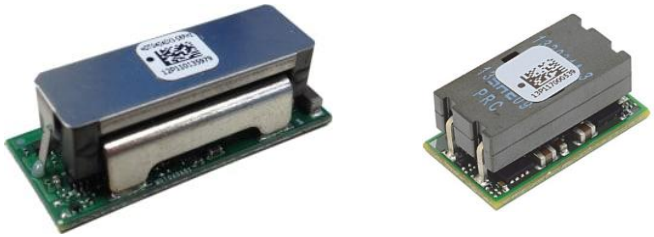


Pulsar3a: Power Distribution



Many high current power rails converge under the BGA. Split planes and lots of vias present challenges routing power to the FPGAs:





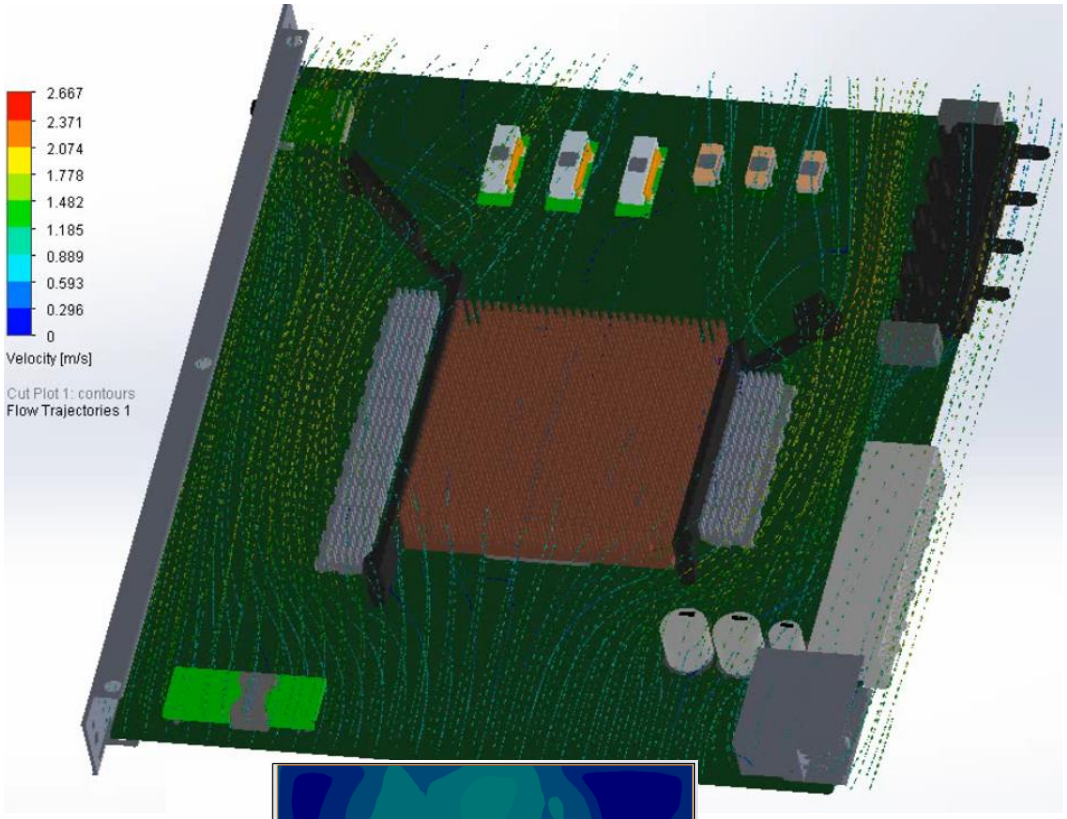
High efficiency non-isolated point of load switching regulators (40A and 20A)

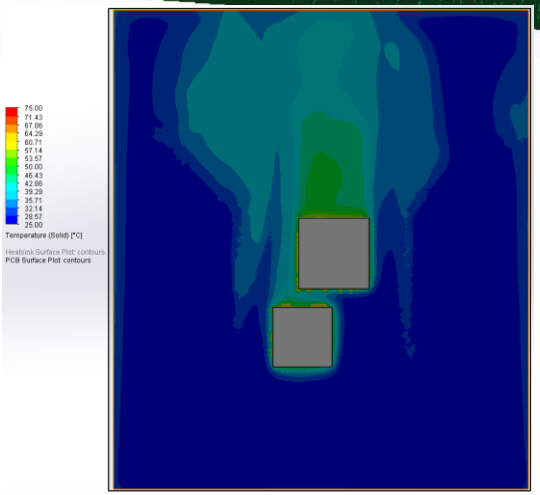
Pulsar3a: Telemetry

- Sensors all over the board
  - PMBus regulators report temperature, voltage, current
  - FPGA core temperature
- Firefly modules
  - Pages of status and control bits
- Programmable low jitter clock synthesis chips for MGT reference clocks
- All of these peripherals are I2C and connect to IPMC
- Continuously scanned by IPMC
- IPMI Sensor Data Records to Shelf Manager

Pulsar3a: Thermal

- Master FPGA: 60W
- Slave FPGA: 30W
- Airflow and heatsink modeling in Solidworks
- Improve airflow with 3D printed air baffles
- Several different heat sink designs ready for testing





Conclusion

- Pulsar3a was initially motivated by CMS L1 tracking trigger R&D and builds upon the experience gained from Pulsar2b and Pulsar2a
- Continue to pursue our design goals
  - General purpose FPGA platform
  - Scalable, flexible, interconnected
  - High bandwidth interconnects
- Presented a first look at the new Pulsar3a hardware testing
- Next steps:
  - More boards, more testing!
  - Future board revision: precision clock distribution