



# An FPGA Based Fast Linear Discharge Method for Nuclear Pulse Digitization

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**ABSTRACT** – Inspired by Wilkinson ADC method, we implement a fast linear discharge method based on FPGA to digitize nuclear pulse signal. In this scheme, we use a constant current source to discharge the charge on capacitor which is integrated by the input current pulse so as to convert the amplitude of the input nuclear pulse into time width linearly. Thanks to the high precision of TDC measurement that we have achieved in FPGA, we can increase the current value of the discharge to make the discharge time short, so as to obtain a small measurement of dead time. We have realized a single channel fast linear discharge circuit which contains only one dual supply amplifier, two resistors and one capacitor. The rest part can be implemented in an FPGA (Field Programmable Gate Array). Leakage current from the sensor would cause the base line drifting slowly, which can influence the measuring precision. Our method solve this problem without losing the linearity of measurement. We have built the circuit and experimental setup for evaluation. Using them to measure energy spectrums of PET detectors of PMT coupled with LYSO and LaBr<sub>3</sub> crystal, the energy resolution is 12.67% and 5.17% respectively. The test results show that our circuit is rather simple, stable and conducive for multi-channel integration.

## Introduction

Particle detectors often require front-end electronics to digitize the output analog pulse signals with short dead time, high energy resolution, large measurable dynamic range and capability for multi-channel integration. For example, high resolution PET detector module based on large continuous crystals need such a front-end electronics [1]. Traditional methods, such as waveform digitization scheme include high speed ADC sampling, Time over threshold are not well suitable for the case. On the basis of Wilkinson ADC scheme, combining our high precision time-to-digital (TDC) technique, a field programmable gate array (FPGA) based fast linear discharge method is proposed in this paper. Its advantages of short dead time, high precision and simplicity makes it very suitable for the PET detectors

know, FPGA digital high output supply a fixed voltage and the input negative port of amplifier is virtual short to ground, so we can get a constant voltage difference on resistor R<sub>1</sub>, so the current on resistor R<sub>1</sub> is constant which will discharge the charge on capacitor linearly. Meanwhile, R<sub>2</sub> works as a pull-up resistor and does not drain the charge on capacitor at all. The discharge process come to an end when the voltage on capacitor cross the threshold voltage again. Then the LVDS comparator flips which leading to the tri-state output return to high resistance. All in all, an input pulse from sensor will lead to a rectangular pulse whose width is linear to the charge of input pulse. Measuring the rectangular pulse width using a TDC in FPGA will obtain the amplitude of input pulse we want.

## Method and Experiment Circuit

We have realized the linear discharge circuit of single channel shown in Fig. 1. The circuit is composed of a dual supply amplifier, two feedback resistors, one feedback capacitor and an FPGA. An LVDS comparator and a TDC block are implemented in the FPGA. The output of amplifier is connected to the positive input port of LVDS comparator directly to compare with a fixed low threshold voltage. The output of the comparator is connected to the middle of two feedback resistors by a tri-state output buffer of FPGA.

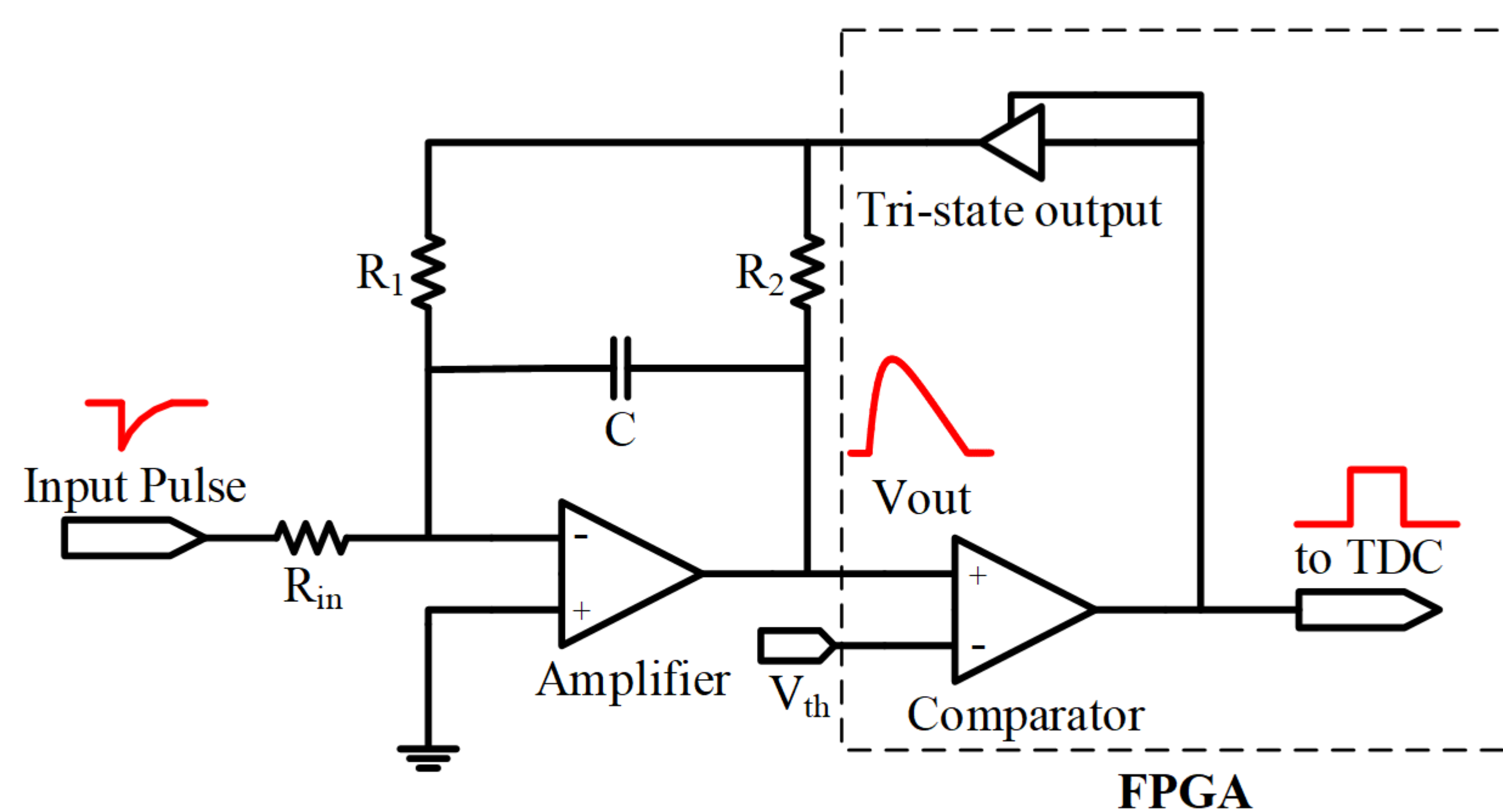


Fig. 1. The basic circuit of fast linearly discharge method. The comparator and TDC module are implemented in the FPGA.

When a signal does not arrive, the charge accumulated on capacitor by noise or leakage current will be released through the feedback resistors R<sub>1</sub> and R<sub>2</sub>, which keeps the voltage on capacitor stable below the threshold voltage. And the tri-state output of FPGA is high resistance. When a signal arrives, the voltage accumulates on capacitor beyond the threshold voltage, causing the comparator to flip and the output of the tri-state output to convert from high resistance to digital high output. As a result, the middle of two feedback resistors become pulled up rather than hanging. As we

## Test Result

A realistic board with Xilinx Kintex-7 FPGA was built to evaluate the performance of fast linear discharge method. The detector we use is HAMAMATSU R9800 PMT together with large continuous crystals LYSO and LaBr<sub>3</sub>. A dual supply inverting amplifier AD8065, one capacitor and two resistors make up the analog module outside the FPGA. The energy spectrum of <sup>22</sup>Na  $\gamma$  source is measured with this circuit.

Test result shows that the nonlinearity of our circuit can be reduced to 0.01%. The 511KeV and 1274KeV energy peak is visible so we can calibrate the conversion between energy and discharge time with them. After calculation, we can get energy resolutions of 511KeV peak 12.67% of LYSO crystal and 5.17% with LaBr<sub>3</sub>. The test performance evidents that this circuit works well as expected.

## Conclusion

We have realized a single channel fast linear discharge method to digitize nuclear pulse with a simple circuit structure combined with an FPGA. The amplitude of nuclear pulse from detector is converted into pulse width for subsequent measurement and processing. The test result shows that this scheme has advantages of high linearity and high energy resolution. Compared with traditional amplitude digitization scheme, this method has a shorter dead time and a larger measurable dynamic range, and consist of fewer passive components which is conducive to multi-channel and high event rates applications.

## References

- [1] Wang Yonggang, Zhu Wensong, and Chen Jun, "A novel nuclear pulse digitizing scheme using time over dynamic threshold", 2011 IEEE Nuclear Science Symposium Conference Record, N50-5, p2174-2179