Contribution ID: **585** Type: **Poster presentation**

Design and test of sTGC front-end electronic interface board

Thursday, June 14, 2018 3:50 PM (15 minutes)

Small-strips Thin Gap Chamber(sTGC) is one of the detectors on new small wheel(NSW) which is an important part of Atlas Phase-I upgrade. We will present our design and test results for the sTGC front-end electronic interface board, which aims to demonstrate the functionality and interface of ASICs on the sTGC front-end board. VMM, TDS(Trigger Data Serializer), SCA(Slow Control Adapter) and ROC(Read-out Controller) are the new ASICs designed for sTGC, which has complex functions and massive ports. The sTGC front-end ASICs interface board provides us a good chance to study and understand the configuration, function test and data transition of these ASICs, find potential problems and gain experience. On the other hand, due to the output of TDS has a speed of 4.8Gbps, which requires the jitter clean clock, the interface board has SMA test point for both the input clock and the clock output of ROC in order to validate the clock jitter. The interface board also have the same connectors so it can be connected to other electronics to demonstrate the performance of high speed output with long cables.The studies on the interface board will provide us chances to understand the performance of the sTGC front-end ASICs and give feedback to the ASIC design and guidance for the design of the final sTGC front-end boards.

Description

STGC DAQ board

Institute

University of Washington

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Country

USA

Minioral

Yes

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Session Classification: Poster 2

Track Classification: Front End Electronics and Fast Digitizers