Design and Evaluation of LAr Trigger Digitizer Board in the ATLAS Phase-I Upgrade

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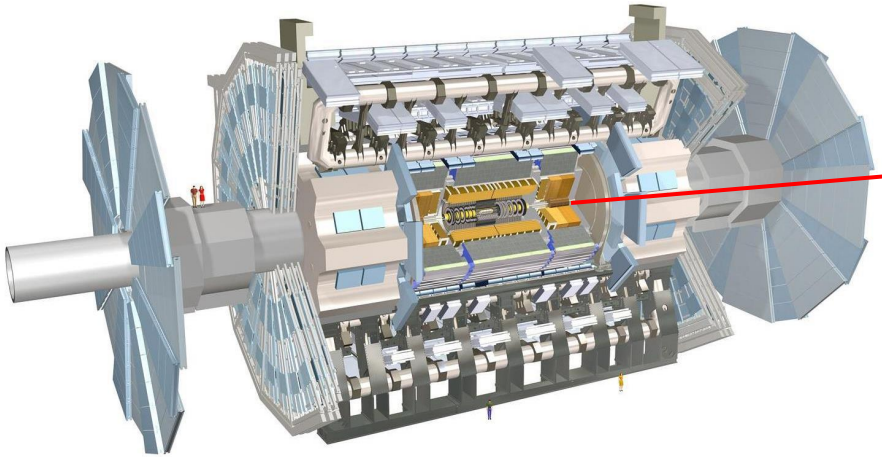
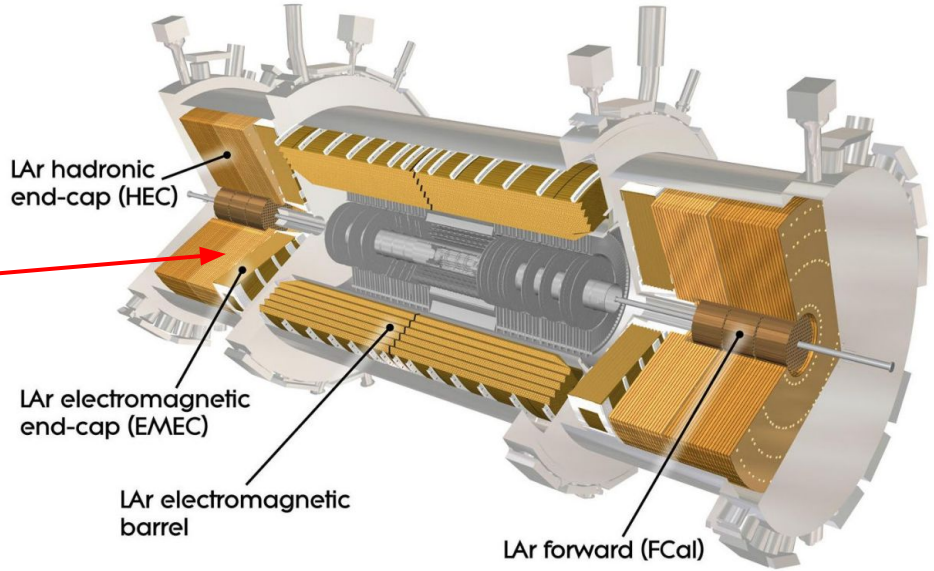
ATLAS EXPERIMENT

ATLAS LAr calorimeter

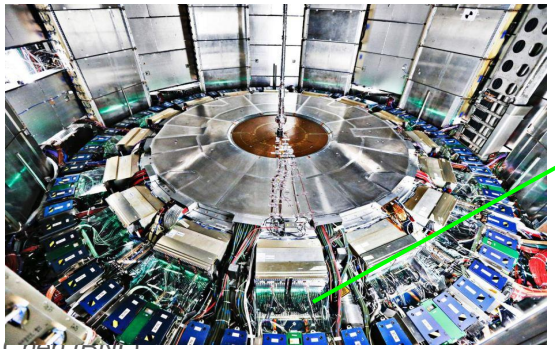
- ~180k channels for the full readout of the electromagnetic barrel and endcap (EMB and EMEC), hadronic (HEC) and Forward (FCAL) calorimeters.
- 1524 Front End Boards (FEB)
- 3584 channels for analog trigger readout

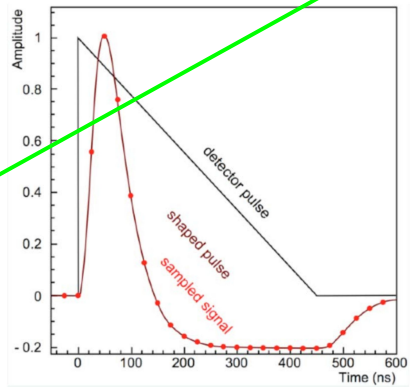


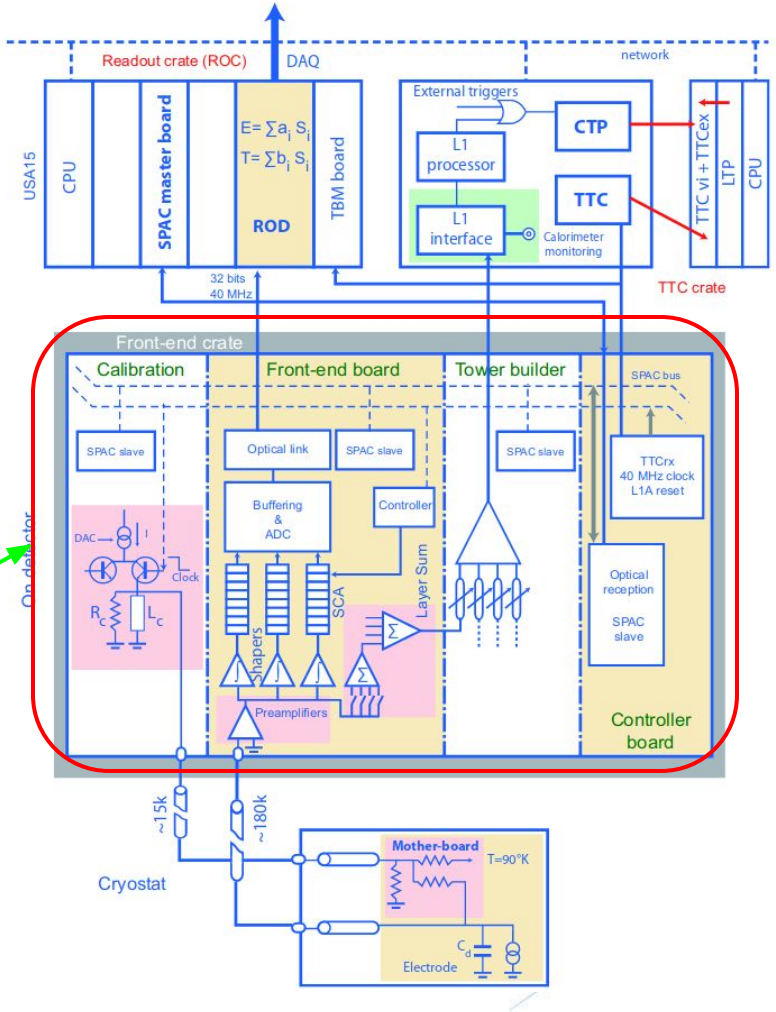


Current LAr electronics

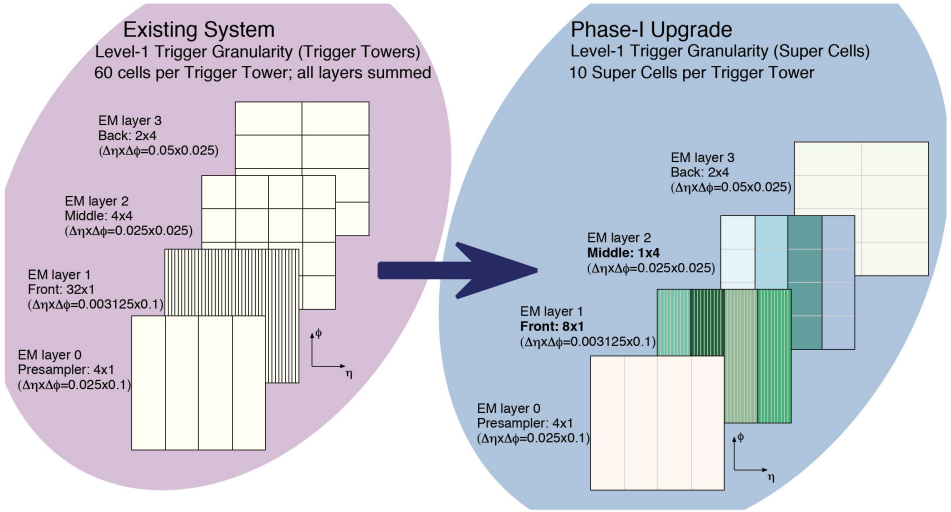
- 128 channel per FEB, 8 FEBs per ROD
- 32 trigger towers of (Δ_η x Δ_ϕ= 0.1x 0.1) per Tower Builder Board (TBB)
- ***Main readout***
  - *Cell signals are amplified, shaped, sampled at 40 MHz, digitizd and transmitted at 100 kHz upon L1A trigger*
  - ***Will be upgraded in HL-LHC***
- ***Triggr readout***
  - *Sums signals from Layer Sum Board (LSB) to form trigger towers, and sends them to L1Calo system*
  - ***To be upgraded in Phase-I***





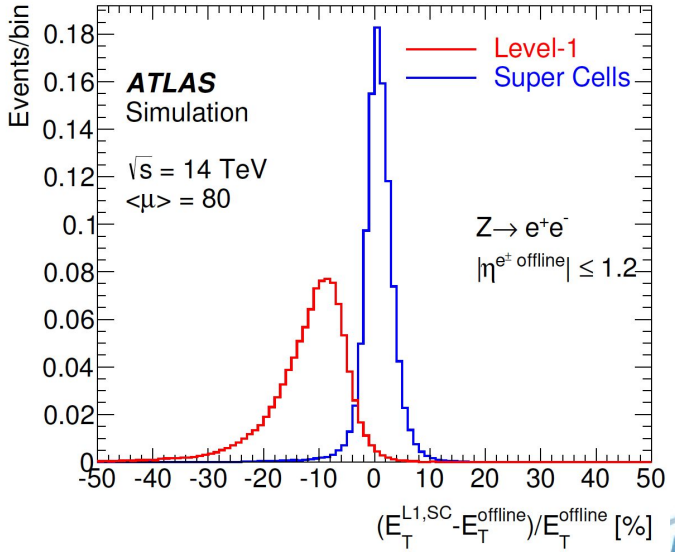


Phase-I upgrade



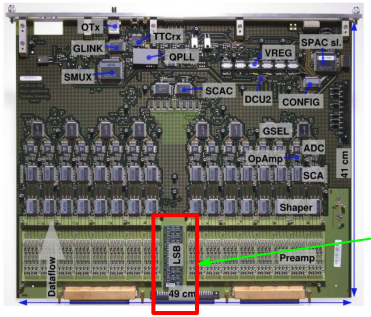
Layer		Elementary Cell	Trigger Tower		Super Cell	
		$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$
0	Presampler	0.025×0.1	4×1	0.1×0.1	4×1	0.1×0.1
1	Front	0.003125×0.1	32×1		8×1	0.025×0.1
2	Middle	0.025×0.025	4×4		1×4	0.025×0.1
3	Back	0.05×0.025	2×4		2×4	0.1×0.1

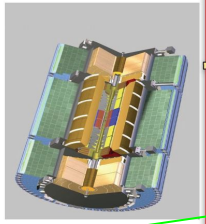
- ***10* times finer granularity**
  - *Keep layers information*
  - *Finer layer segmentation: Δ_η x Δ_ϕ= 0.025 x 0.1 for **front** and **middle** layers*
- Better energy resolution
- Better background rejection



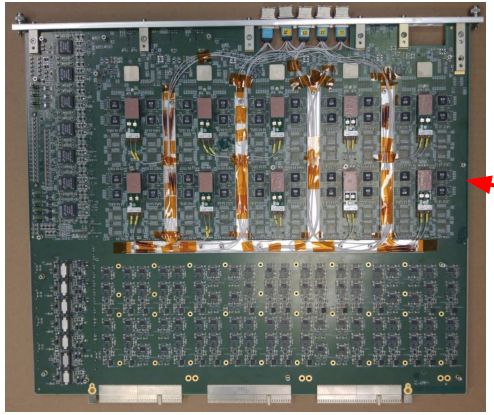
Difference from offline reconstructed energies

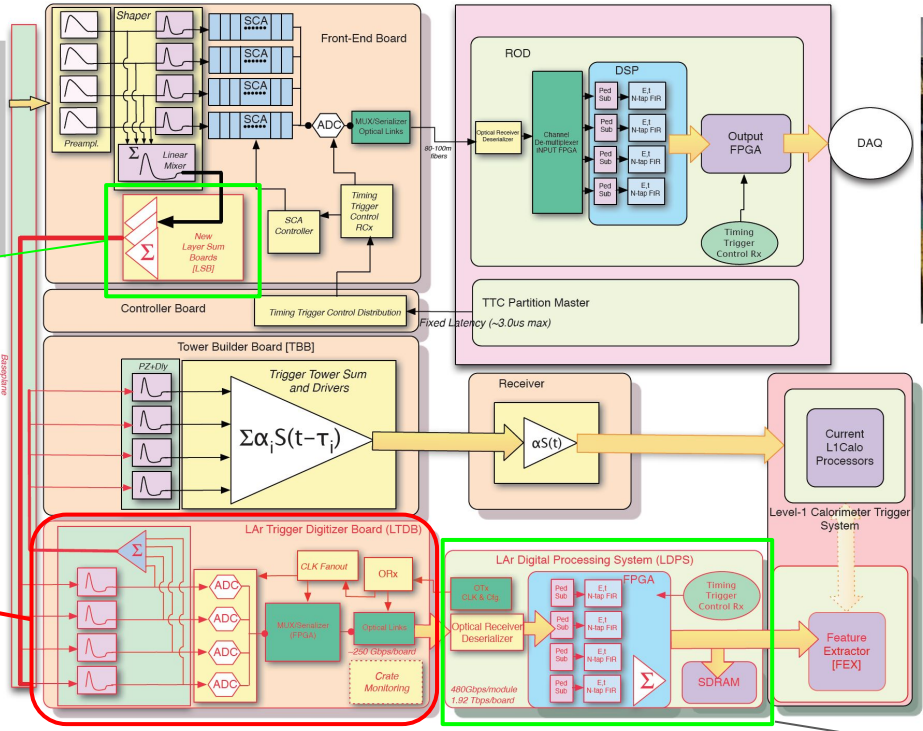
Phase-I upgrade



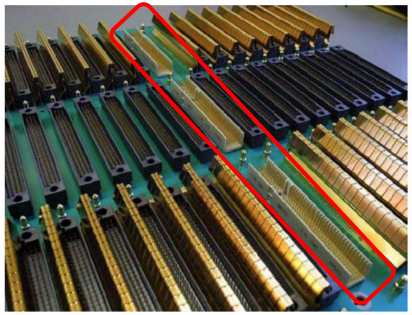


***L**ayer **S**um **B**oard mezzanine*

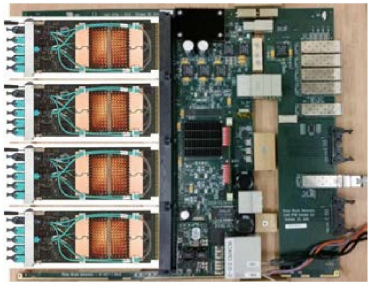




Slot for LTDB

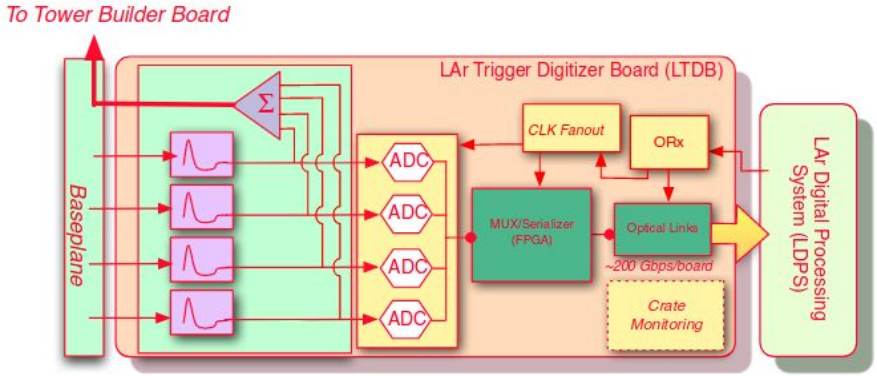


Baseplane



***L**Ar **D**igital **P**rocessing **S**ystem*

LTDB in Phase-I upgrade



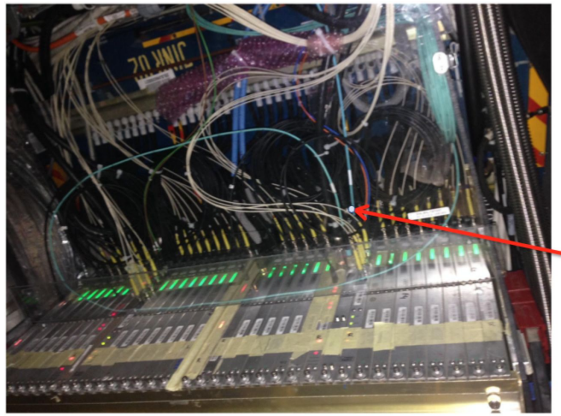
- To LDPS:
  - Digitizes up to **320** SC in 40 Msps and sends the information to LDPS via **40** optical links in **5.12 Gbps**
- To Tower Builder Board (TBB):
  - *Sums front and middle layers SC signals and send them to current TBB*
- With FELIX
  - *Clock and TTC signals are from ATLAS FELIX (Front End LInk eXchange) system via 5 GBT links*
  - *Control, calibration and monitoring is also via GBT links*

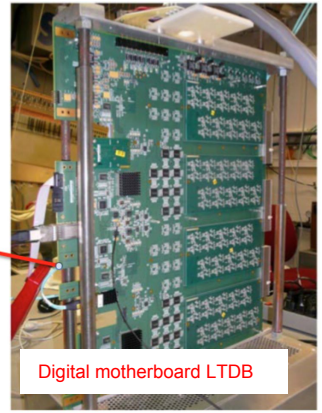
LTDB Type	Channels	LTDB #
EMB	290	64
EMEC Std	312	32
EMEC Spc 0	240	8
EMEC Spc 1	160	8
HEC	192	8
FCAL 0	192	2
FCAL 1	192	2
Total		***124***

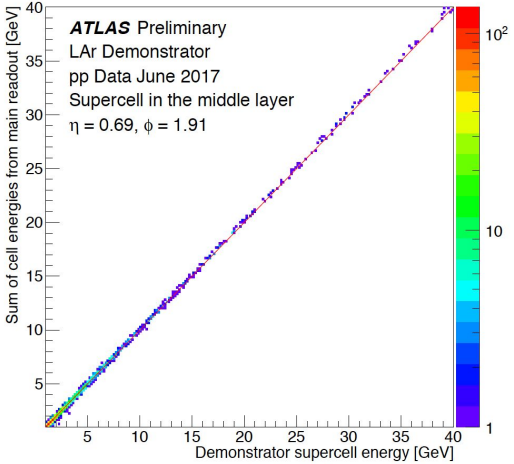
- ***124*** *LTDBs to be installed to handle ~34000 Super Cells; ~25 Tbps*
- *LTDBs will need to operate beyond the HL-LHC upgrade*

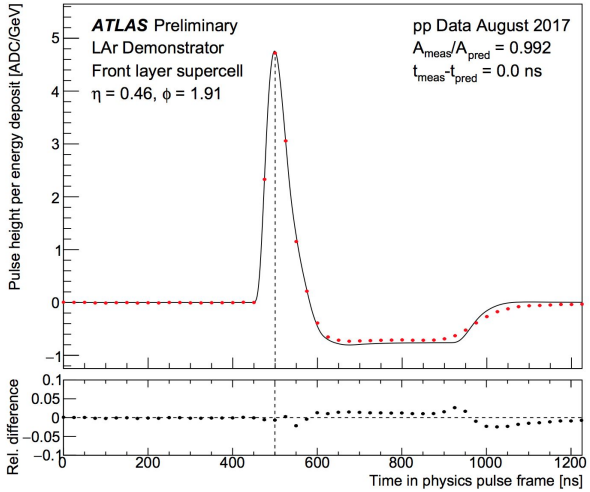
Evolution of LTDB: demonstrator

- All COTS components
  - *Pre-selection irradiation testing for the analog COTS components (ADC, DC-DC modules...)*
- Two versions: analog motherboard or digital motherboard
  - *4/10 FPGA, 40 4.8 Gb/s links to back-end*
- ***LTDB demonstrator boards have been successfully installed on detector in July 2014***
- ***Data taken shows satisfactory performance***

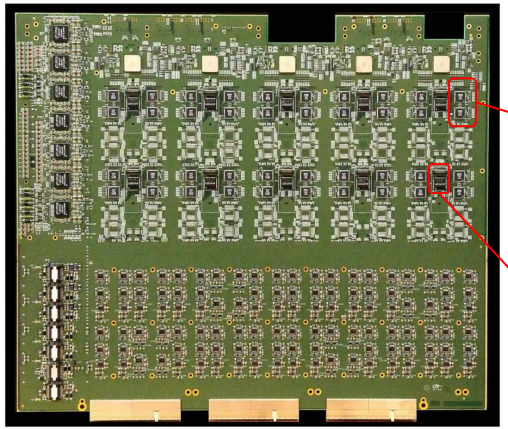


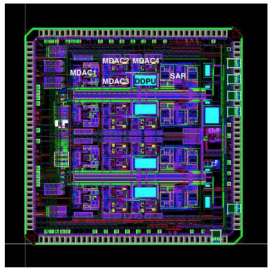


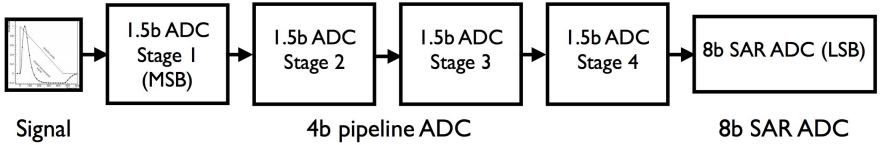




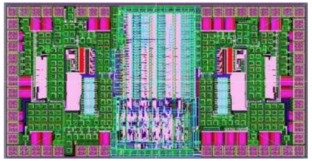
ASICs on pre-prototype and prototype board



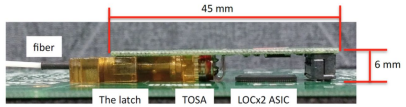


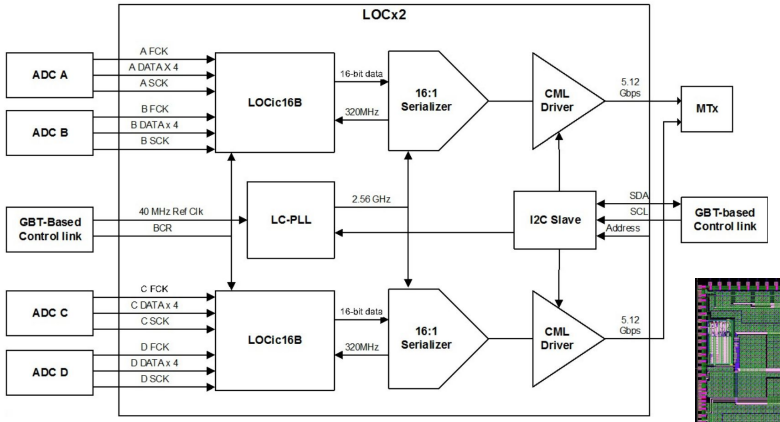


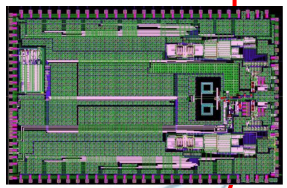
12-bit quad-channel 40 Msps radiation-hard pipeline ADC: 3.6 x 3.6 mm, 72 pins QFN



Laser driver LOCld: Dual channel VCSEL driver

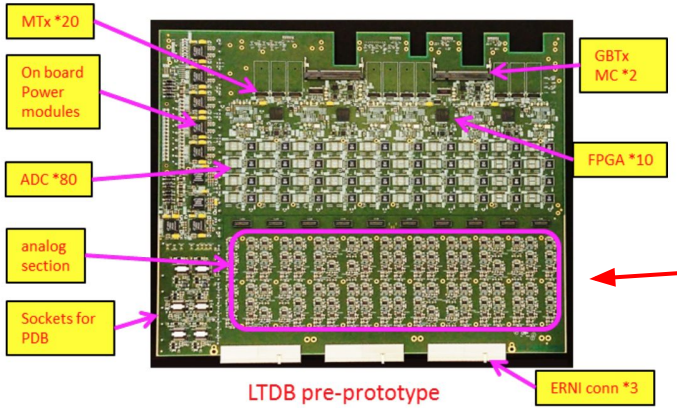


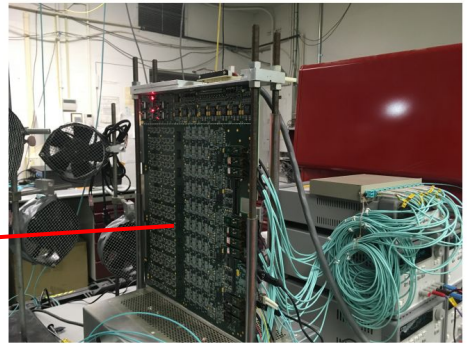


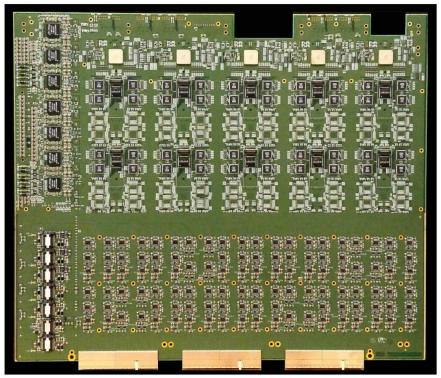


LOCx2: serializer to organize 8 ADC channels into 5.12 Gbps link: 6.036 x 3.68mm, 100 pins QFN

Evolution of LTDB: pre-prototype & prototype

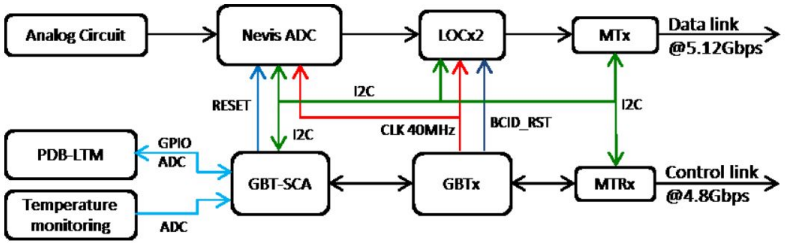






Prototype

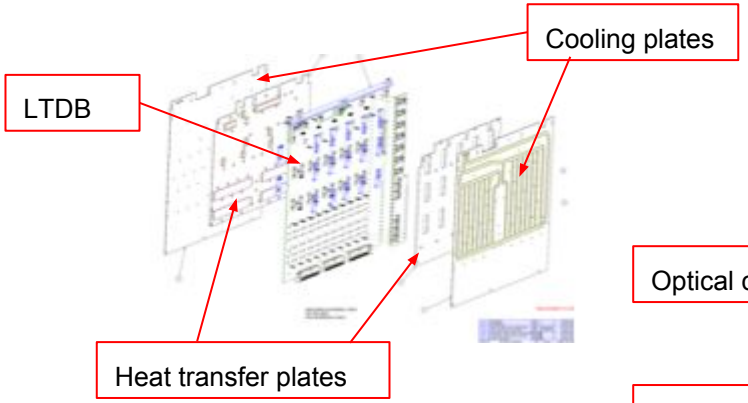
- ***Pre-prototype: 10 Artix-7 FPGAs + 80 NEVIS ADCs + 2 GBTx***
- ***Prototype: 20 LOCx2 + 80 NEVIS ADCs + 5 GBTx & GBT-SCA***
- *Analog and digital parts are designed by different institutes. Gerber files are merged together for fabrication.*
- *24-layers PCB.*
- ***Power mezzanine is used: easy to be replaced for HL-LHC.***

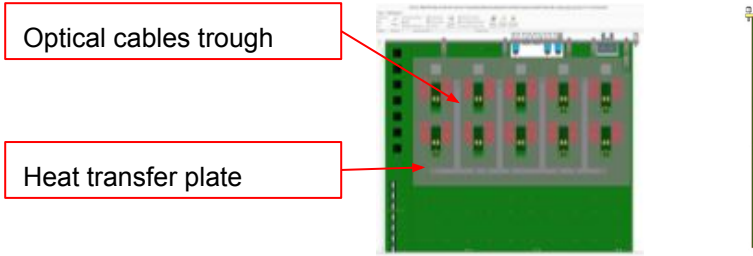


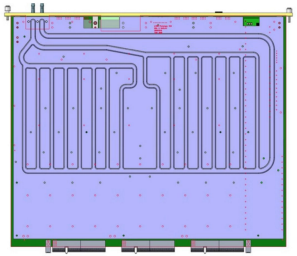
Evolution of LTDB: pre-production

- *Compared to the prototype: clocks for LOCx2 are changed from GBTx DCLK to CLKDES, to solve the LOCx2 phase unstable issue.*
- *Packages & functions of all ASICs are verified.*
- *All LTDB functions are verified at BNL, CERN LAr EMF.*
- ***Two boards were installed on the detector in UX15 in early 2018.***

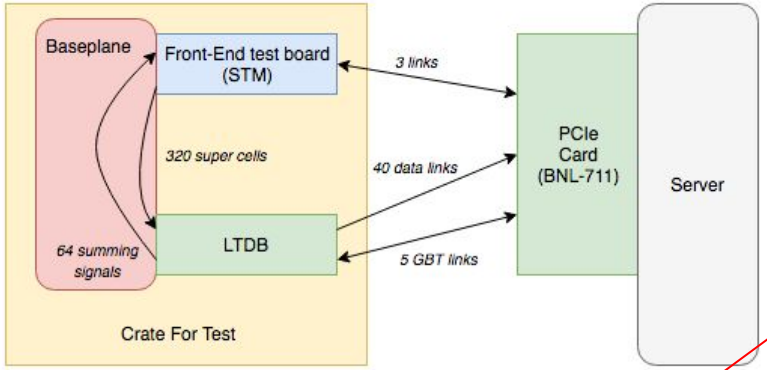
LTDB pre-production

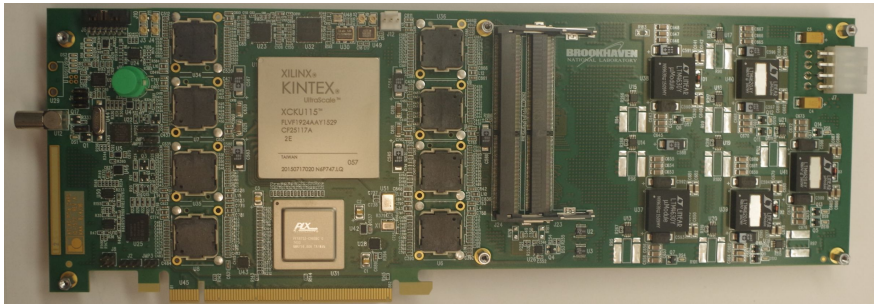




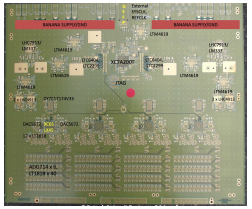


Test stand for production



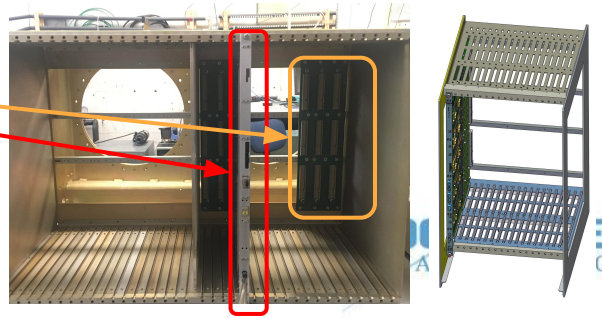


BNL-711

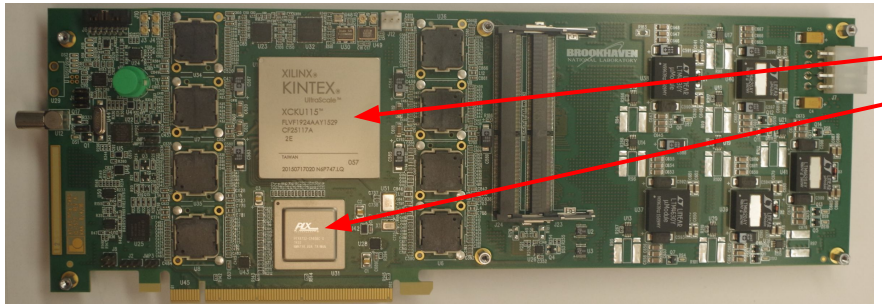


Front-end STM board

- To test the 124 LTDB production boards, a full test setup is under developing.
  - *PCIe card: (fully tested)*
  - *Front-end test board: (under testing)*
  - *Baseplane: (under testing)*
  - *Custom crate: under designing, for Multiple STM & LTDB*

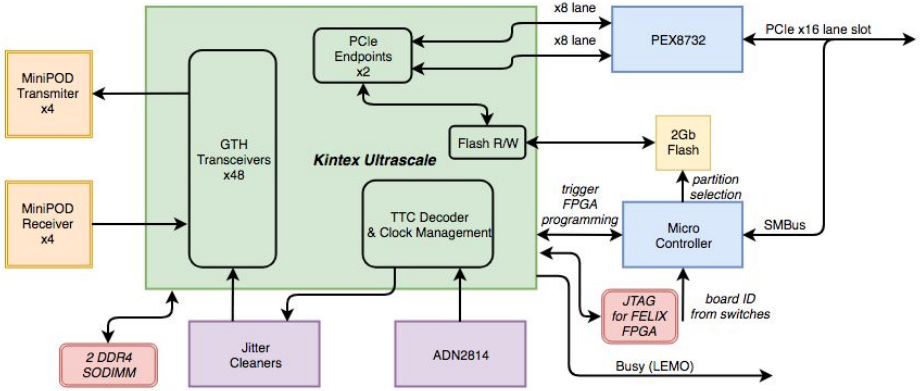


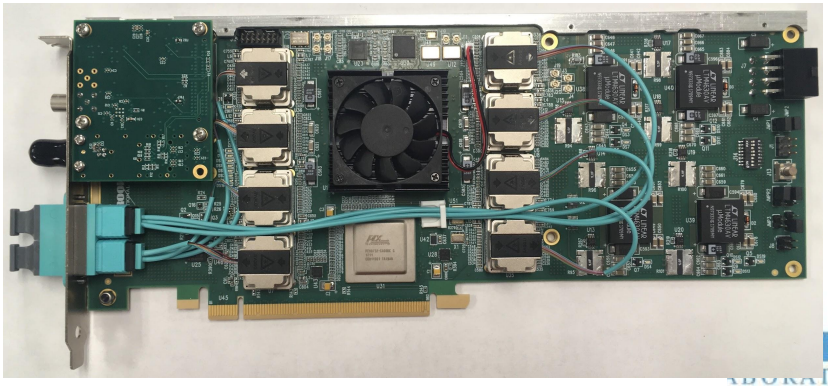
LTDB test stand: BNL-711 PCIe card



BNL711

- *Xilinx Kintex Ultrascale FPGA: XCKU115*
- *PCIe Gen3 16-lane*
- *Supports 2 DDR4 SODIMM memory up to 32GB*
- *48 bi-directional optical links up to 14 GB/s*
- *Support to interface ATLAS TTC system*
- *On-board 0-delay jitter cleaner*
- *16-layer PCB*
- *Version 2: DDR4 are removed. It is used in*
  - *ATLAS Phase-I readout system FELIX*
  - *TPC and MVTX readout in sPHENIX project*
  - *ProtoDUNE-SP readout*

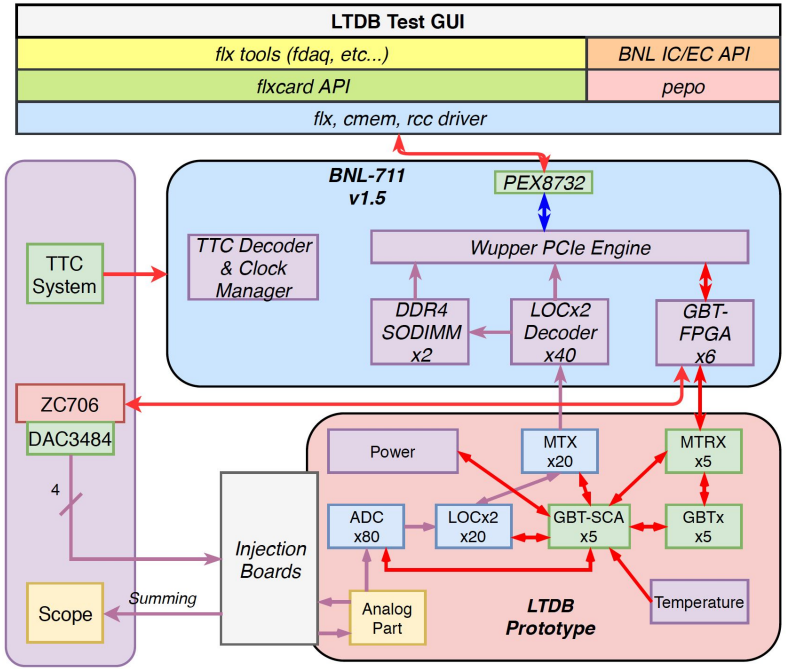


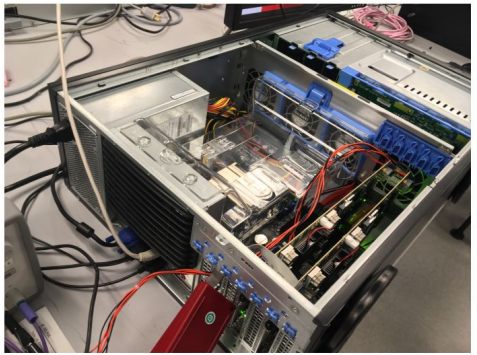


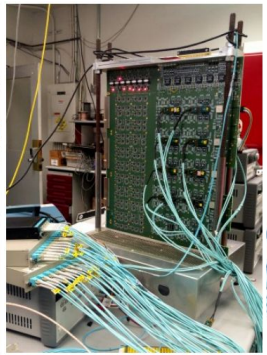
BNL712

Current LTDB test stand

- The test system based on BNL-711/712
  - *TTC clock and signal distribution (x5)*
  - *ASICs control & calibration*
  - *ADC data decoding and buffering (x40)*
  - *power control, V/C/T monitoring*
  - *3 links are reserved for control and readout the front-end analog test board STM*
- ZC706 + DAC card (16-bit, 1.25Gsps) for LAr signal generation, to be replaced by STM.
  - *signals are sent to LTDB via 3 injection boards.*

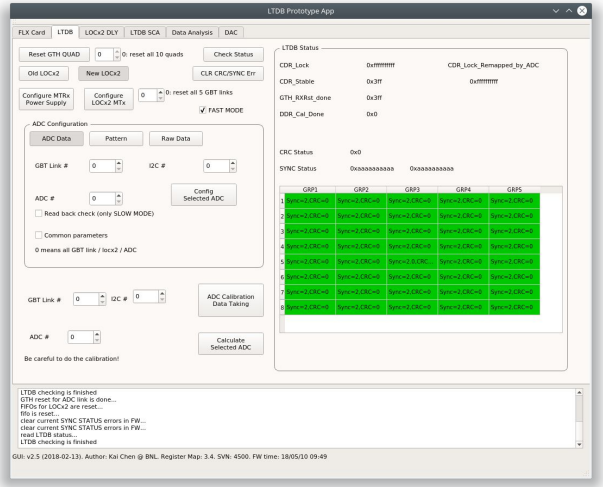


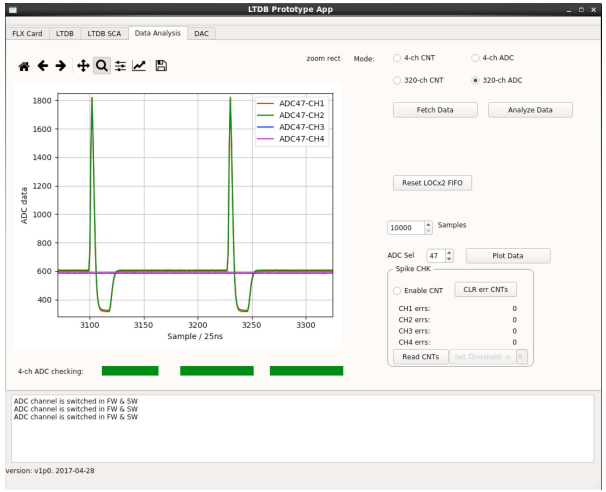




Software development for the LTDB test

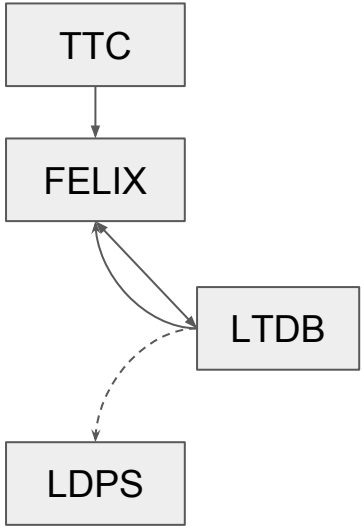
- Software: based on low-level tools from ATLAS FELIX project (***fdaq***, ***pepo***, *etc*).
  - A python API is developed to control GBTx and GBT-SCA via IC & EC bits in GBT link.
  - Scripts and the GUI application
    - *Configure GBTx via GBT link (with IC/EC API), configure all ASICs via GBT-SCA (with IC/EC API): GPIO and I2C ports.*
    - *Calibration of all 80 ADCs and clock phase for LOCx2 chips.*
    - *Controls the power, and monitor voltage, current and temperature.*
    - *DAC output waveform control (amplitude, phase, LAr pulse type).*
    - ***Different modes of data taking.***

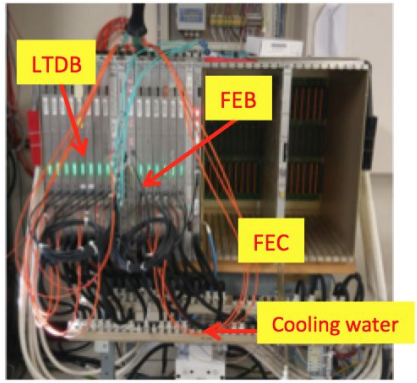


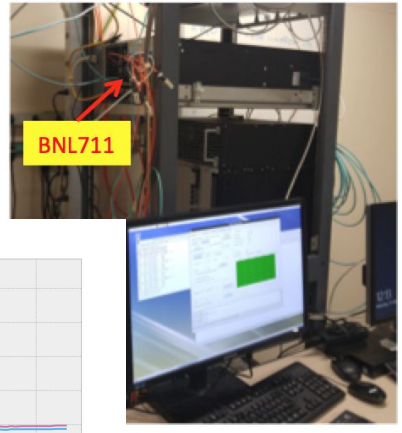


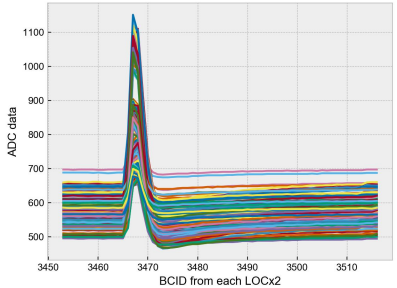
Test at CERN LAr EMF

- Setup at **E**lectronics **M**aintenance **F**acility:
  - FELIX distributes clock, BCR to LTDB
  - FELIX controls/monitors/calibrates LTDB
  - SC data can be readout by:
    - *FELIX (temporary solution)*
    - *LDPS (integration is ongoing)*
- Tests carried out:
  - All 40 data links are **stable**
  - **Fixed latency** for all LTDB channels
    - d*elay from injected pulse to the digitized ADC signal latched by LOCx2 are same*
  - **Mapping** verification of SC, and summed signal to TBB
  - Noise and crosstalk test for legacy trigger readout

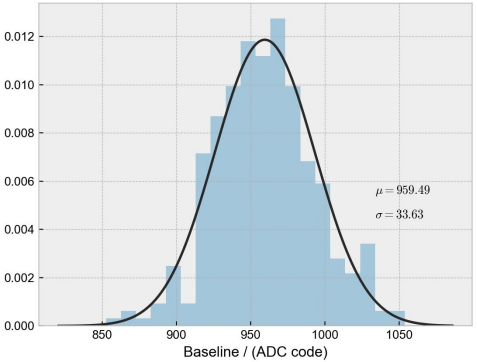




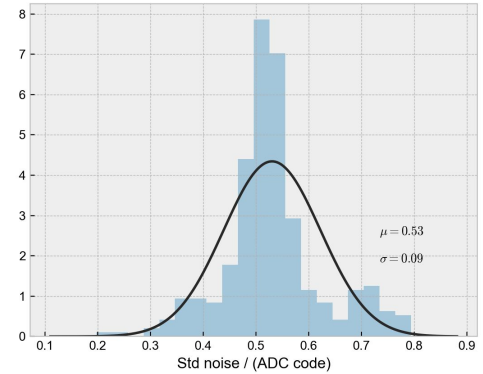




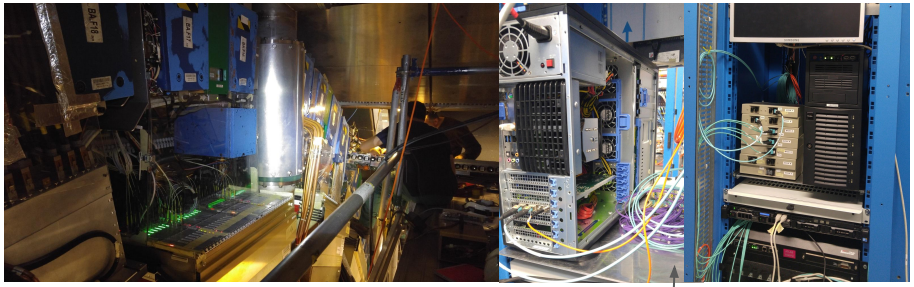
Test results on detector



Pedestal distribution



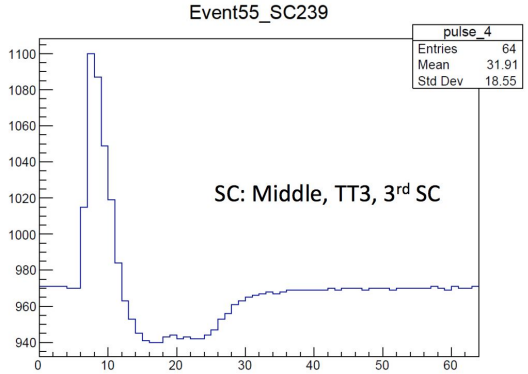
Noise distribution

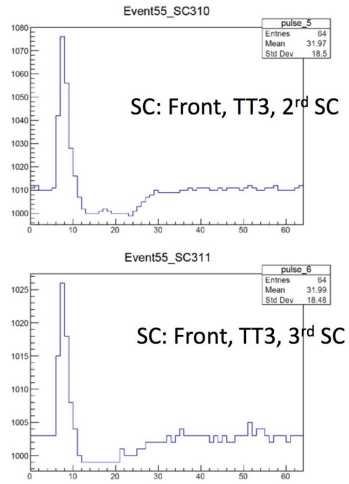


LTDBs in UX15

FELIX in USA15

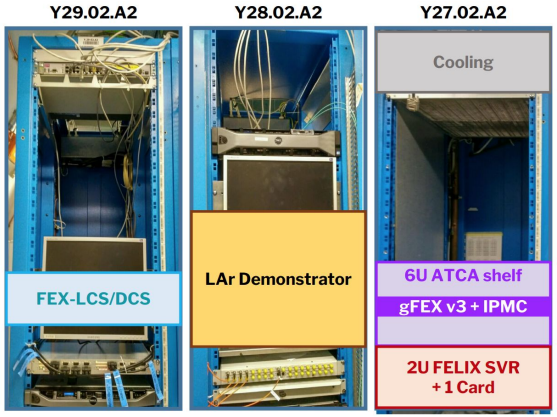
In file tmpdataL1A-180503-003412.data
→ 2018 May 3rd, 0:34.

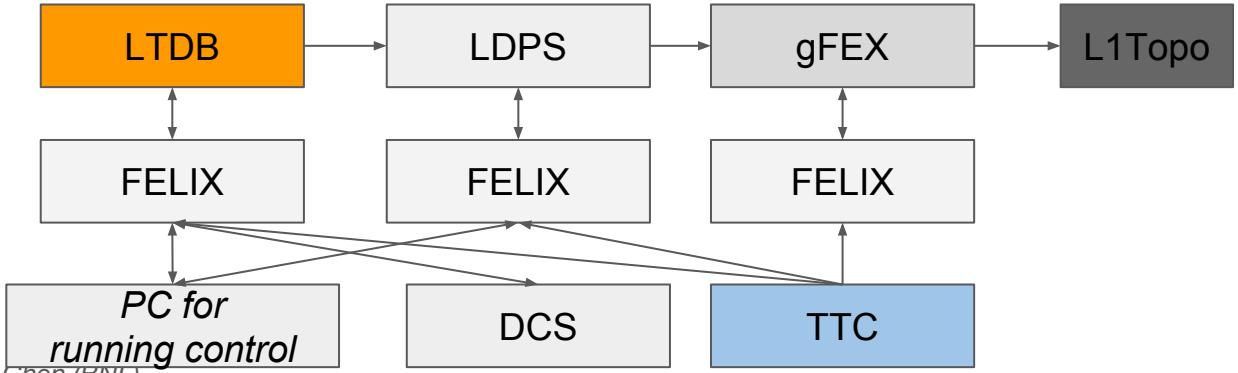




Summary and outlook

- LTDB is the kernel part in front-end of the ATLAS LAr Phase-I upgrade.
  - *High density, radiation tolerant, multiple high-speed links*
- Demonstrator board
  - *Installed in 2014*
  - *Successful data taking from 2015 to 2017*
- Pre-production board
  - *Installed in early 2018*
  - *Data taking is ongoing*
- Full chain integration will take place in this summer:





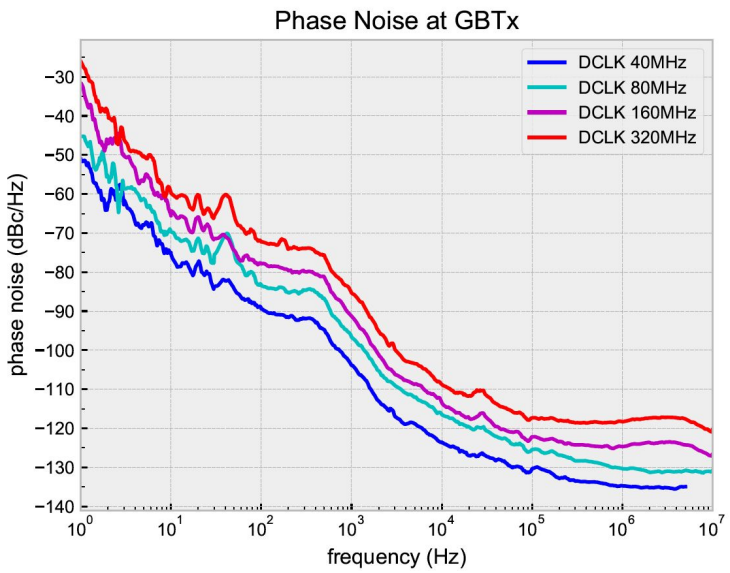
Thanks!

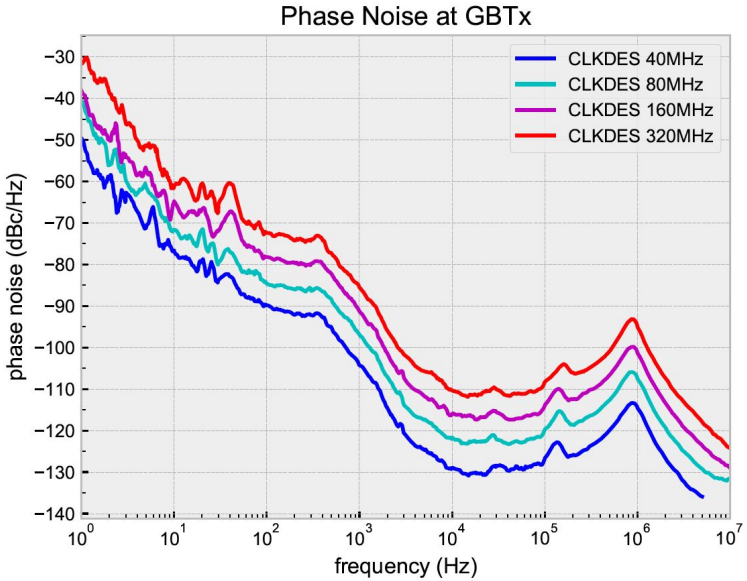
Job opening at BNL for Trigger & DAQ

https://jobs.bnl.gov/job/upton/postdoctoral-research-associate/3437/8059129

- This job post is for multiple openings.
- The successful candidate is expected to play an essential role in **FELIX** and **Global Trigger** development in the ATLAS upgrades and other *high-energy physics*, *nuclear physics* and *astronomy* experiments.
  - *Design, develop, prototype, and produce hardware and firmware for the ATLAS experiment*
  - *Evaluate hardware and firmware and characterize system performance*
  - *Participate in system integration of multiple combined systems*

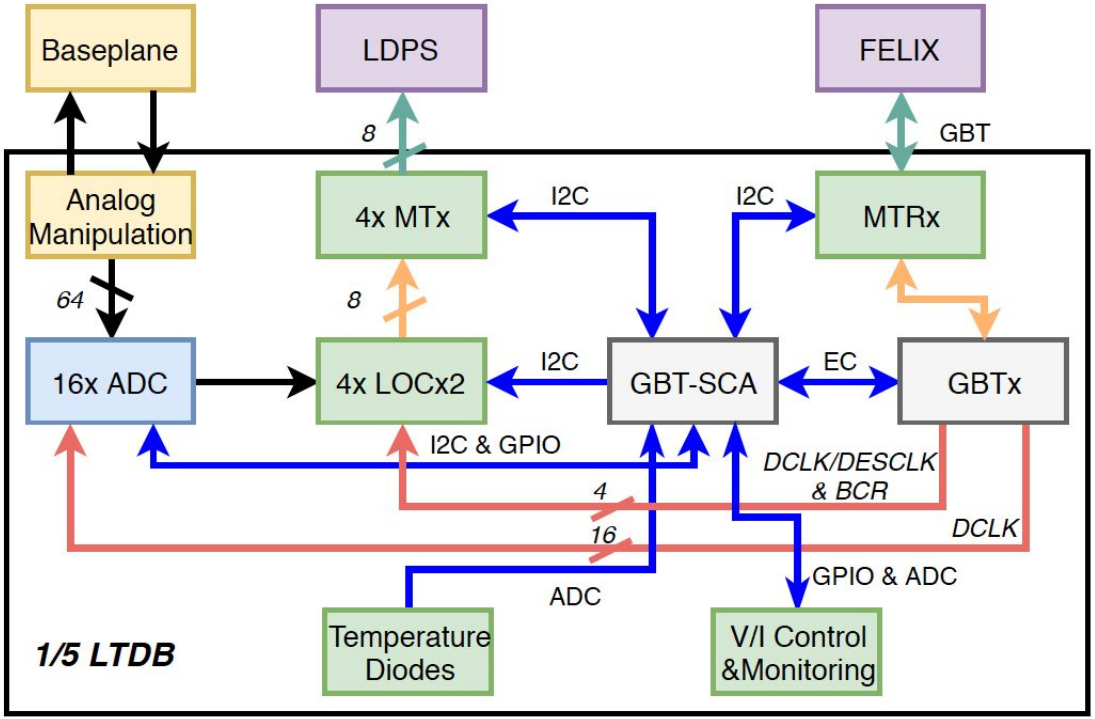
Phase noise for GBTx output clocks





- Jitter from 100 Hz to 5 MHz:
  - *4 ps for DCLK*
  - *10 ps for CLKDES*
- Both are good when used as reference clock for LOCx2 and FPGA GTX/GTH.

Diagram of the 1/5 prototype LTDB



The python API for GBTx/GBT-SCA control