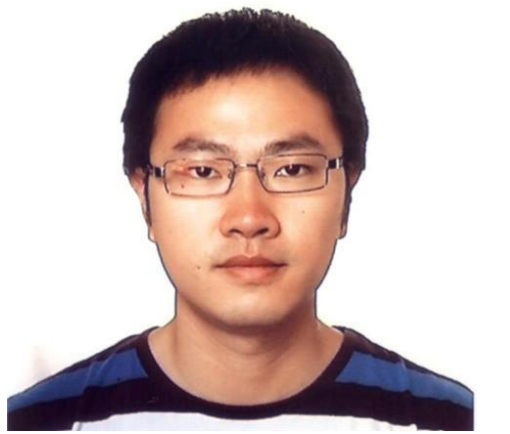




# Design of a common verification board for different back-end electronics options of the JUNO experiment

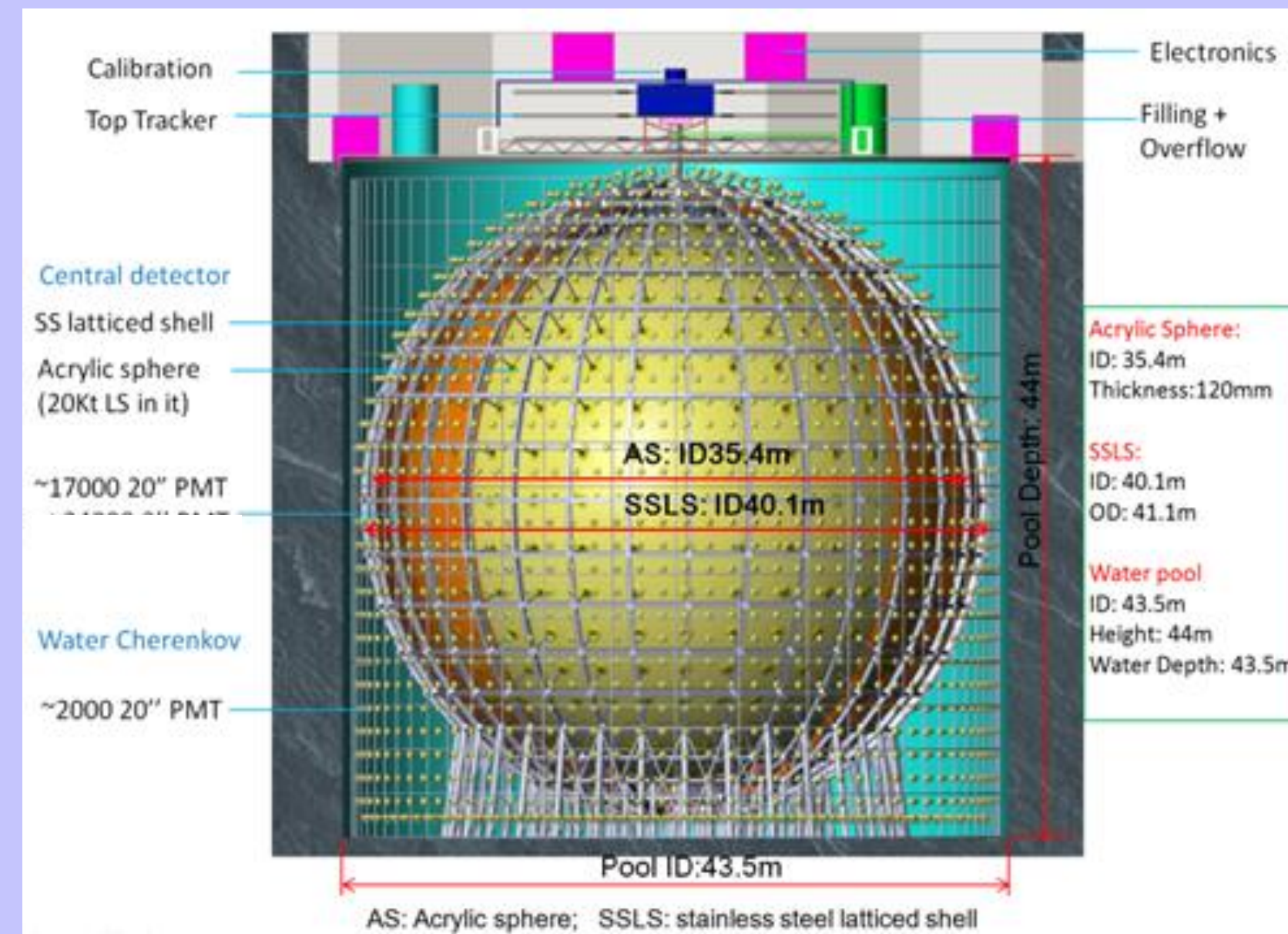


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On behalf of the JUNO collaboration  
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The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose neutrino experiment. It was proposed in 2008 for the measurement of the neutrino mass hierarchy by detecting reactor antineutrinos from nuclear power plants (NPP).

The site location is optimized to have the best sensitivity for the neutrino mass hierarchy determination, which is at 53 km from both the Yangjiang and Taishan NPP.



The neutrino detector consists of a large volume of liquid scintillator with a 20 kton fiducial mass, deployed in a laboratory 700 meters underground.

The JUNO readout electronics system will have to cope with signals of 17,000 photomultiplier tubes (PMT) of the central detector, as well as 2,000 PMT installed in the surrounding water pool to detect the Cherenkov light from muons. To avoid signal loss due to long distance transmission, most parts of the electronics system will be located in the water, close to the detector body.

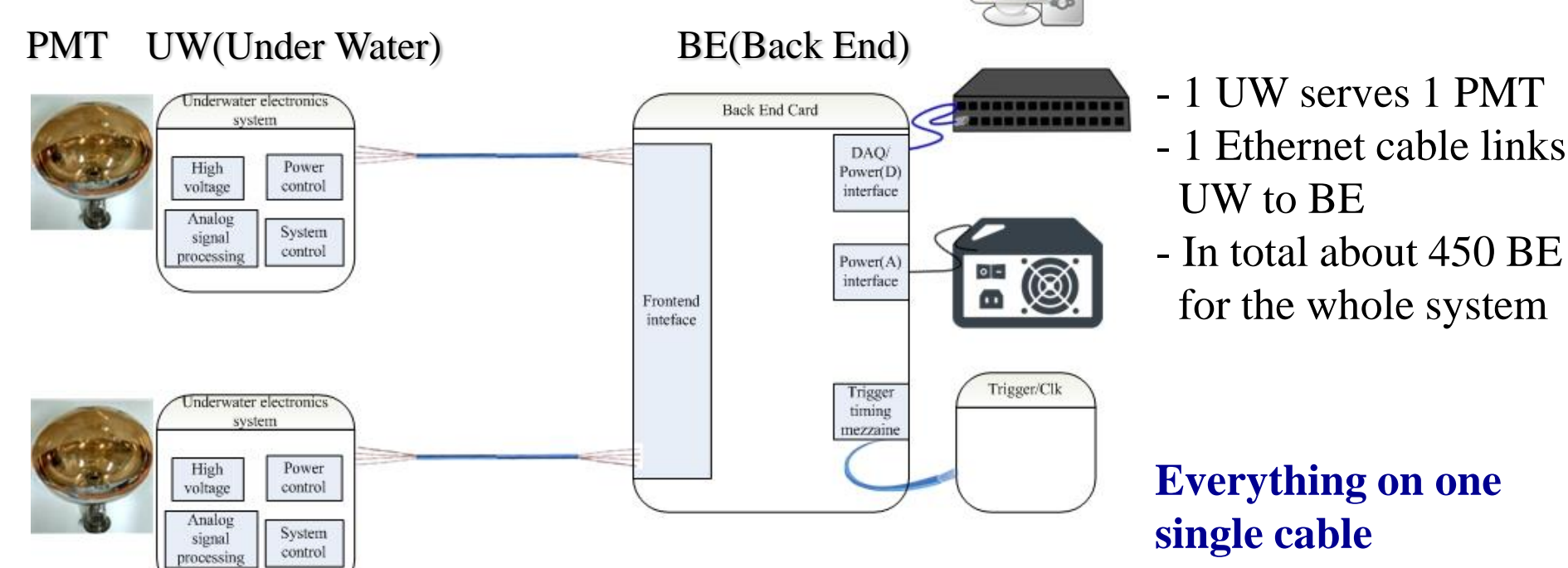
The JUNO electronics system can be separated into mainly two parts:

- the front-end electronics system performing analog signal processing (the underwater electronics), and after about 100 m cables,
- the back-end electronics system, sitting outside water, consisting of the DAQ and the trigger.

Data exchange between underwater electronics and backend electronics includes synchronized data (trigger and clock running at 250 Mbps and 62.5 MHz) and asynchronous data (100 Mbps Ethernet packet with event data and slow control command). Besides, power supply needs also to be delivered to underwater electronics from outside water.

Depending on the usage of transmission media (mainly Ethernet cables), some possible schemes linking the two parts are proposed. A common verification board, which is able to implement different types of tests, is important and critical for the choice of the best scheme and for the qualification of the full data chain.

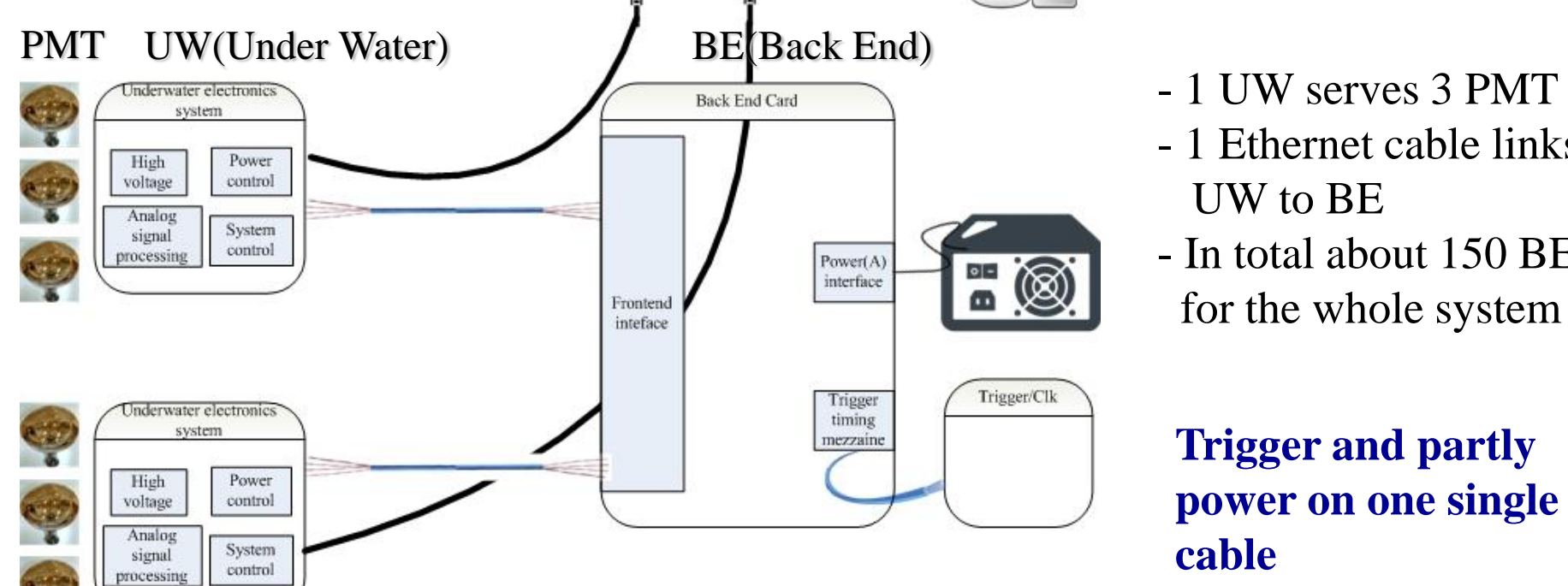
## BX scheme



- 1 UW serves 1 PMT
- 1 Ethernet cable links UW to BE
- In total about 450 BE for the whole system

Everything on one single cable

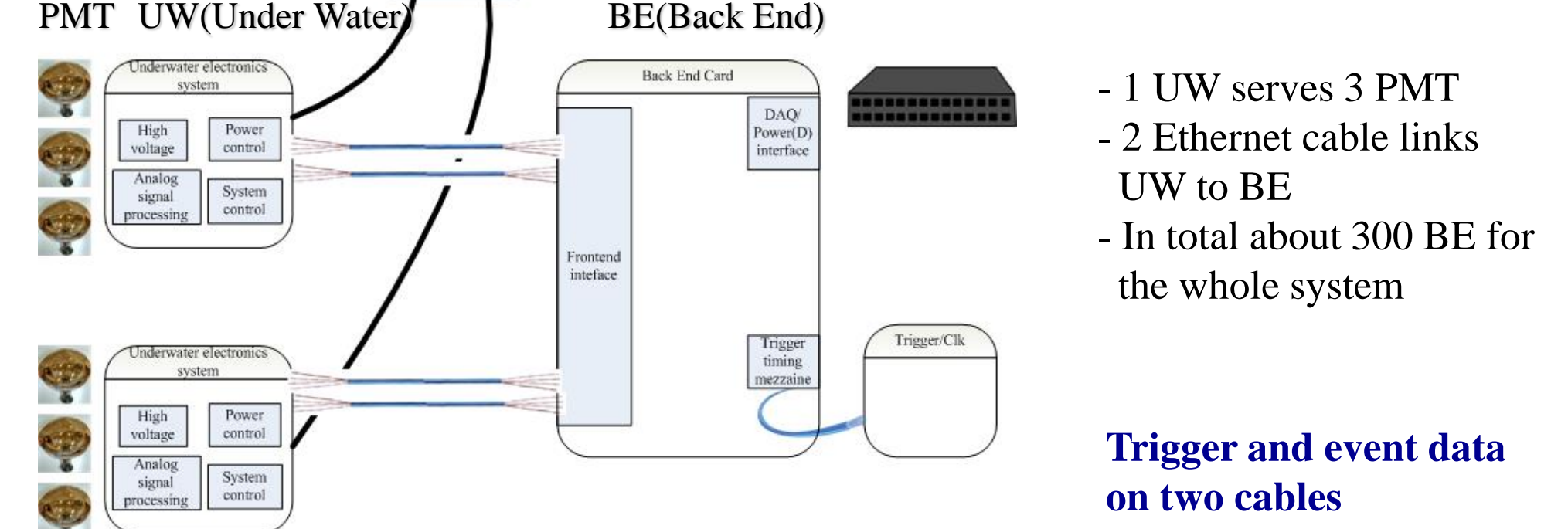
## 1F3 scheme



- 1 UW serves 3 PMT
- 1 Ethernet cable links UW to BE
- In total about 150 BE for the whole system

Trigger and partly power on one single cable

## RE1F3 scheme



- 1 UW serves 3 PMT
- 2 Ethernet cable links UW to BE
- In total about 300 BE for the whole system

Trigger and event data on two cables

One back-end (BE) card receives 48 Ethernet cables from underwater. The BE cards connect to trigger system through a FMC mezzanine card named TTIM, and can connect directly to DAQ and power supply, depending on the scheme.

Basic requirements for the links in one Ethernet cable:

- Link 1: trigger request from underwater to BE, 1 per PMT channel, running at 250 Mbps, needs equalizer to compensate for signal loss
- Link 2: trigger acknowledgement from back-end to underwater, derived from central trigger processor, same for all channels
- Link 3: event data and status monitor data, 100 Mbps Ethernet tx packet, linked directly to the DAQ system
- Link 4: control command, 100 Mbps Ethernet rx packet, linked directly to DAQ system

Power delivery : around 20 W (BX scheme) or 35 W(1F3 or RE1F3 schemes) in total from POE and/or direct connection

Pin definition of different schemes	BX	1F3	Partly redundant	Common solution
1,2	Trigger ack (250 Mbps with 15 W power)	Trigger ack (250 Mbps)	Trigger ack (250 Mbps)	Trigger ack (250 Mbps with 15 W power)
3,6	Trigger request (250 Mbps)	Trigger request (250 Mbps)	Trigger request (250 Mbps)	Trigger request (250 Mbps)
4,5	Ethernet tx (100 Mbps)	15 W Power +	Ethernet tx (100 Mbps)	Ethernet tx (100 Mbps) or 15 W Power +
7,8	Ethernet rx (100 Mbps)	15 W Power -	Ethernet rx (100 Mbps)	Ethernet rx (100 Mbps) or 15 W Power -

## Common verification board implementation:

- Use baseboard and mezzanine card structure; the baseboard has the full function of the 1F3 scheme
- Able to test critical data path without the need of real underwater electronics and real TTIM
- Using two 0 Ohm resistors on each signal path to minimize signal stub
- All differential pairs use impedance control even for power supply
- Each channel for power supply use 12 mils track on 1 oz copper for 1A current with separate resettable fuse protection, 8 channels share one power module
- Power supply for underwater electronics is separated from the power supply for back-end card, for different grounding possibilities
- Making library of mezzanine card and integrate into baseboard design
- Implementing individual trigger request and acknowledge connection to two FMC connectors for maximum flexibility

Stackup Information:

Layer	Info	Thickness
TOP		0.333(Plating)
L1	PP TU-75P 1080x1080	5.086(mil)
L2	Core TU-752 0.13	1.02
L3	PP TU-75P 1080x2110	5.118(mil)
L4	Core TU-752 0.21	1.02
L5	PP TU-75P 1080x2110	8.268(mil)
L6	Core TU-752 0.13	1.02
L7	PP TU-75P 1080x2110	5.118(mil)
L8	Core TU-752 0.13	5.074(mil)
L9	PP TU-75P 1080x2110	1.02
L10	Core TU-752 0.13	0.333(Plating)

设计板厚	(2.992-0.299-4.299) mil	1.6(-0.16-0.16) MM
设计板厚	80.327 mil	1.645 MM
材料板厚	TU-752	TU-752

Impedance Information:

层号	材料	厚度	介电常数	阻抗公差	设计值	阻抗公差	设计值	阻抗公差	设计值	阻抗公差	设计值	阻抗公差
L1	L2	PP	PP	100±10%	5.08	100±10%	5.08	100±10%	5.08	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
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L1	L2	PP	PP	100±10%	5.08	99.13	100±10%	5.08	99.13	100±10%	5.08	100±10%
L1	L2	PP	PP	100±								