A 5.5 ps Time-interval RMS Precision Time-to-Digital Convertor Implemented in Intel Arria 10 FPGA

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CONTENT

1. INTRODUCTION

2. TDC IMPLEMENTATION

3. TEST RESULTS

4. CONCLUSION

INTRODUCTION

Time-to-digital converters(TDC):

1. Applications:
   - High energy physics experiments
   - Atomic physics experiments
   - Time-of-flight PET
   - Laser rangefinder et al.

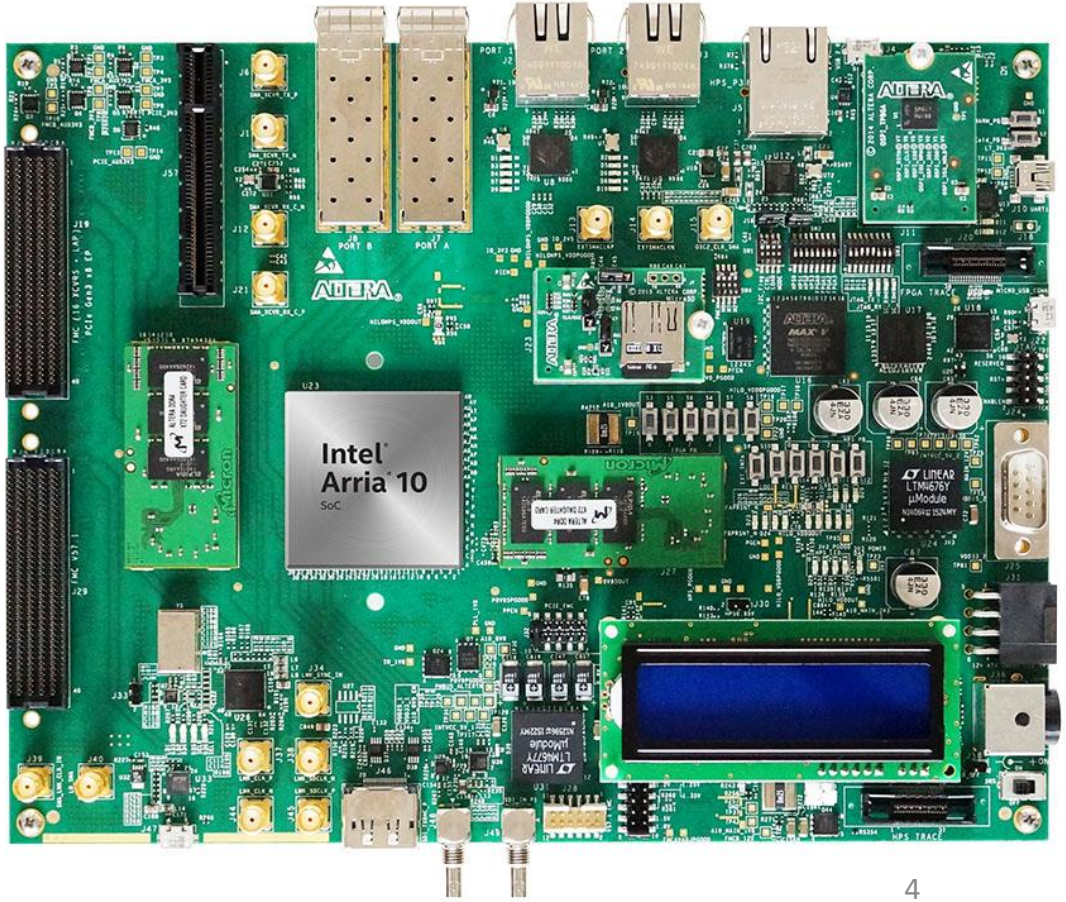
2. Requirement
   - High measurement throughput
   - High time precision
   - Multi-channel

INTRODUCTION

The Intel Arria 10 SoC Development Kit:

- 10AS066N3F40E2SG
- TSMC's 20nm
- Dual-core ARM
- 660K Logic Elements
- 251680 ALM
- 42620 M20K
- 5788 MLAB
- 1687 DSP Block

(from Intel Arria 10 Device Overview)



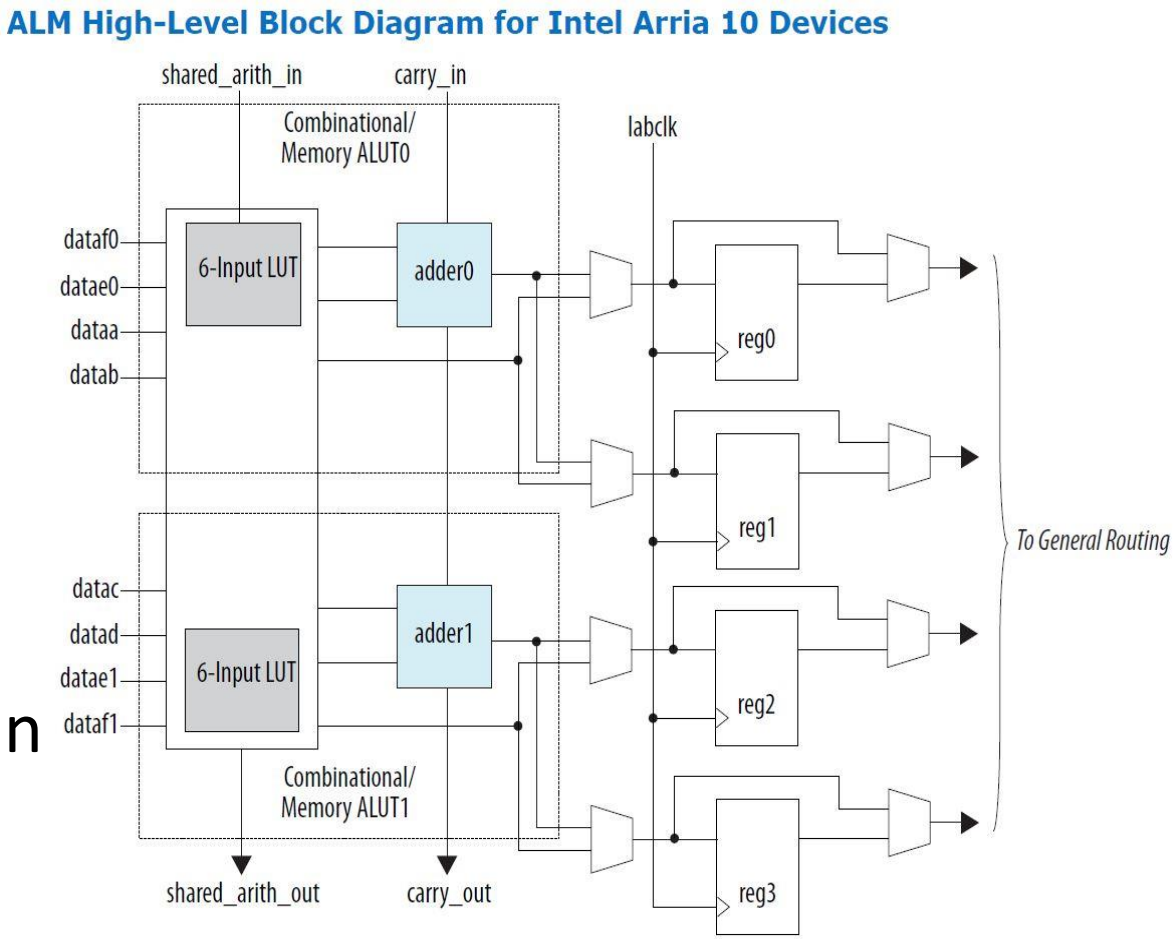
TDC IMPLEMENTATION

ALM

- Two Adaptive LUTs
- Four Registers
- Two Full Adders

LAB(MLAB)

- Ten ALMs
- Dedicated Carry chain

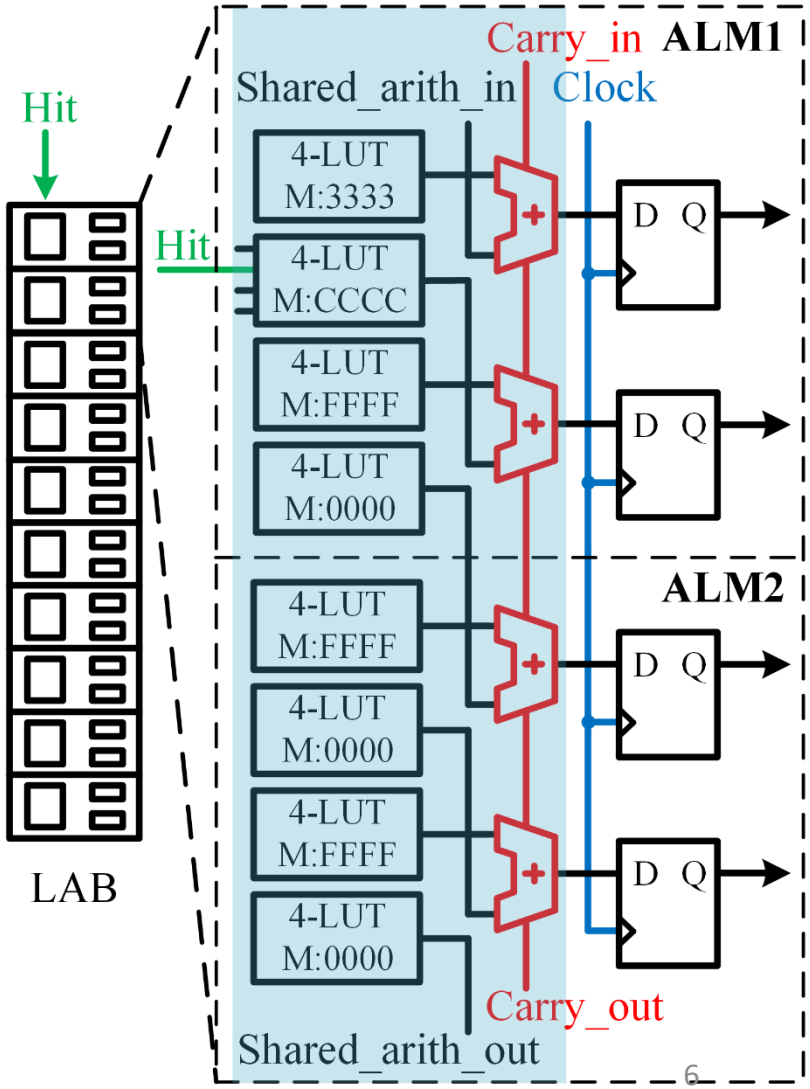


(from Intel Arria 10 Core Fabric and General Purpose I/Os Handbook)

TDC IMPLEMENTATION

TDC Core:

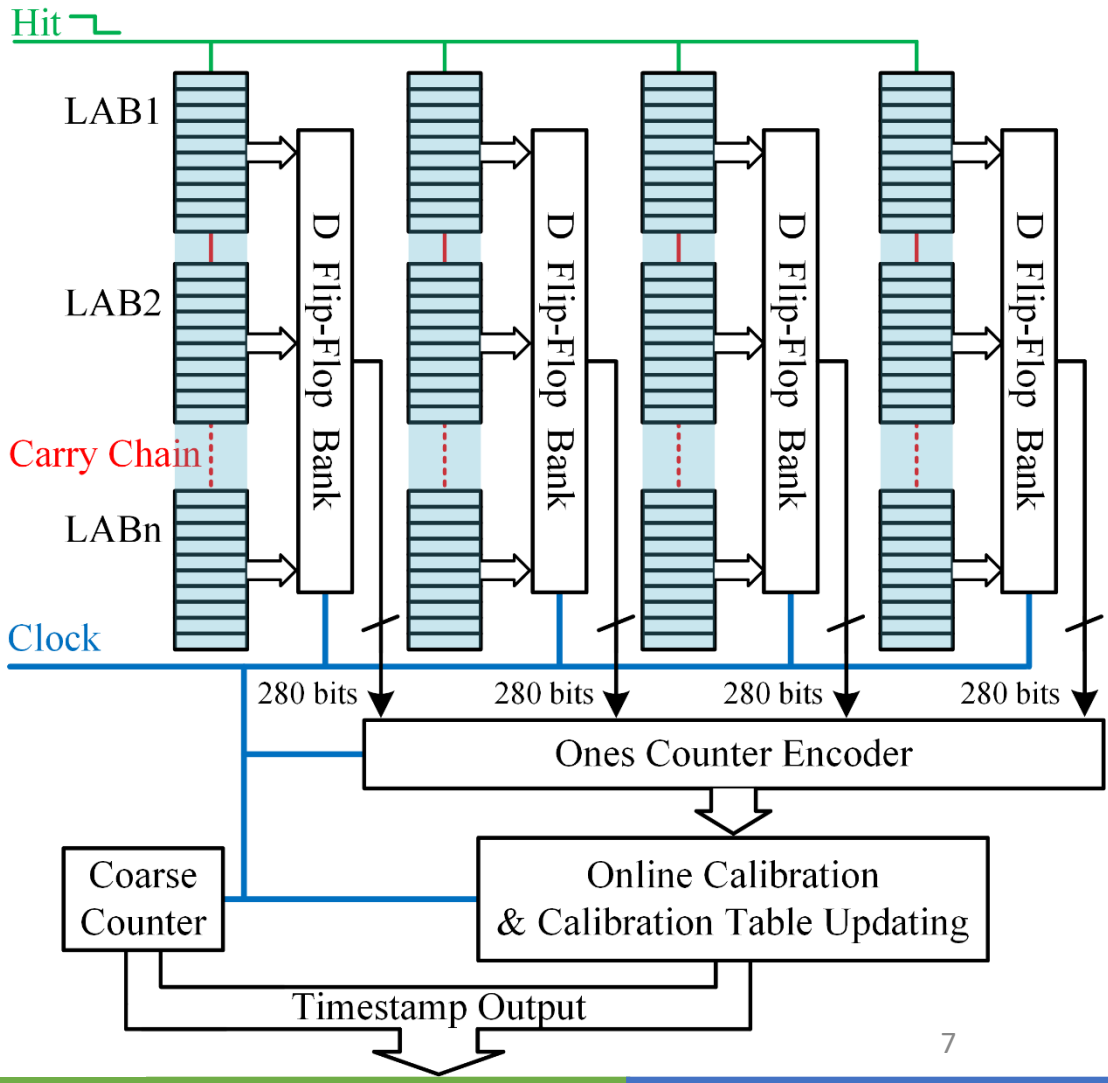
- $N'hFFFFF \ldots + 1'bHit$
- The TDL status will be latched out by registers with a hit signal propagating along the TDL
- Clock rate: 500MHz



TDC IMPLEMENTATION

TDC Structure:

- Coarse Counter
- TDC Core
- Ones Counter Encoder
- Online Calibration
- FIFO & Data Readout



TDC IMPLEMENTATION

TDC Encoder:

$$Thermometer\ Code \Rightarrow Binary\ Code$$

$$111111000000000 \Rightarrow 4'b0110$$

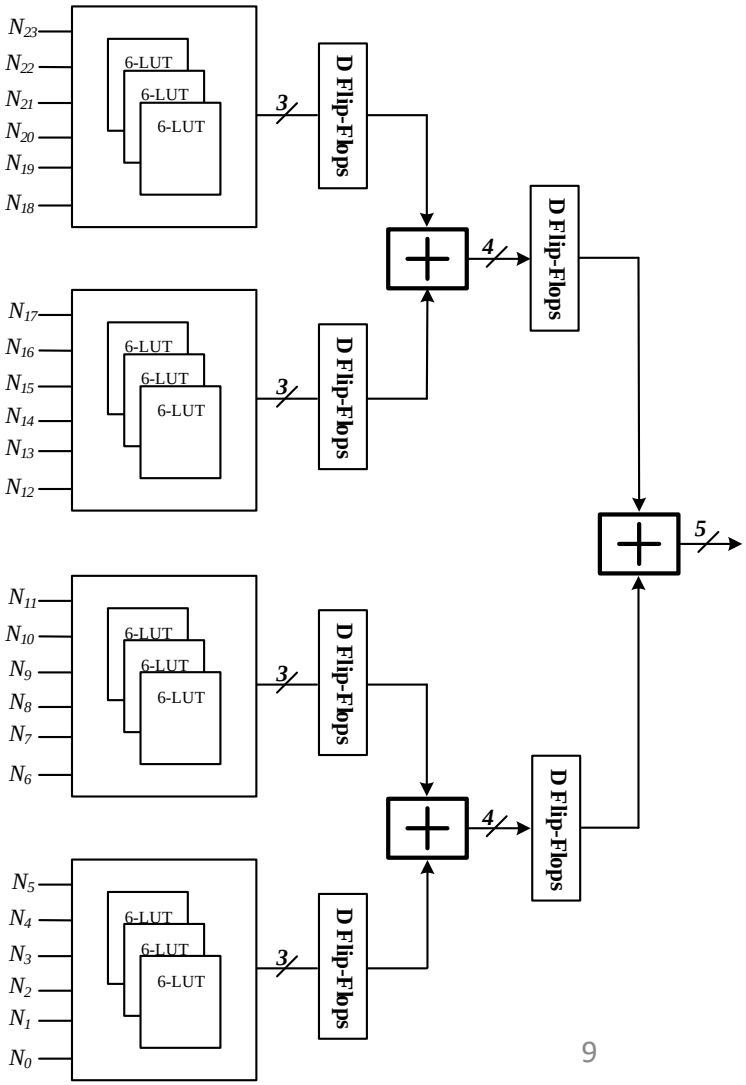
$$111100101100000 \Rightarrow 4'b????$$

TDC IMPLEMENTATION

Ones Counter Encoder:

$$Thermometer\ Code \Rightarrow Binary\ Code$$

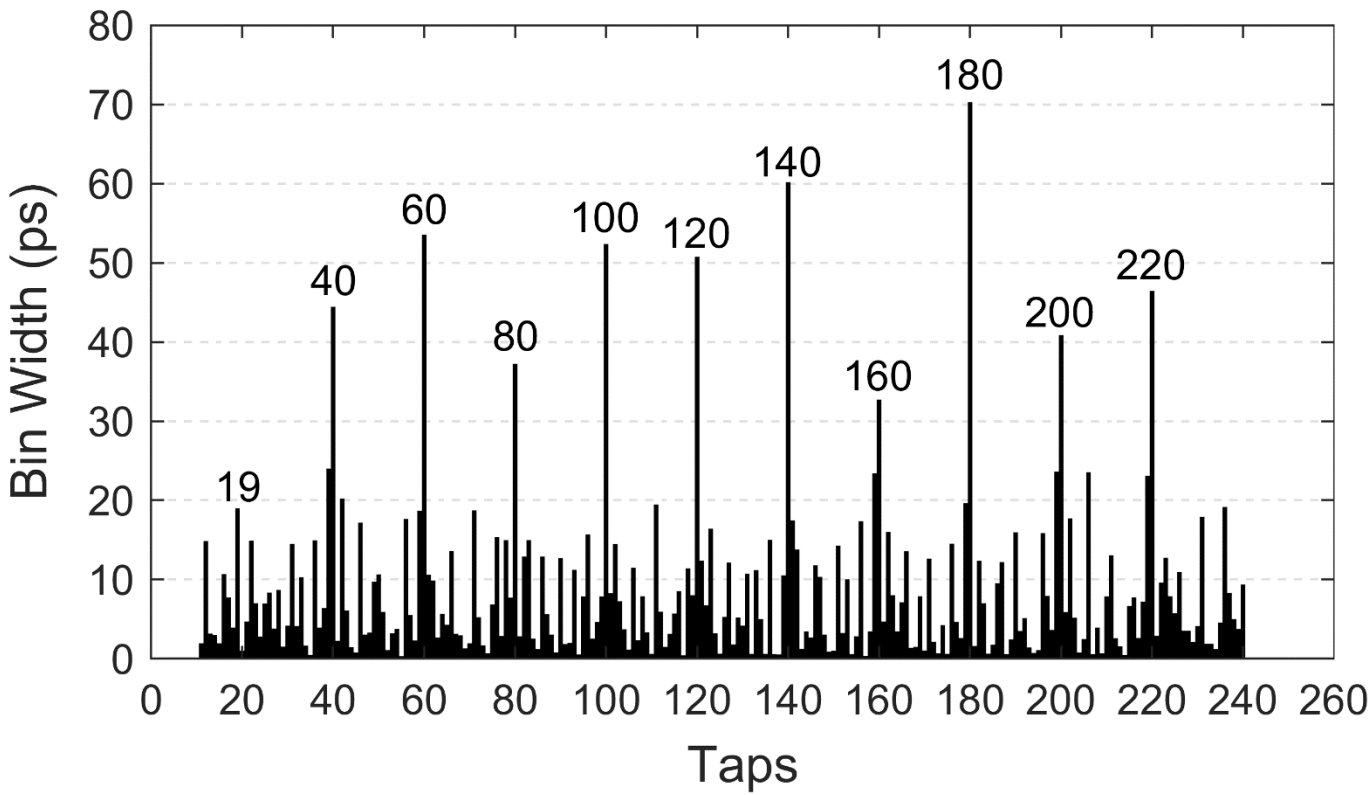
$$111100101100000$$
$$\Downarrow$$
$$111100\ \&\ 101100\ \&\ 000$$
$$\Downarrow$$
$$3'b100 + 3'b011 + 3'b000$$
$$\Downarrow$$
$$4'b0111$$



(Yonggang Wang, Jie Kuang, Chong Liu, Qiang Cao. "A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA." *IEEE Transactions on Nuclear Science* 64.10 (2017): 2713-2718.)

TEST RESULTS

A. Single-TDL TDC test



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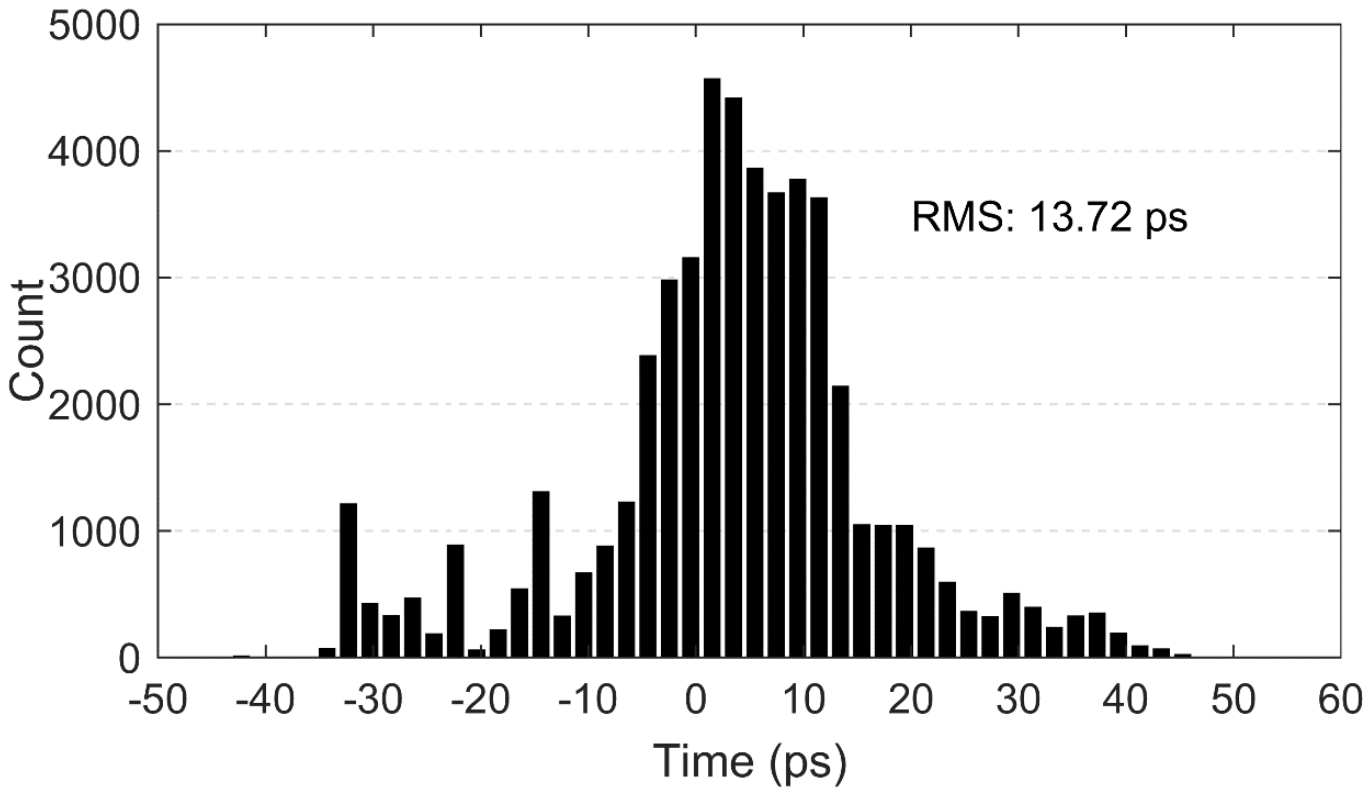
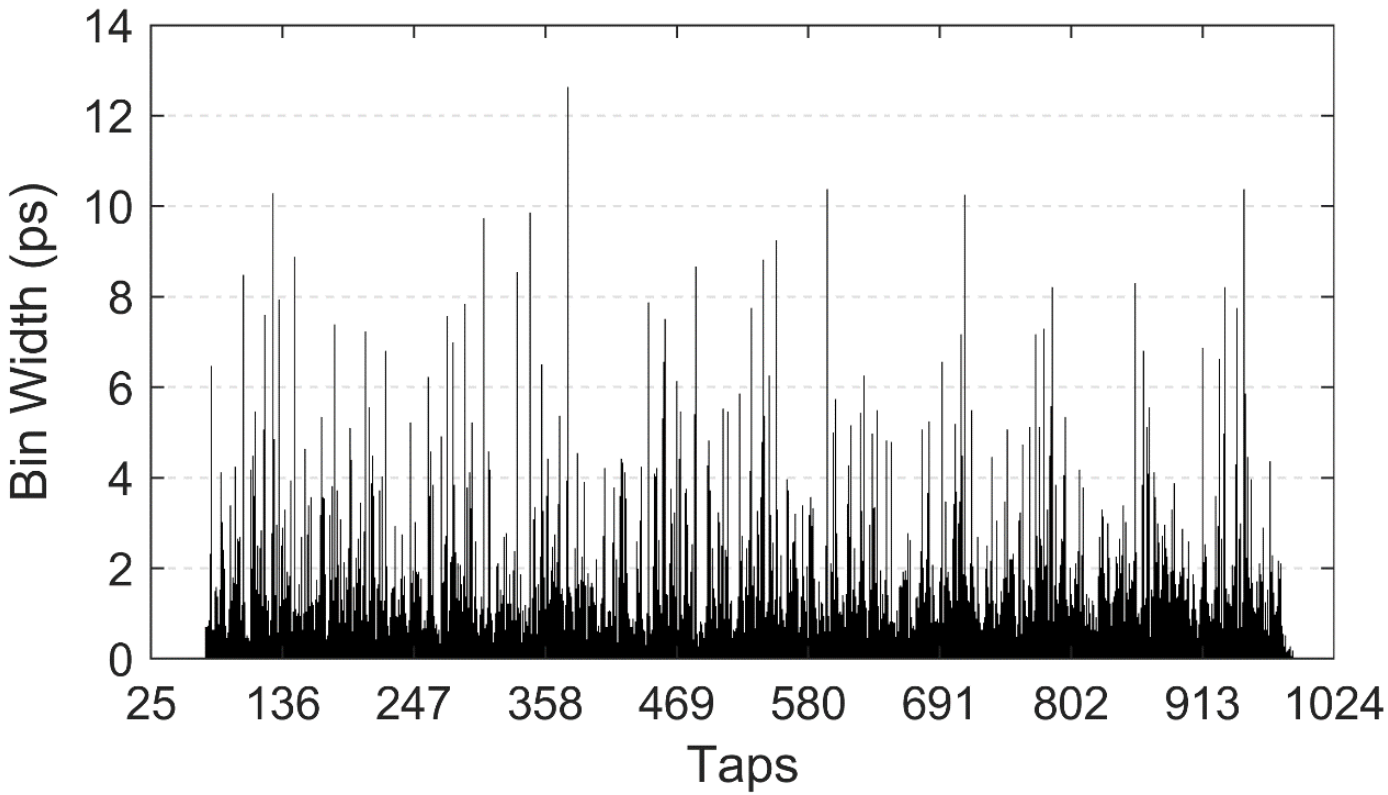


TEST RESULTS

B. Multi-TDL TDC test



Effective bins: 921

TEST RESULTS

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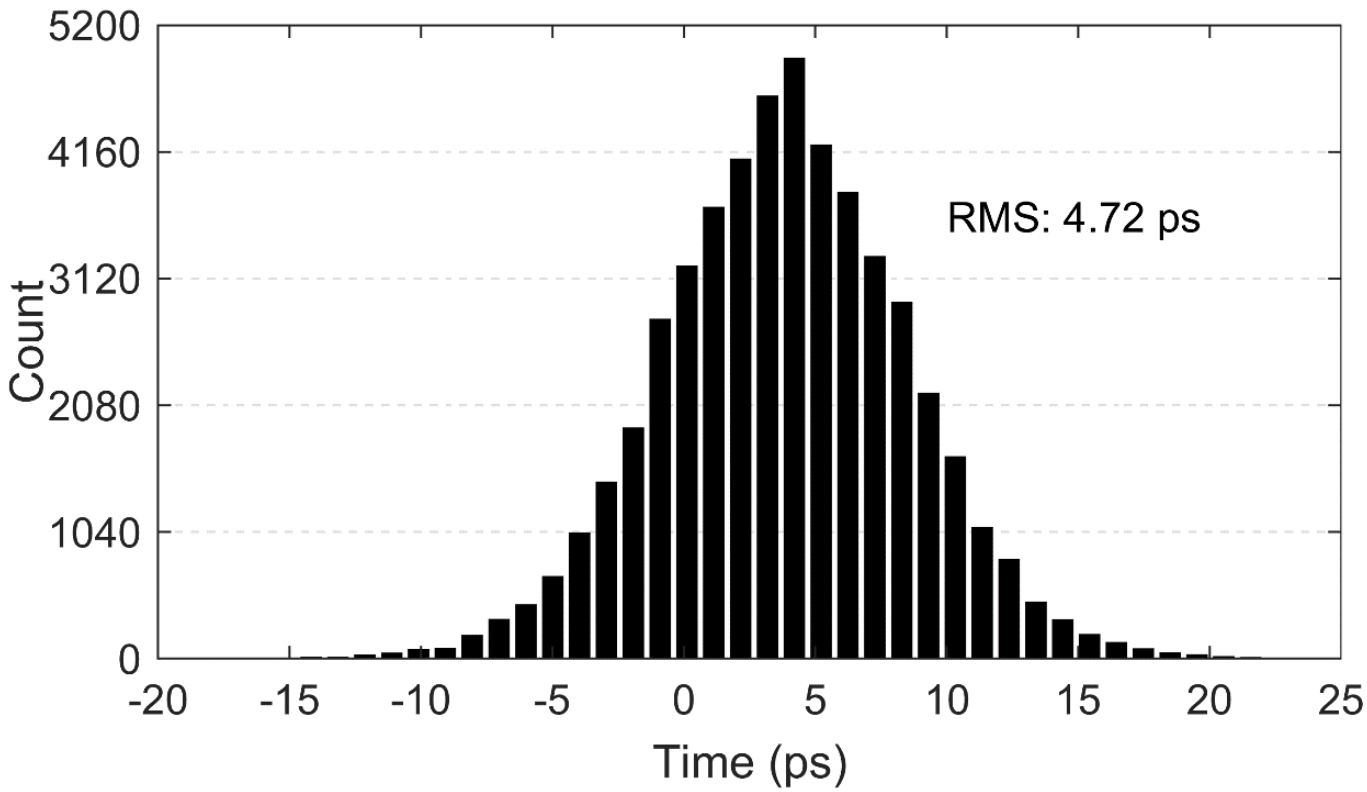

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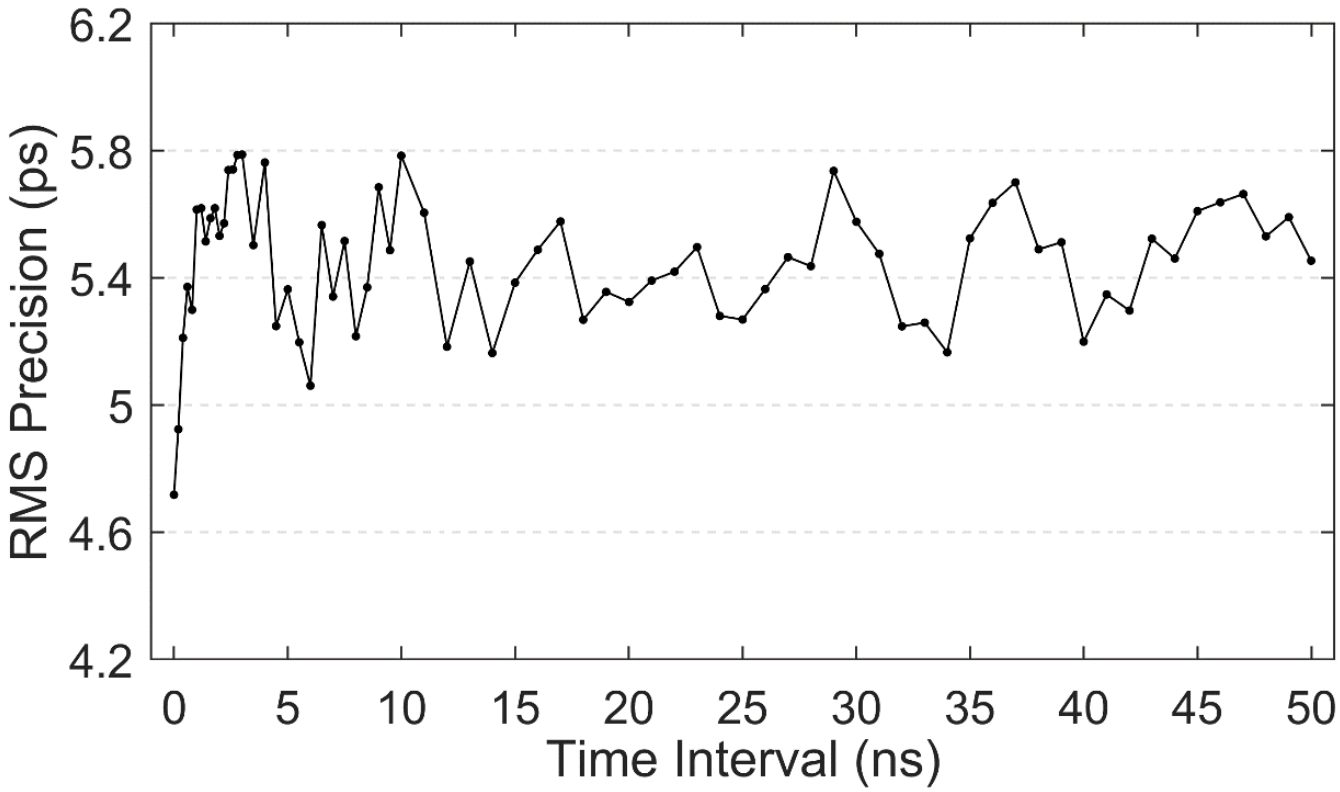

Average precision = 5.5 ps

CONCLUSION

- A practical 5.5 ps time-interval RMS precision TDC with 250 M throughput is achieved in Intel Arria 10 FPGA using the structure of four TDLs parallel.

- The measured result of TDL property is highly consistent with its underlying structure features.

- Compared to TDC in Xilinx FPGA, the structure features indicate Intel FPGA has slightly poor ability for achieving TDC.

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THANKS