Development of a multichannel FPGA based high resolution Time-to-Digital Converter

Tomonori Takahashi

Research Center for Nuclear Physics (RCNP), Osaka University

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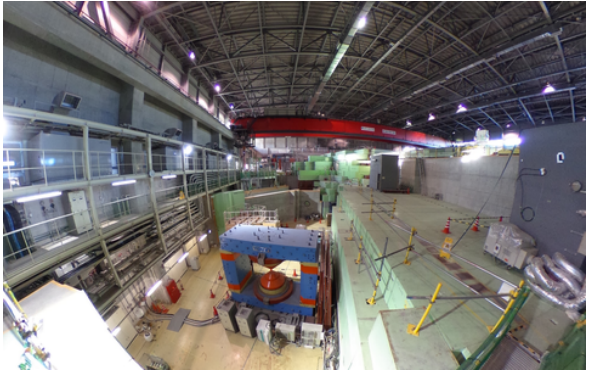
Outline

- Modivation
- Hardware overview
- Fimrware implementation
- Performance measurement
- Summary



High momentum beam line
at J-PARC Hadron Experimental Facility

Motivation

Demand for low cost and high resolution TDC (HR-TDC) for TOF and an event pileup rejection

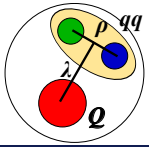
- Hadron physics, nuclear physics at J-PARC and SPring-8 LEPS2
  - Restoration of chiral symmetry breaking at ρ_0
  - Diquark as effective degrees of freedom in QCD
  - Extotic hadrons, multiquark systems
- Readout for plastic scintillator, Čerenkov counter, MRPC

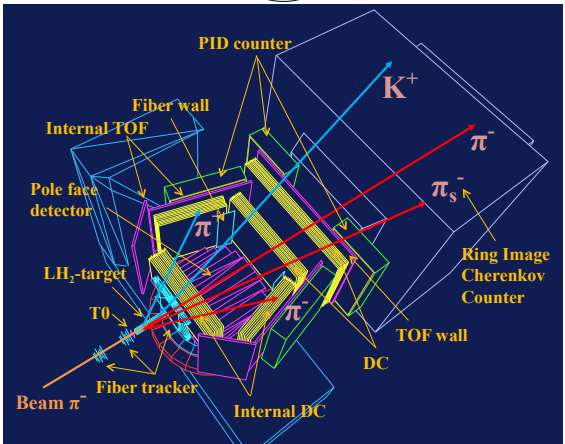
J-PARC E50 experiment

- Investigate the diquark correlation via a charmed baryon spectroscopy
- Large acceptance multi-purpose spectrometer
- π^- beam: 60–180 M/spill (30–90 MHz), 20 GeV/c
- Start from 202X
- Streaming DAQ, > 20k ch
- 0.5–1k ch HR-TDC

Requirement for HR-TDC:

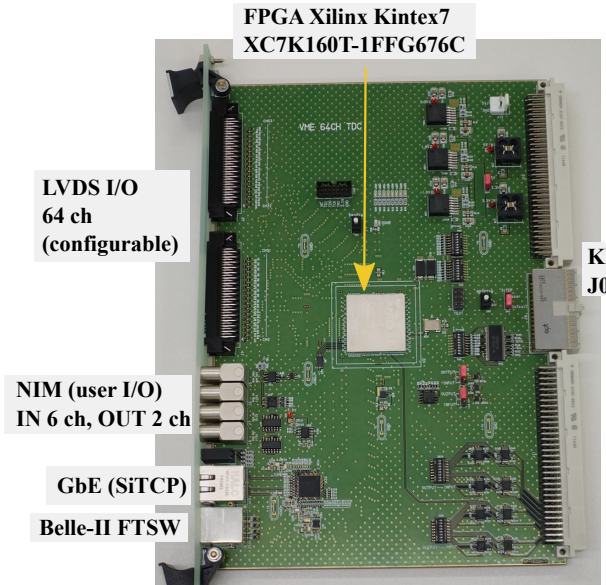
- Time resolution < 30 psec (σ)
- dead time < 3.3 nsec
  99% Hit detection efficiency
  @ 3 MHz/ch





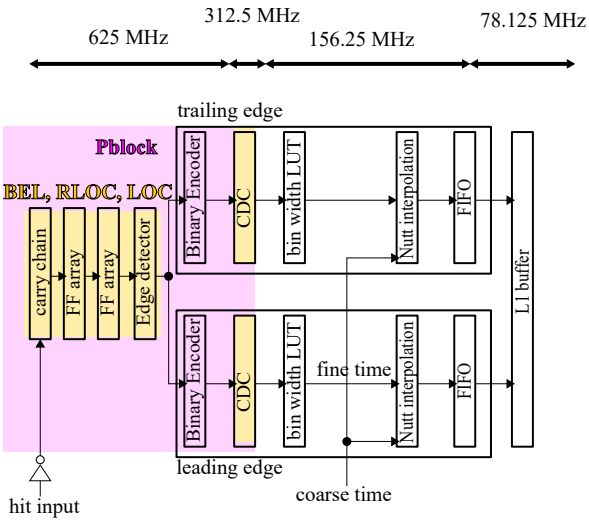
Hardware for HR-TDC demonstration

- VME 6U
- **FPGA : Kintex-7 XC7K160T-1FFG676C a few 100s USD**
- Orignal application: FPGA TDC w/ LSB=1 nsec for drift chamber readout



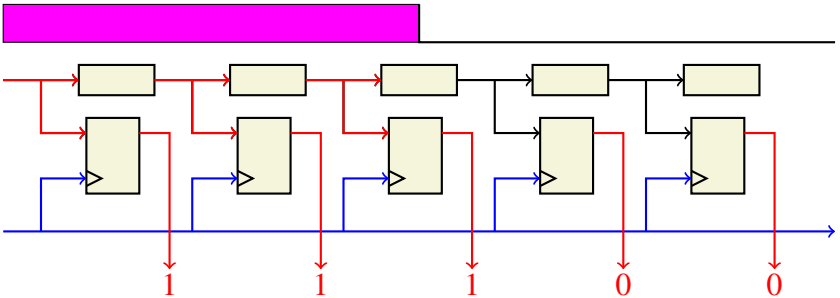
FPGA TDC

- Tuned delay line : 160 bins
  @ 625 MHz clock (1.6 ns/cycle)
- Edge detector (Thermometer code to 1 hot)
  - leading edge
  - trailing edge
- Binary Encoder
  - OR-based
  - Bin ID 8 bit, hit detect
- CDC (clock domain crossing)
  - 625 MHz → 312.5 MHz
  - 312.5 MHz → 156.25 MHz w/ FIFO
- Bin width look-up-table in FPGA
  - fine time 8 bit
    LSB = 1.6 ns/256 = 6.25 ps



TDC 1 channel

Tapped delay line

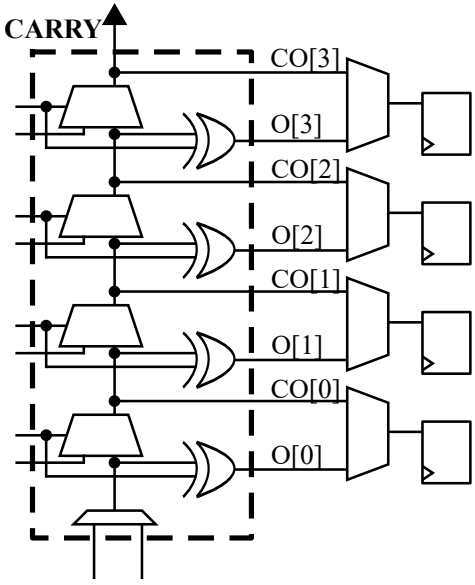


- Carry chain and D-FF array in FPGA
- Ideal: Thermometer code output
- Realistic: Bubbles appear in the thermometer code.
- Many zero-width bins in a conventional tapped delay line TDC for recent FPGAs

Tapped delay line→ Tuned delay line

Heterogeneous sampling
(J. Y. Won and J. S. Lee, IEEE TIM Vol.65, No.7, 1678 (2016))

- Optimal combination of outputs from:
  - **O (inverted by XOR)**
  - **CO (non-inverted)**
- Won and Lee: Output from Os and COs are encoded individually, then, merged.
- This work: **Edge detector for the heterogenous sampling** (shown later)



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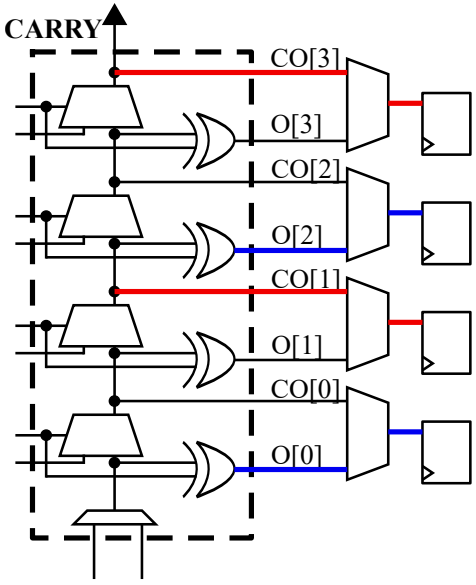
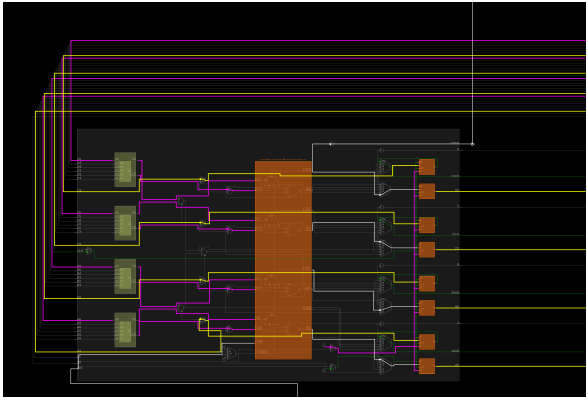


Double FF synchronizer

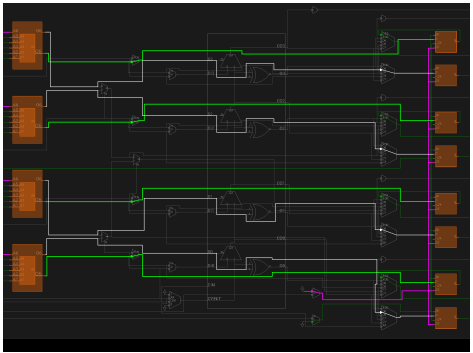
- Metastability with 1 FF array @ 625 MHz sampling
- Double FF arrays in the same SLICE
  - reduce resource usage
  - shorter path
- SLICE LUTs: explicitly instantiated to fix paths to S and DI of CARRY4
  - avoid a routing conflict with the syncronizer



Edge detector for thermometer code

Find a 1→0 (0→1) transition in a thermometer code of the heterogeneous sampling

- 6-input 2-output LUT
  → 5-input LUTs ×2
- INIT attributes of the LUTs (truth table):
  - O5 : leading edge
  - O6 : trailing edge



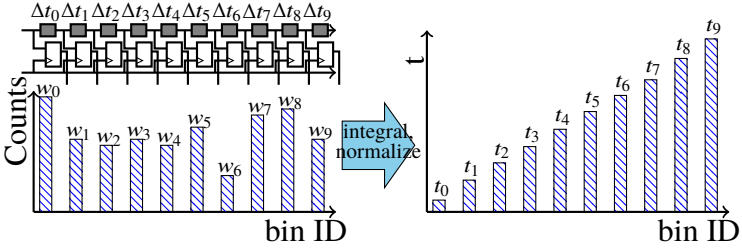
	homogenous all CO	heterogeneous O-CO-O-CO-O	CO-O-CO-O-CO
I0 I1 I2 I3 I4	01111	11010	00101
	11110	01011	10100

Bin width calibration

Code density test: $\Delta t_i \propto w_i$

- Block RAM
  - Histogram
  - Look-up-table

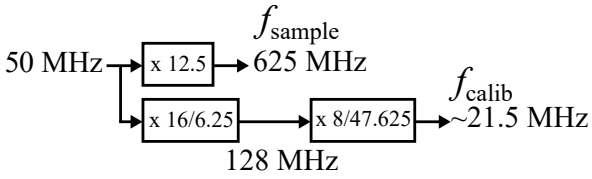
$$t_n \propto \frac{w_n}{2} + \sum_{k=0}^{n-1} w_k$$



- Calibration pulse from FPGA internal clock generator

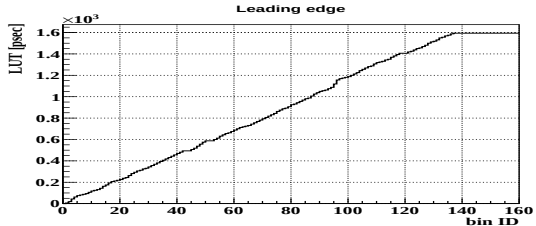
  (J. Wu, DOI:10.1109/RTC.2014.7097534)

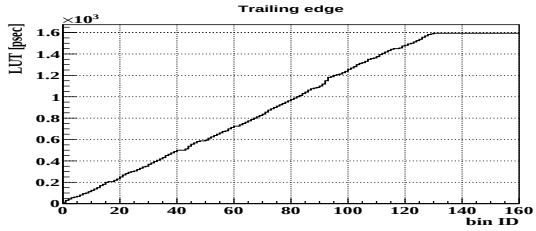
  - $f_{\text{sample}}/f_{\text{calib}} = (3 \cdot 5^4 \cdot 127)/2^{14}$



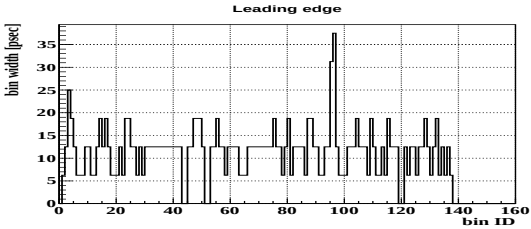
Bin width calibration (2)

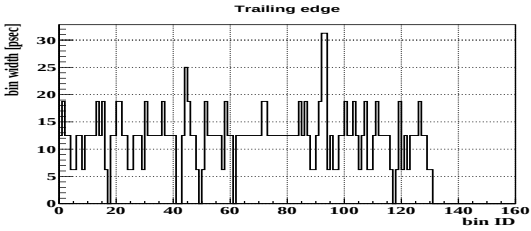
LUT





DNL

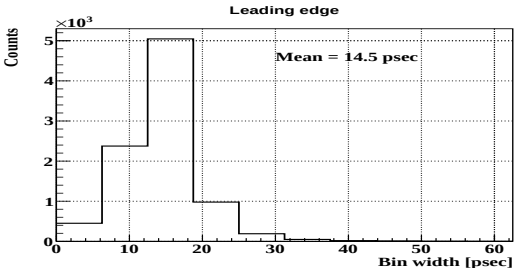


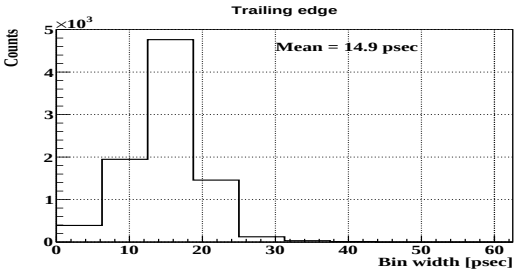


Ultra wide bin due to the FPGA structure : horizontal clock row (HROW) at the middle of each clock region

Bin width calibration (3)

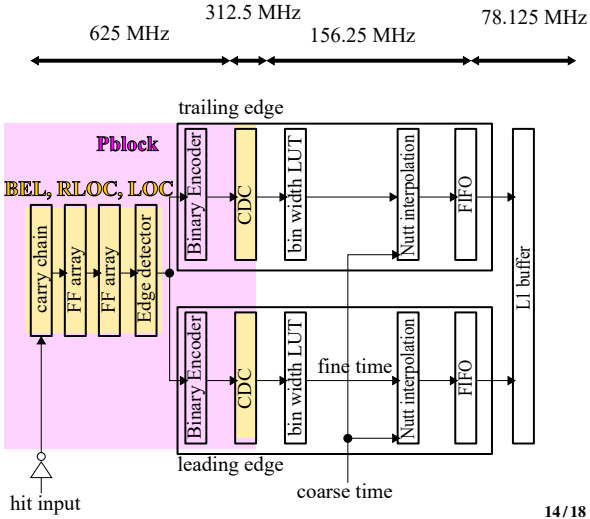
	leading edge	trailing edge
Mean	14.5 ps	14.9 ps
Max	50 ps	37.5 ps
Zero-width bins	4.9%	4.5%





Place and Route (PAR) constraint

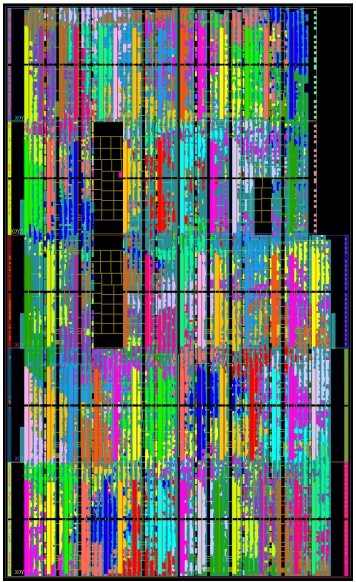
- RLOC, BEL (in VHDL code):
  - Tuned delay line
  - Edge detector (thermometer to one hot)
- LOC (in xdc):
  - Origin of RLOC for the delay line and the edge detector
  - BRAM in CDC
- Pblock:
  - 50×8-50×10 SLICEs per channel: components running at ≥312.5 MHz
  - Each clock region: duplication of coarse counter and reset.



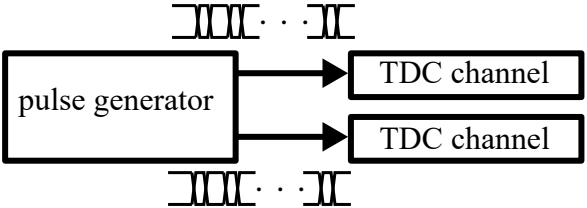
Resource usage

	All	TDC 1 ch
LUT	70%	1.2%
LUTRAM	2.4%	0.34%
FF	63%	0.92%
BRAM	89%	1.2%

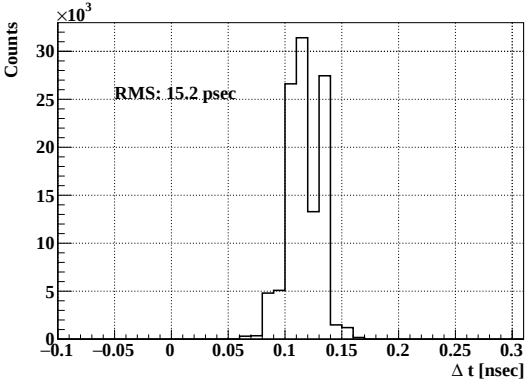
All = TDC 64+1 ch, trigger controller, SiTCP, etc.
Most of FIFOs are configured as built-in FIFO to save the resource.



Performance measurement



measurement setup



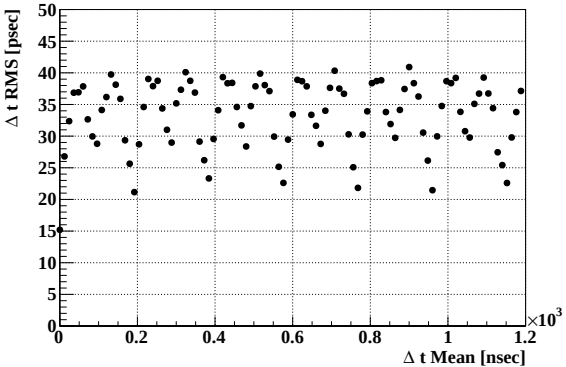
Inject 100 consective pulses

- 8 nsec width
- 12 nsec interval

RMS = 15.2 psec for Δt ~0 nsec

Performance measurement (2)

- Good resolution for $\Delta t \leq 1$ nsec
- However, 20 – 41 psec for $\Delta t > 1$ nsec
- DC-DC switching power supply on the board? (not clear)



Summary

- FPGA : Xilinx Kintex-7 XC7K160T-1
- 64+1 channels
  - leading-edge and trailing-edge measurement
- Tuned delay line with 160 bins
  - Heterogeneous sampling and edge finding
- Built-in bin width calibration
  - Bin width (Avg.): 14.5–14.9 ps
- Dead time: 2 cycles @ 625 MHz (= 3.2 nsec)
- Time resolution (σ) : 15–41 ps resolution
  - On-board DC-DC power supply might cause resolution worse.