A programmable clock generator for automatic Quality Assurance of LOCx2

Zhi-yue Wang, Tian-kuan Liu, Qi-jie Tang, Yi Feng, Jian Wang*

State Key Laboratory of Technologies of Particle Detection and Electronics, Modern Physics Department, University of Science and Technology of China

*Email: wangjian@ustc.edu.cn, IEEE Senior Member

1.Introduction

The upgrade of ATLAS Liquid Argon Calorimeter (LAr) made a demand of a high-speed, low-latency data transmission to read out from the LAr Trigger Digtizer Board(LTDB). The readout signal goes into the LTDB which split the signal into four ways of ADCs and the data yield by ADCs was caught by LOCx2, which was an ASIC designed to meet the requirement of high-speed and low-latency data transmission. About 7000 LOCx2 were fabricated, therefore a automatically Quality Assurance need to be done in order to pick out those dies with better performance.

Fig.1 shows the Block diagram of LOCx2 BER, I2C, and input skew test setup. All 7000 LOCx2 chips will get through the test of BER and I2C. About 1% of the chips that pass the eye diagram tests and BER tests in each wafer will be sampled to measure the 3.125-ns input skew tolerance in the ASIC ADC mode. Si5338 play the role of generating an any-frequency clock signal for test. A host PC will control and supervise the whole test system automatically. Therefore, we develop a set of firmware and corresponding host program to control the Si5338 signal generator.

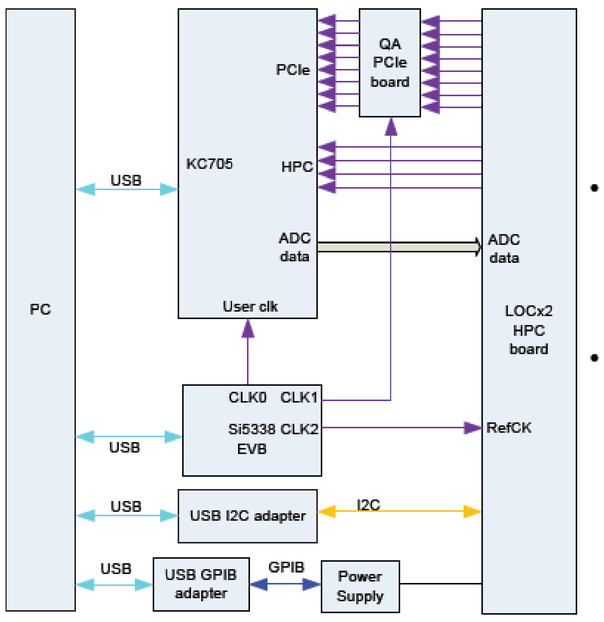

Fig.1. Block Diagram of the Test System

2.Structure of Entire System

Fig.2 shows that Si5338 is a programmable, any-frequency, four channels clock signal generator, whose output signals can be configured by its registers, and this is the kernel for generating the clock signals. C8051F340 is a MCU based on CIP-51 core which maintains the function of the hardware SMBus I/O, and an USB-controller, which is used to communicate with SI5338 through I2C bus to configure the output of clock signal and the voltage of power supply modules for Si5338. AD5263 is a programmable variable resistor and MAX8869 is a voltage regulator. In order to meet the power supply for five different VDD pins on the Si5338, five channels of power supply module which consist of an AD5263 and a MAX8869 were needed. AD5263 is controlled by MCU through I2C bus as well. All these components were on the Si5338 EVB board and make up the programmable clock generator.

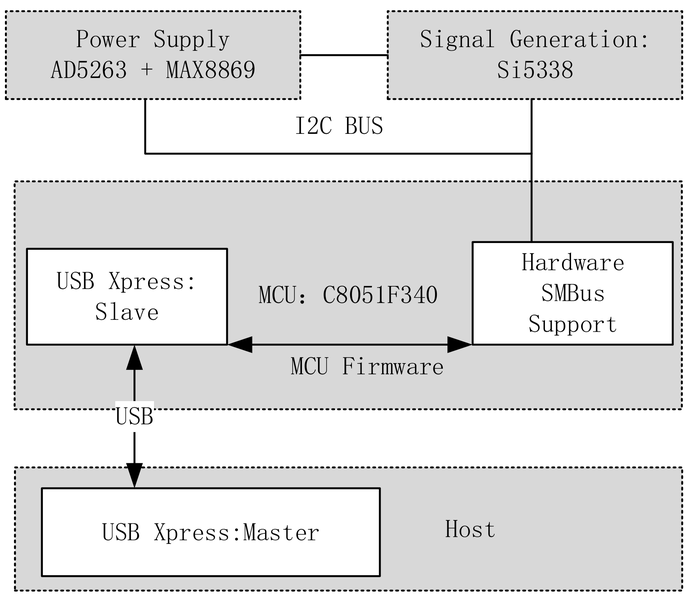

Fig.2. Block Diagram of Si53338 EVB with host computer

Concerning the Si5338 EVB has a USB interface, and C8051F340 MCU has a USB controller built-in, The USB interface was choosen to send to and receive commands from MCU. A set of solution called USBXpress which could drive the USB interface in both host and device was adopted. Base on this software, we developed the host program as well as device firmware which communicate with each other through USB interface.

3.Design of Device Firmware

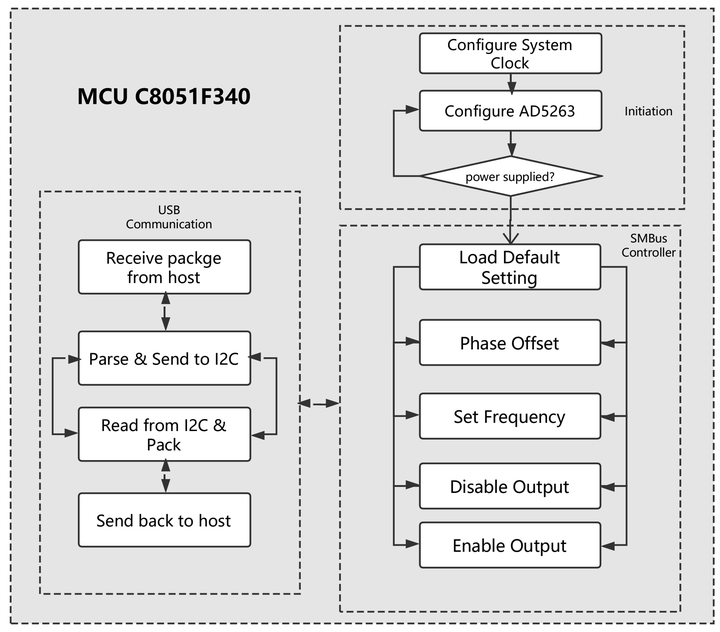

Fig.3. Block Diagram of MCU Firmware

Fig.3. shows the structure of firmware, at the beginning of procedure, MCU would set up the system clock, register the interrupt vectors, configure USB and SMB controller and disable the hardware watch dog. Finished this basic startup routine, MCU would configure power support module through I2C bus.

When a USB write event happened, MCU would enter the USB interrupt. In the interrupt, MCU will parse the command sent by host and record the information of this command. Back to main procedure, MCU would perform the operation as host indicated. Fig.4. shows two kind of process MCU would perform, including I2C read and I2C read.

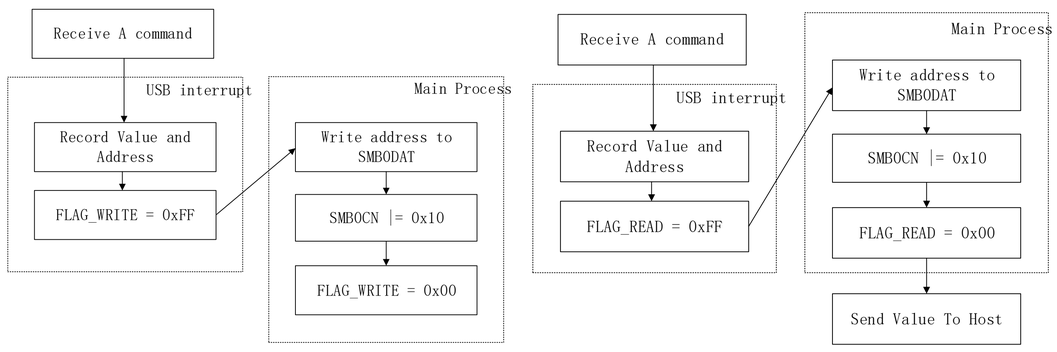

Fig.4. The I2C write and I2C read operation

3.Design of Host Program

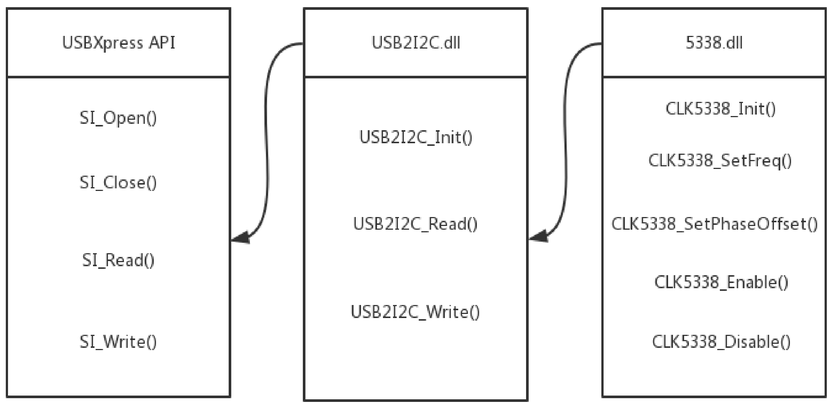

Fig.4. Block Diagram of Host Program

We try to decouple the host software into 3 layers, as shown in Fig.3, the fundamental layer drives the USB interface, and provide API for upper layer to read and write through USB. The first layer will pack up the protocol of command, which make it less complicated to instruct MCU. The second layer is the most important one, as all the configure processes were done in this layer, it calls the API provided by fundamental layer, and provide several API, including modifying the frequency of output clock signal, changing the phase and latching each channel of output. The third layer, application layer, is the user program which calls the API of second layer.

Bibliography

1. SILICON, L. "USB Xpress Programmer's Guide." (2007).
2. Xiao, L., et al. "LOCx2, a low-latency, low-overhead, 2× 5.12-Gbps transmitter ASIC for the ATLAS Liquid Argon Calorimeter trigger upgrade." Journal of Instrumentation 11.02 (2016): C02013.