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The Design and Testing of the Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade

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The Address in Real Time (ART) Data Driver Card (ADDC) is designed to transmit the trigger data in the Micromegas detector of the ATLAS New Small Wheel (NSW) upgrade. The ART signals are generated by the front end ASIC, named VMM chip, to indicate the address of the first above-threshold event. A custom ASIC (ART ASIC) is designed to receive the ART signals from the VMM chip and do the hit-selection processing. Processed data from ART ASIC will be transmitted out of the NSW detector by GBTx serializer and VTTx optical transmitter module through fiber optical links.
The ART signal is critical for the trigger selection in ATLAS experiment thus the functionality and stability of the ADDC is very important. To ensure extensive test of the ADDC, a test platform based on FMC card and special firmware/software are developed. This test platform works with the commercial Xilinx VC707 FPGA development kit, it can test all the functionalities and long term stability of the ADDC even without other NSW electronics boards. This paper will introduce the design, test procedure and preliminary test results of the ADDC and the FMC based test platform.

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