A multi-channel DAQ system based on FPGA for long-distance transmission in nuclear physics experiments

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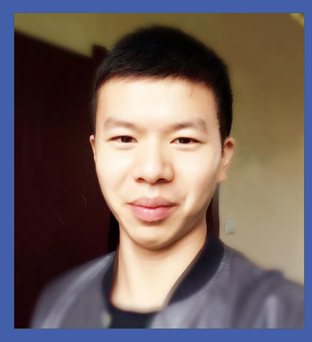

1. Introduction

Data acquisition(DAQ) system is an important information system in nuclear physics experiment. The main function of DAQ system is to collect signal from detectors in nuclear physics experiment and transmit signal to workstations through transfer medium. The workstations receive and store data in order that researchers complete data processing and analyzing to get the information they want.

2. System architecture

With development of science and technology, the scale of nuclear physics experiments is getting larger and larger. Large-scale nuclear physics experiments are usually accompanied by several thousand channels of data, the order of magnitude of which reaches Gb/s. Meanwhile the detectors and workstations are often separated by several kilometers or even tens of kilometers. Therefore a DAQ system for large capacity and remote real time transmission is needed. Optical fiber transmission is one of the most common method of long-distance data transfer. The advantages of optical fiber transmission are high bandwidth, no interruption from electromagnetic noise and long-distance transmission. Generally data transfer speed of single-mode optical fiber reaches Gb/s for several kilometers. Considering the advantages of optical fiber transmission, we designed a DAQ system with large-capacity and remote real time data transmission based on streaming mode, the core of which is FPGA. Taking advantage of hardware parallelism, FPGAs provide more powerful computing ability than digital signal processors (DSPs) and offer more flexibility. The simplified prototype architecture of nuclear physics experiments is shown in Fig.1.

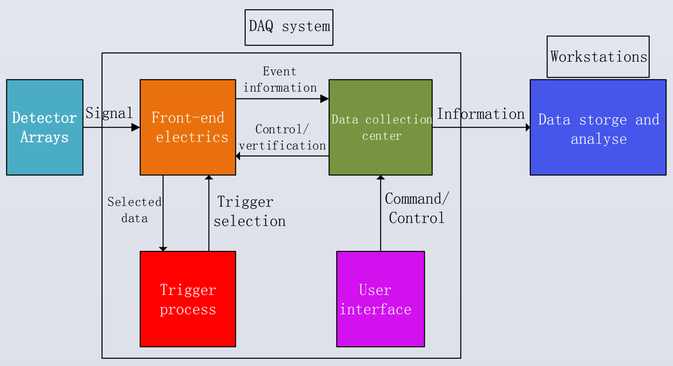

Figure 1. Architecture of readout electronics system

One of the advantages of the system is real-time transfer of large-capacity data based on streaming transmission mode，which utilizes error detection and correction mechanism to ensure the transmission of high reliability. Another major advantage of the system is high-speed high-precision data acquisition and remote transmission by optical fiber. The system utilizes an 8-channel, 24-bit simultaneous sampling analog-to-digital converter (ADC) at a speed of 16 kilo samples per second (KSPS). Signal-to-noise ratio(SNR) reaches 108dB at 16 KSPS in high resolution mode.

3. Hardware architecture

According to the design requirements, the functional block diagram of core circuit board of DAQ system is shown as Fig.2. The board consists of the on-board power system, FPGA, optical interface unit, electrical interface unit and ADC module. We utilized the Xilinx Kintex-7 FPGA as the central processing unit so as to guarantee that the FPGA have sufficient memory blocks and process data with adequate speed. The FPGA is configured by a Serial Peripheral Interface(SPI) flash and the system clock is 40MHz provided by external crystal oscillator. For electrical interface, low-voltage differential signaling (LVDS) technology is used to exchange data and command. LVDS is a current-driven differential signal transmission technology. It is suitable for short distance cable high-speed transmission. The data transmission of LVDS rate is up to 655Mbps, which meets most of the data transfer rate requirements of physics experiments. The key elements of optical interface is Small Form-factor Pluggable(SFP) transceiver, which is a small, hot-pluggable optical transceivers for optical communications

applications. A kind of SFP transceiver was applied to exchange data and command between the board and workstation, the transmitting rate of which reaches 1Gbps and is far exceeding the system bandwidth of the prototype architecture.

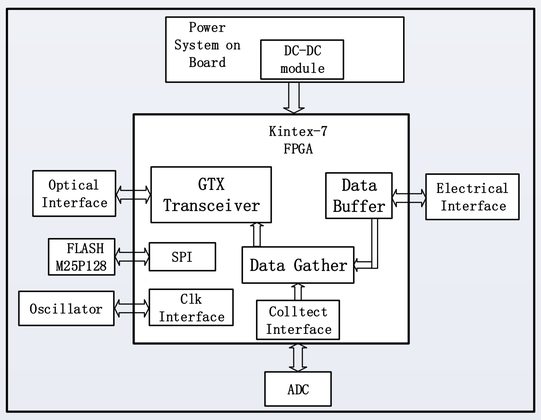

Figure 2. Simplified architecture of the core circuit board

4. Signal Flow

The simplified signal flow of core board is shown in Fig.3. In nuclear physics experiments, ADC acquires analog signal from detector and converts it to digital signal. FPGA receives signal from ADC and sends command signal to ADC. At the same time, electrical interface is used to receive data from other circuit boards. The two part of data is merged in First Input First Output(FIFO) inside of FPGA and then sent to workstation for storage and analysis. The core board mainly undertakes collection of local data and transmission of external data and local data.

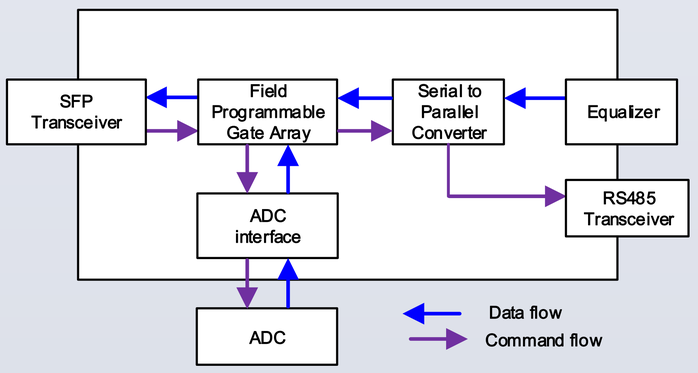

Figure 3. Signal Flow

5.Test Result

The core board of the system is mainly responsible for data summary and transmitting data to workstations remotely. To transmit data to workstation over long distance, we have used the GTX transceiver of Kintex-7 FPGA. It is the physical layer foundation that achieves high-speed serial data transmission, of which the line speed reaches up to 500Mb/s-12.5Gb/s. Meanwhile, the Integrated Bit Error Ratio Tester(IBERT) provided by Xilinx is used to test and debug the GTX transceiver's transmission capabilities and performance. The test result is shown as Fig.4. The bit error rate(BER) is pretty low, and the magnitude is about 10-12, which indicates that the transceiver link status is normal. We utilized Integrated Logic Analyzer(ILA) core for further testing, which is a logic analyzer that can used to monitor programmable logic signals and ports inside a design project. Test result is shown as Fig.5. The system transmission clock is 50MHz and the internal data bit width is 16bit. System runs at a bandwidth of 1Gbps after 8B / 10B encoding for the internal data. The sender generates a counter within the FPGA in the loopback mode. Furthermore the receiver is able to receive the correct signal.

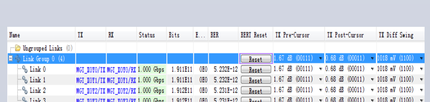

Figure 4. IBERT test

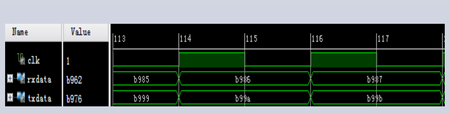

Figure 5. Test Result

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