Upgrade of HADES data acquisition and event building software for FAIR phase 0

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***Abstract*—The High Acceptance Di-Electron Spectrometer (HADES) is a versatile detector system that has been operational at the GSI heavy ion accelerator facility for about 15 years.**

For the "FAIR phase 0" beam time campaign in summer 2018 a number of HADES components are being upgraded, such as the RICH and the ECAL. Both detectors will be read out by dedicated front-end boards with FPGA-based TDCs of the TRB3 family. These TDCs provide an excellent timing precision of about 15 ps. The expected increased data rates, and the necessary software calibration of each TDC channel in the new systems, require significant changes in the DAQ set-up.

This contribution will discuss the software aspects of the DAQ system, such as the network topology of front-end and event builders, implementing TDC calibration directly in event builder nodes, and reducing the amount of data stored on the disks.

I. Introduction

THE High Acceptance Di-Electron Spectrometer (HADES) is a detector system to investigate proton and heavy ion collisions in the few AGeV energy region [1]. It has been operational in various experiments at the GSI accelerator facility since 2002. HADES consists of several subcomponents, for example a START/VETO detector with time of flight detectors (TOF), a Ring Imaging Cherenkov detector (RICH), 4 planes of Multi-wire Drift Chambers (MDC), and an Electromagnetic Calorimeter (ECAL). The data acquisition (DAQ) of these components is triggered and controlled by the TrbNet DAQ network [2]. The digitized data is concentrated in about 30 subsystem hubs and is send as UDP packets via Gbit Ethernet to a cluster of event builder servers. Here up to 16 event building processes receive these data, combine them to full events, and store parallel streams of raw event files to hard disk, and as well to a tape archive. In previous experiments a typical data rate of 150 Mbyte/s could be written. Since 2012 this event building software is based on the Data Acquisition Backbone Core (DABC) framework [3].

For the "FAIR phase 0" beam time campaign in summer 2018 a number of HADES detector components are being upgraded, such as the RICH and the ECAL. The RICH will be newly equipped with 428 Multi-Anode Photomultipliers (MAPMT) of 64 pixels each, and the ECAL is a new construction with 978 lead glass modules. Both systems will be read out by dedicated front-end boards with FPGA-based TDCs of the TRB3 family [4]. These TRB3 TDCs work by the "tapped delay line" method and provide an excellent timing precision of about 15 ps. To achieve this, however, a complex calibration procedure of each individual channel is required which should run frequently to cope with drift effects over time.

The expected increased data rates and the TDC calibration purpose of the new systems imply significant changes in the DAQ set-up and the topology of the event builder network.

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II. Hardware upgrade

The existing RICH detector is being upgraded with new Hamamatsu MAPMT sensors. The read-out is handled with dedicated front-end boards DIRICH [4] (see Fig. 1). The DIRICH module contains one TRB3 FPGA for 32 TDC channels, or one half of each MAPMT sensor. With 428 MAPMTs this results in a total of 27392 TDC channels. Per triggered event several TDC hits with time and time over threshold information can be acquired for each channel.

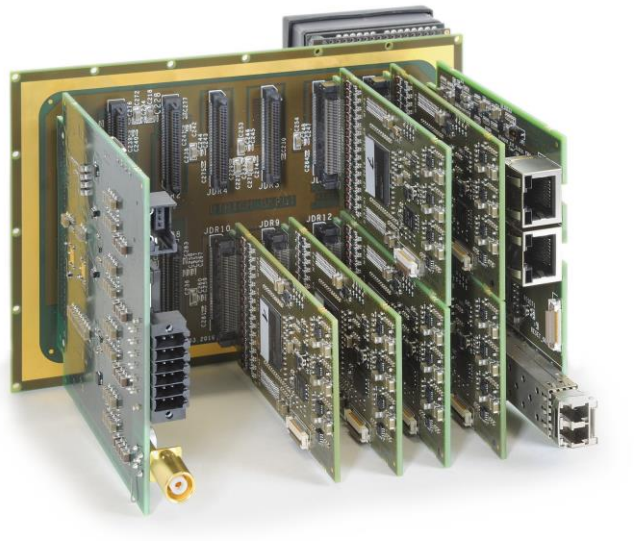

Figure 1: A DIRICH carrier board equipped with several DIRICH modules, and power and I/O modules. This device may read out 6 MAPMTs of the new HADES RICH detector which will be plugged to the backside. Photo by Gaby Otto, GSI

Additionally, the forward ECAL has been newly constructed as an array of 978 lead glass crystals, read out by TRB3sc crates with PaDiWa AMPS FEBs (charge to width conversion) [4]. Data from this read-out delivers the same TRB3 TDC message format as for the RICH.

III. TDC CALIBRATION

The DABC event builder framework offers the possibility to calibrate the TRB3 TDC fine time values "on the fly" before writing the raw subevents to disk [5]. This has been implemented for different calibration methods (statistical approach, temperature calibration function, simple linear calibration) and was verified in several laboratory test benches. Moreover, advanced analysis and monitoring techniques in such a DABC code have been helpful to further understand functionalities and limitations of the FPGA TDC. Especially the status of the calibration can be inspected by the DABC web interface for any event collecting node [5].

It is planned that in the final HADES production beam times, the DABC event builders store the time calibrated TDC messages only, thus reducing significantly the amount of data written. In the testing phase, it is possible to store the original uncalibrated data additionally. This allows checking the calibration with offline analysis afterwards. If a frequent calibration of the TDCs during the beam time was required, a "calibration type trigger" could be distributed to the TRB3 front-ends which lets them send uncorrelated data on all TDC channels to be used by the DABC calibration procedure. Such calibration triggers could use the SIS accelerator spill pause where no regular detector signals are to be expected.

IV. EVENT BUILDING TOPOLOGY

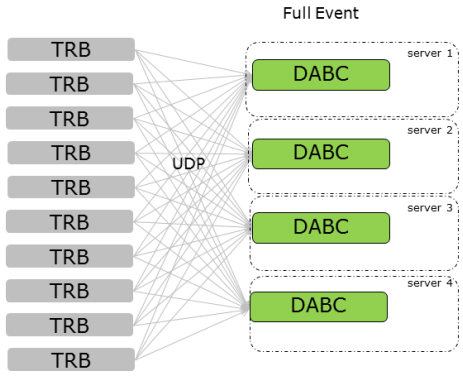

Figure 2: Previous HADES event building network topology: Each trb front-end hub sends to all event builders via UDP in an "n x m barrel shifter" scheme. Figure taken from [3]

To fully benefit from such an online TRB3 TDC calibration, the topology of the event building network is going to be changed (see Fig.2).

In the previous set up, each front-end hub was sending data via Gb Ethernet UDP connections to all receiving event builder nodes in a barrel shift mode (Fig.2). Instead, each front-end will send to a dedicated entry server only and the full event combination is done by a second TCP/IP "builder network" BNET (Fig.3) [3]. So only such BNET entry servers have to run the TDC calibration software which are receiving the TRB3 data. In general, the load of the event building entities can be tuned better according to the different data rates from individual detector components.

Event building with such configuration has been tested in principle already with the existing front-end hardware. This just required a change in the trbnet hub configuration which schedules the data destinations of the subsystem packets.

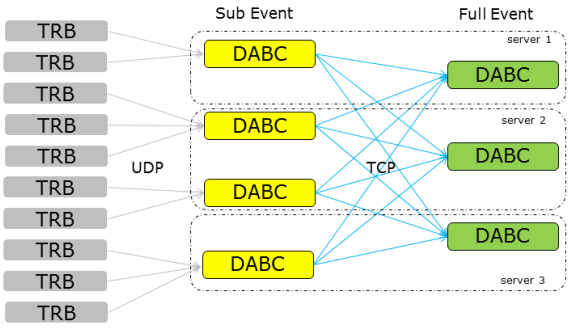

Figure 3: New HADES event building network topology as tested: The trb front-end hubs send via UDP to dedicated "subevent input" processes. Full events are built via TCP in a second stage builder network (BNET). Figure taken from [3]

V. OUTLOOK

For the upgraded FAIR-0 beamtime set-up, not only the BNET event builder topology, but also the complete trbnet hub architecture and DAQ network is going to be changed. Also the subevent components of existing detectors are aggregated differently by new TRB3sc hardware, and with improved Ethernet data connections to the event builder servers. Moreover, the event builder hardware will be exchanged by new server PCs. So the complete DAQ and event building system will be newly configured and optimized for the BNET topology.

The HADES experiment expects to take data from Ag-Ag collisions at 1.65 A GeV with this system in August 2018. Even before the event builder software will be tested and optimized, gaining experience for the production runs.

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