Development of FEB Configuration Test Board for ATLAS NSW Upgrade

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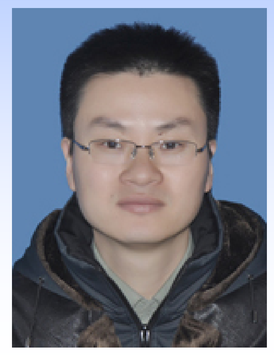

The FEB(front end board) configuration test board is developed aiming at the requirement of testing the new generation ASIC(application-specific integrated circuit) chips and its configuration system for ATLAS NSW(New Small Wheel) upgrade, this research studies the configuration of the key chips on the FEB–VMM3 and TDS2 using GBT-SCA, develops multiple level standards and communication protocol, and verifies the whole data link. It provides technical reference for prototype FEB key chip configuration and data readout, as well as the final system configuration.

1. Introduction

The ATLAS trigger system is responsible for recording the signal of interesting events, and it can eliminate most of the background events so as to greatly reduce the write rate, the ATLAS uses multi-layer trigger mode to build highly selective and efficient trigger system, so as to achieve efficient reception of collision events, and reduce overall data rate. The ATLAS hardware gets the trigger information from the CALO detectors and the Muon detectors, and reduces the input data rate from the 40MHz to about 75kHz. The NSW trigger is a complex and highly configurable system, each piece of FEB has a GBT-SCA chip on it specially designed for FEB mode configuration. This paper mainly discusses the development process of FEB configuration test board, it mainly completes the verification of FEB system configuration function, masters the use of GBT-SCA, configures VMM3 and TDS2 chips on FEB, and studies the configuration process of NSW.

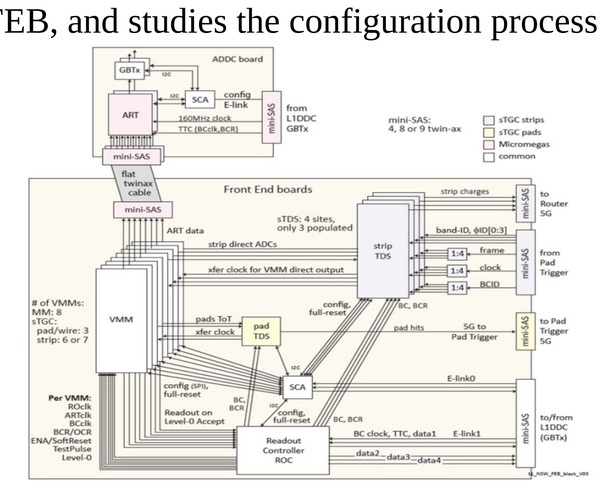

Fig.1 of NSW Configuration.

2. Design of FEB Configuration Test Board

The diagram of the FEB configuration test board is illustrated in Fig.2. The board is divided into the following modules, including FPGA control module, GBT-SCA configuration chip, VMM3 chip, TDS2 chip, network communication module, data interface module, E-link interface and GTX high-speed interface, power supply module, and clock module.

Fig. 2 Diagram of Hardware Design

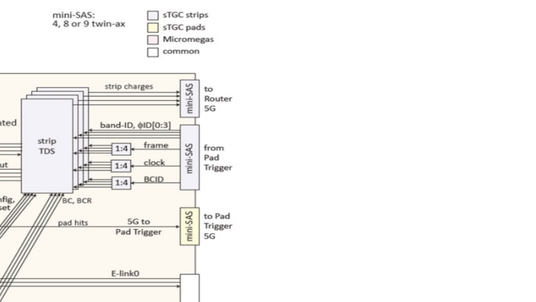

Fig. 3 Diagram of Firmware Design

FPGA on the FEB configuration test board is mainly responsible for network communication with the host computer, data communication with GBT-SCA chip, data interface with VMM3, and high-speed data interface with TDS2. Figure 3 is FPGA firmware block diagram of configuration test board.

The FPGA firmware includes network transmission module (Ethernet Interface Control/Command Decode), clock module(PLL), data control module (Data control), SCA packet data generation module (SCA packet generator), communication control module (Comm Contrl), E-port module, GBT-SCA interface.

3. ConfigurationTest

The FEB configuration test board is mainly used to test the GBT-SCA, VMM3, and TDS2 chips on the board, and interactivity with other hardware, including communication interface relationships, such as GBT-SCA communicate with VMM3, GBT-SCA communicate with TDS2, and GBT-SCA communicate with FPGA. GBT-SCA is the core chip of the configuration test board and researching on controlling of GBT-SCA is the key of FEB configuration test board.

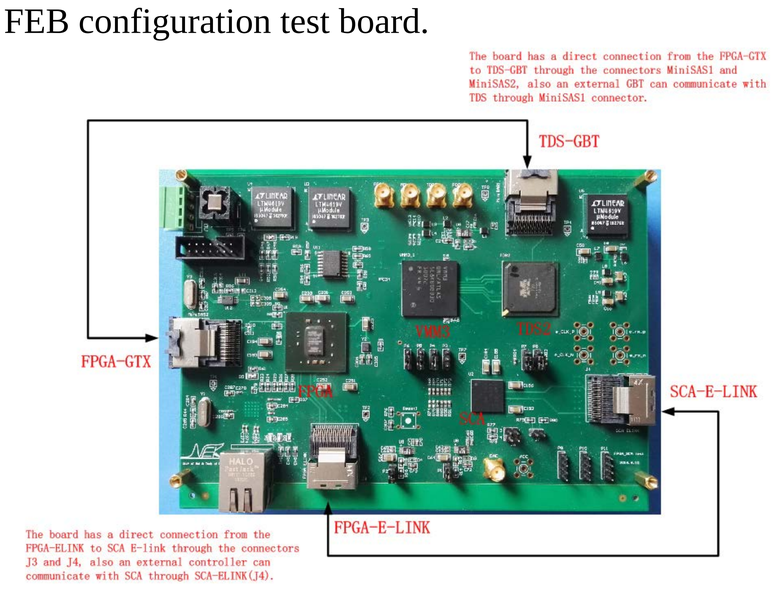

Fig.4. Test of the Configuration Test Board

The test connection schematic of the FEB configuration test board is shown in Figure 4, the FPGA on the board is used as the main control device. The generation of communication data is controlled by the host computer software, and the communication protocol of the control room is simulated. It is transmitted to FPGA through the network, then, FPGA is transmitted to GBT-SCA through E-link data transmission protocol. The interface is mini-SAS and connected by mini-SAS cable. GBT-SCA communicate with VMM3 through the SPI interface and communicate with TDS2 through the I2C interface. The output data rate of TDS2 is 4.8Gbps, and the data of TDS2 is transmitted to FPGA for verification, and it is connected with FPGA through the mini-SAS interface. The FEB configuration test board we designed can be independent of the other modules of the system, and the configuration function can be verified by a computer and a FEB configuration board.

4. Conclusion

The FEB configuration test board realizes the operation and control of the SCA chip, including E-link, SPI, I2C, GPIO communication, implements the configuration of VMM3 and TDS2, while verifying the TDS2 4.8Gbps high-speed data transfer function. FEB configuration test board also conducted electronic integration test in CERN, it completed communication with Pad trigger and Router board.