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## Scanning Test System of p/sFEB for the ATLAS Phase-I sTGC Trigger Upgrade

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The ATLAS detector which is one of the four experiments at Large Hadron Collider will fulfill Phase-I upgrade to extend the frontier of particle physics. The upgrade will replace the inner detector (Small Wheel, SW) of the end-cap muon spectrometer with the “news mall wheel” detector (NSW), which consists of the Small-strip Thin Gap Chamber (sTGC) and Micromegas (MM). The Pad Front End Board (pFEB) on sTGC is developed to gather and analyze pads trigger. The Strip Front End Board (sFEB) is developed to accept the pad trigger to define the regions-of-interest for strips readout. About 2000 p/sFEBs will be produced for final delivery and engineering backup. Before the p/sFEBs are mounted on the detector, we need to test the performance of all the p/sFEBs. The performance testing of each p/sFEB includes baseline test, threshold DAC calibration, internal test pulse DAC calibration, gain test and dead channel test, each of which are very important for the front-end electronic system. Therefore, the scanning test system is designed according to the test requirements of the p/sFEB. In this test system, a simulation signal board is developed to generate different types of signal to the p/sFEB. PC software and FPGA XADC cooperate to achieve the scan test of analog parameter. The PC software is written based on Qt platform using the standard C++. The automatic test function of the pFEB has been successfully realized. This system has the advantages of convenient GUI, smooth operation, convenient user operation and good stability.

### **Description**

DAQ Board

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Yes

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