A 2.5 $\text{ps}$ RMS time synchronization for multiple high-speed transceivers in FPGA

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Introduction

Quantum Key Distribution (QKD): absolute security in principle.


Introduction

Global QKD network.
All time.
LEO, GEO.
Both methods need multichannel electric drivers with a deterministic phase skew.
Solution for multichannel electric drivers

Low speed (< 100 MHz)
Parallel drivers with same clock

Clock Generation

Driver 1
Driver 2
...
Driver N

High speed (> 1 GHz)
Serial drivers with independent clock

Clock Generation

Driver 1

Clock Generation

Driver 2
...

Clock Generation

Driver N
Introduction

High speed application

Structure of GTH embedded in FPGA

Clock divider

- Every time the system powers up or resets, clock dividers release at a random time.
When multiple channels are included, there appeal random skew among channels.
Random skew test

Conditions:
- GTH run at rate 2.5 Gbps,
- PLL output period 400 ps,
- Parallel data width 16,
- Parallel period 6.4 ns,
- System powers up or resets for 225 times.

Results:
The skew conforms to a random distribution, it is the integral multiple of 400 ps.
How to solve the intrachannel random skew?

- Self-phase alignment: 22 ps RMS precision, the maximum is 100 ps.

- Another approach

- TDC measured the intrachannel skew.
- PI tuned the GTH’s clock phase.
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PI Controller

PI embedded in GTH, Tuning the clock phase of PLL output,

PI tuned step size

\[
\text{STEP}_{(\text{UI})} = \frac{W_{pi}[3 : 0]}{64 \times D_{txout}}
\]

- \( W_{pi} \): ranging from 1 to 15,
- 1 represent the minimal step size.
- \( D_{txout} \): Serial divider.

- The UI is 400 ps, \( D_{txout} \) is 2, so the theoretical minimal step size is 3.125 ps.
A test for the precision of PI adjustment

- Good linear
- Adj. R-Square equals 0.99983
- The slope is 3.79 ps

3.79 ps tunable precision is enough for the system running at rate 2.5Gbps.

The relationship between the step value and the tuned times.
Time delay line TDC

- Hit event: hit signal needing to measure,
- REF Clock: the system clock,
- TDL: time delay line,
- Encoder: turn the temperature code to bin code,

Constructing TDL with carry chain.

- UltraScale Kintex KU040,
- Carry8: **8 carry-out bits**, 8 data bits. 16 delay units at most.

Define parameter $M$ represent divided factor of Carry8.
Tests of performance of TDC

- The system clock period is 6.4 ns.
- The number of taps with M=2 is 309.
- The number of taps with M=4 is 613.

The bin size distribution

M=2, LSB = 20.4 ps

[Graph showing bin size distribution with M=2, LSB=20.4 ps]

M=4, LSB = 10.2 ps

[Graph showing bin size distribution with M=4, LSB=10.2 ps]
The DNL in most bins are smaller than $\pm 1$ LSB and the maximum is about 2.5 LSB.

The DNL with $M = 4$ are smaller than 2 LSB in most bins, worse than that $M = 2$.
The fitting INL in most bins is smaller than $\pm 2$ LSB.

The fitting INL in most bins is smaller than $\pm 4$ LSB.

The fitting INL shows that a system error exists, which attributes to the large delay spanning banks in FPGA.
TDC

Resolution test

Resolution test: a delay line test was applied to measure TDC resolution by constructing two identical delay chains.

Resolution (M=2): 17.8 ps~24.6 ps RMS.

Resolution (M=4): 18 ps RMS. Flatter.
The parallel clock of master channel is routed as the system clock. All slave channels are combined into a mux.
Test for precision of intrachannel time synchronization

Self-phase alignment: the maximum is 105 ps, the RMS is 22 ps.

TDC-based alignment: the maximum is 14.7 ps, the RMS is 2.5 ps.
Test for synchronized precision at different value

- Self-phase alignment: the intrachannel skew is not capable of adjusting.
- TDC-based alignment: the intrachannel skew can be tuned to arbitrary value.

Synchronization precision at different points sampling 25 times.

Ranging from 2.2 ps~4.4 ps.
Outline

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Summary

- **Conclusion**

  With a PI and a TDC, we implement a high-precision 2.5 ps RMS time synchronization among multichannel serial transceivers. Besides, the intrachannel skew can be locked to arbitrary offset with approximate precision.

- **Outlook**

  The employed TDC resolution is 18 ps, we can further improve the TDC resolution with proper methods, such as INL calibration, bin decimation, and multiple chains measurement. And eventually, a higher-precision time synchronization is achievable.
Thank you!