

Nanoseconds Timing System Based on IEEE 1588 FPGA Implementation

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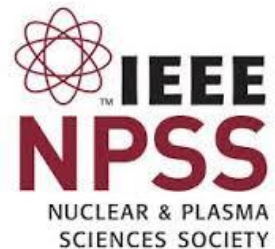
On behalf of

JUNO Padova Electronics Group & JUNO Collaboration



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21st IEEE
Real Time Conference
June 9-15, 2018
Colonial Williamsburg, VA, USA



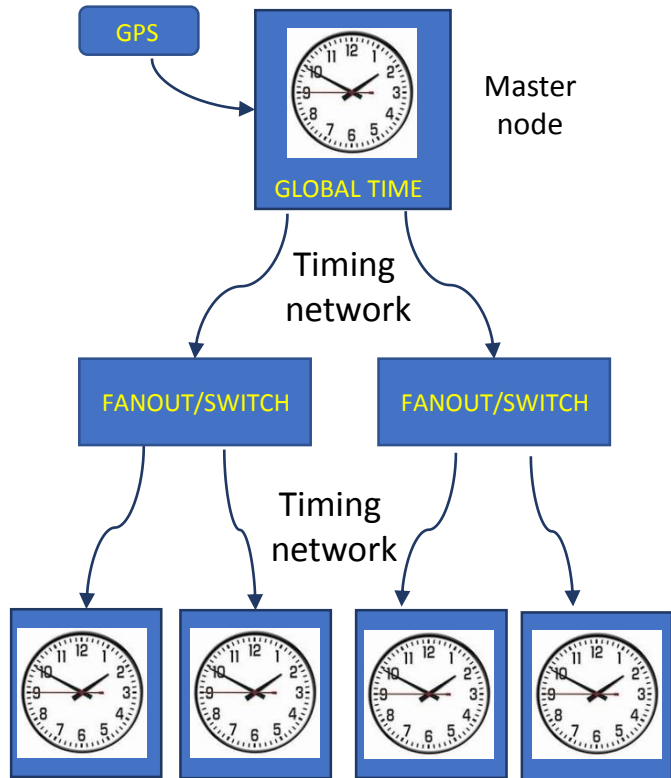
Outline

- Overview of the two approaches to synchronization normally used in physics experiments.
- General introduction to the JUNO synchronization scheme and constraints.
- Design and implementation of a nanoseconds timing system based on a hardware implementation of the IEEE 1588-2008 over a full duplex and deterministic latency communication channel.
- Serial link synchronization and marginal capturing.
- Test setup and results achieved.
- Limitations of the proposed synchronization method and possible improvements.

Different Approaches to Synchronization

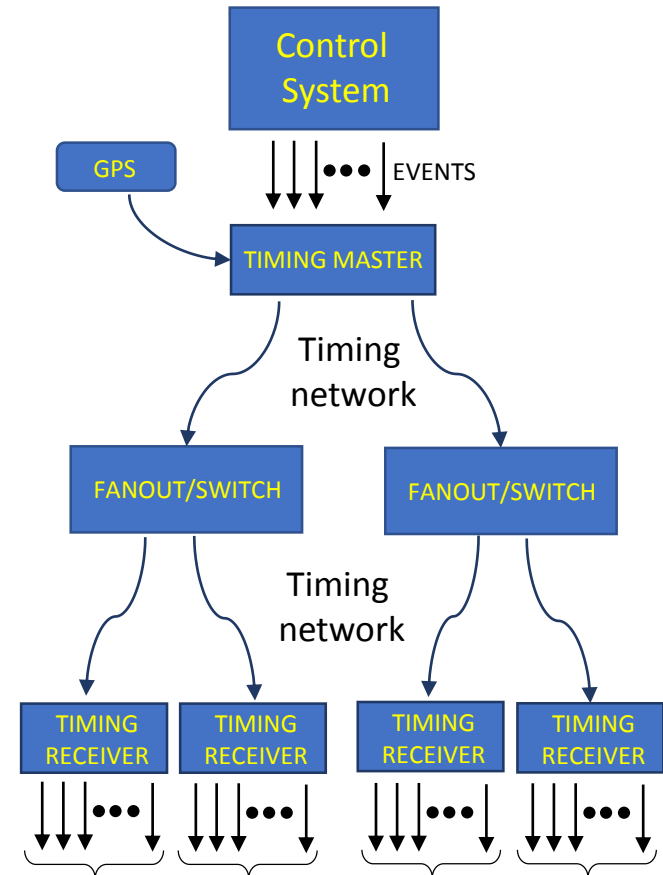
The timing system is an essential part of a physical facility and it synchronizes actions between the distributed nodes within the target temporal resolution.

① Time - based



The timing receivers nodes hold an accurate local copy of global time

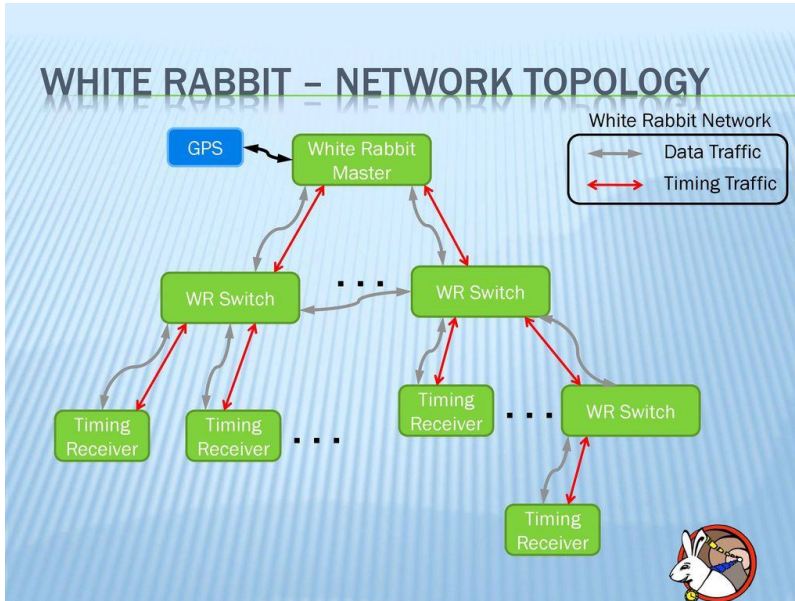
② Event - based



EVENT CODEs converted to synchronized digital output pulses.

Timing Off-the-Shelf Solutions

1 Time - based

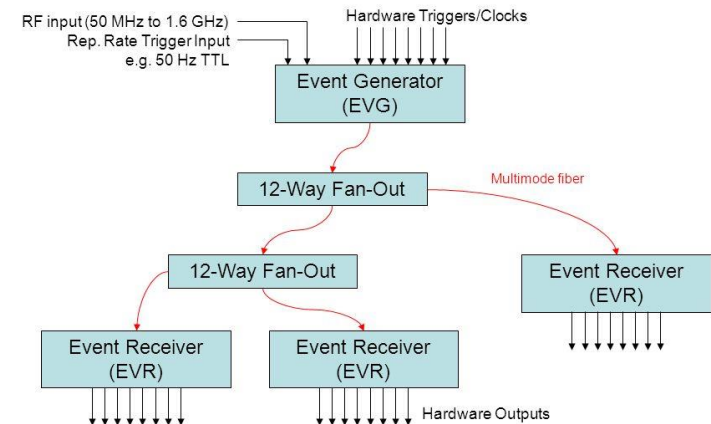


White Rabbit relies on an accurate copy of the global time at the Timing Receiver level for performing synchronized tasks. WR exploits the IEEE 1588 standard and the 1000 base-LX Synchronous Ethernet and it extends the timing resolution to the sub-ns range with a phase detection system based on a Digital Dual-Mixer Time Difference.

2 Event - based

Micro-Research Finland Oy

Timing System Topology

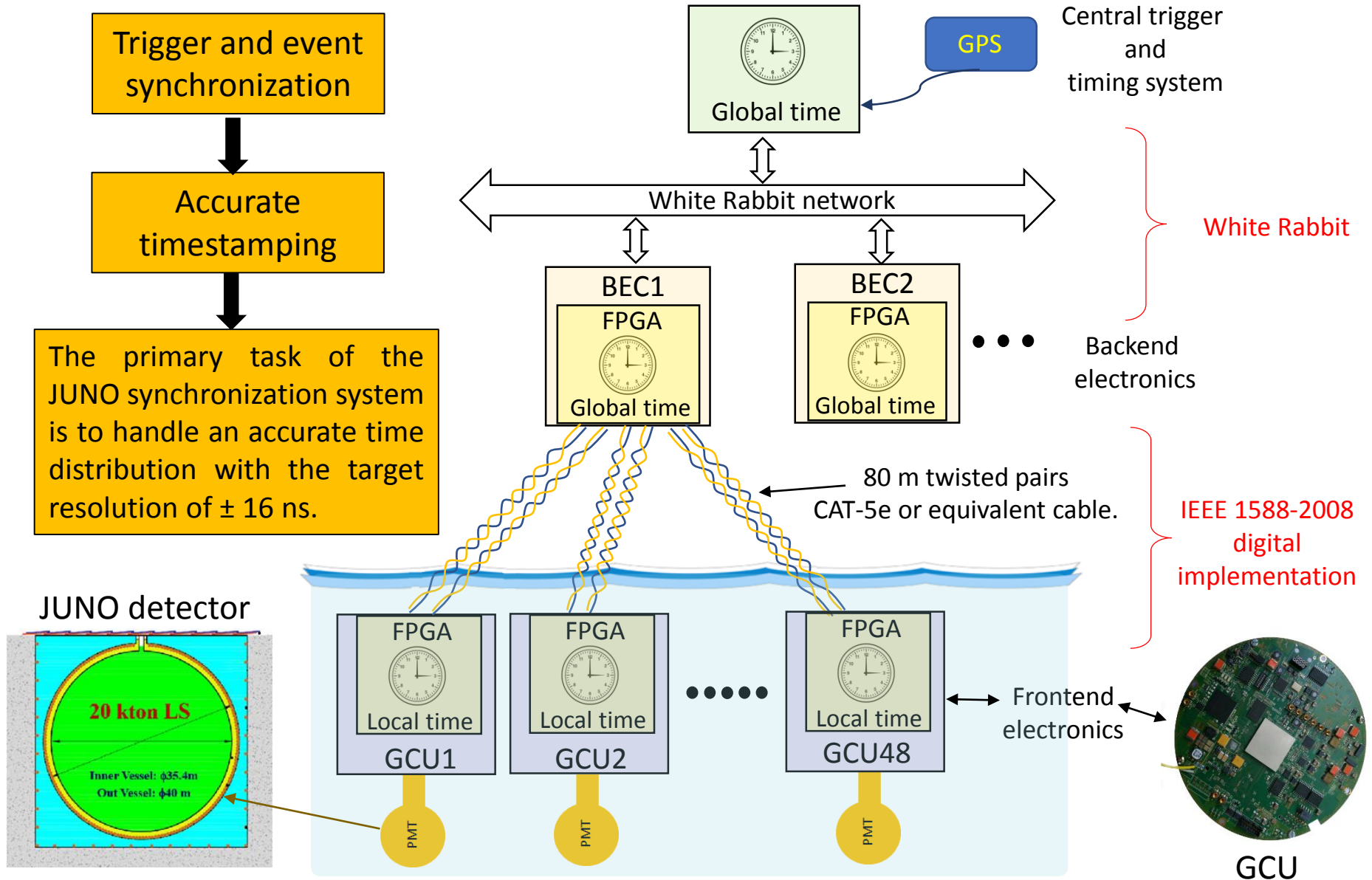


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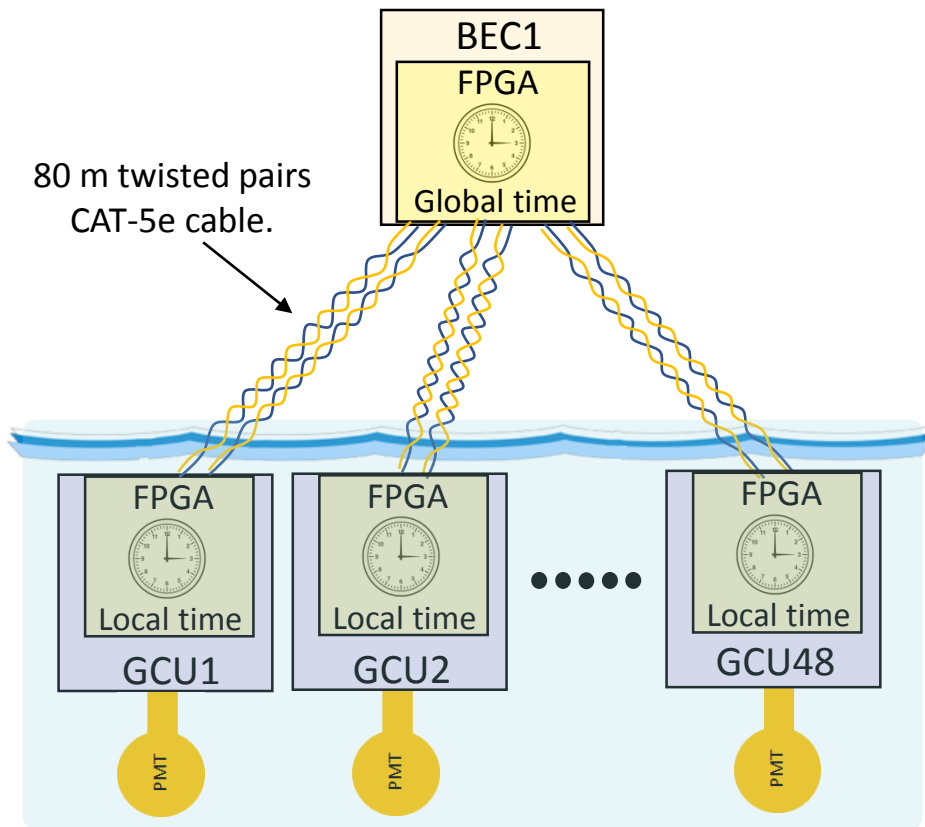
Micro Research Finland is an example of event-based timing system whose primary task is to deliver reliable, fixed and low latency control messages to all the timing receiver nodes. The event generator is the only holder of global time and converts the scheduled timing events in synchronous commands delivered through a deterministic network to an array of event receivers.

JUNO Synchronization System



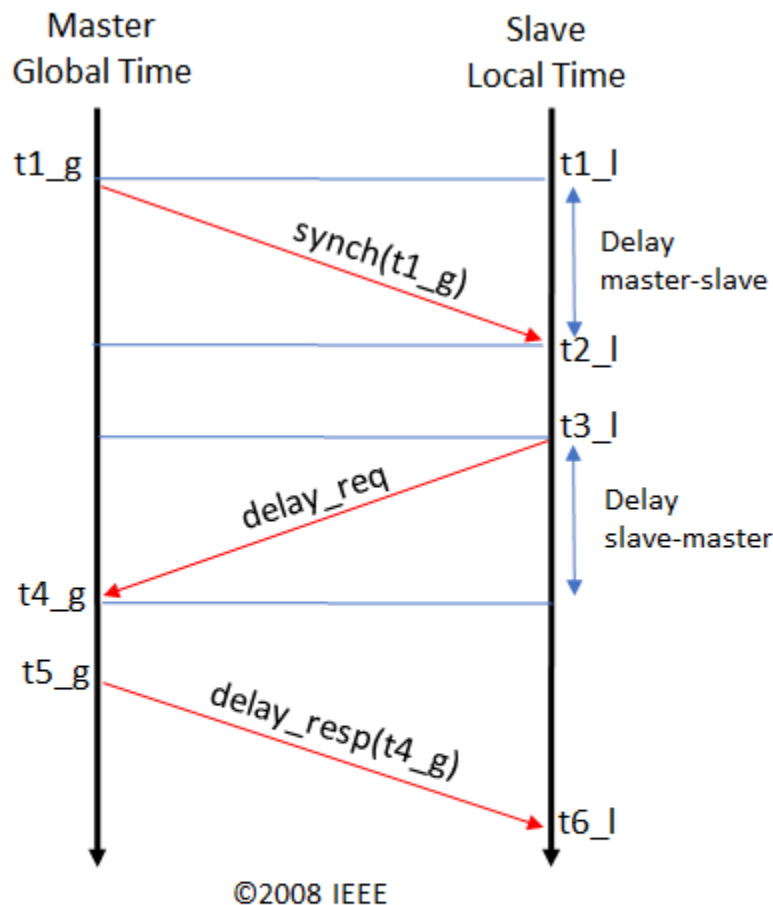
IEEE 1588-2008 Digital Implementation

The proposed research work addresses the clock offset correction mechanism between backend and frontend electronics necessary to ensure that timestamps in all devices use the same time base.



- 1) **Clock syntonization.** The global clock signal is distributed to all the GCUs as encoded information. Any GCU recovers the global clock with a CDR and counts the time locally.
- 2) Every local time will experience an offset with respect to the global time since the start of the counting is not synchronized among GCUs. The clock offset correction mechanism is based on a digital implementation of the **IEEE 1588-2008** Precision Time Protocol (PTP).
- 3) Implementation of a full duplex and **deterministic latency** communication channel between the BEC and any GCU over a couple of copper twisted pairs available.

Clock Offset Correction Mechanism Implemented



- **Assumption:** $\text{Delay master-slave} = \text{delay slave-master} = \text{delay}$
- $t1_g - t1_l = \text{offset}$ to be measured.
- The master sends the synch message to the slave and records the transmission time $t1_g$.
- The slave records the reception time $t2_l$ and computes:
- $t1_g - t2_l = \text{offset} - \text{delay}$.
- The slave sends the delay request message to master and records the transmission time $t3_l$.
- The master records the reception time $t4_g$.
- The master sends to the slave the delay message containing the $t4_g$.
- The slave computes $t4_g - t3_l = \text{offset} + \text{delay}$.
- The slave computes:

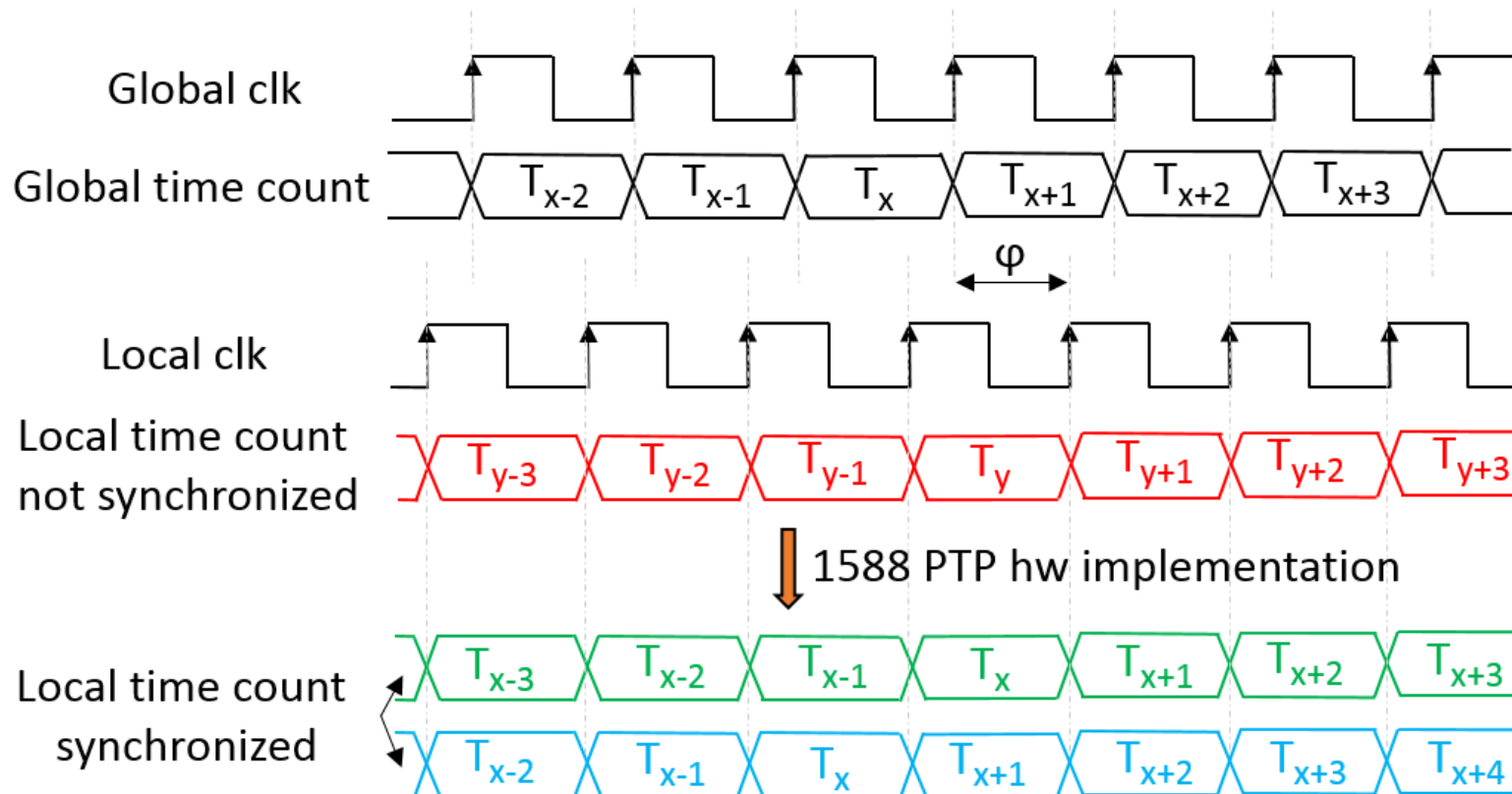
$$(t1_g - t2_l) + (t4_g - t3_l) = 2 \times \text{offset}$$
- The slave computes the offset: 1 bit right shift.

The PTP protocol is based on the assumption that transmit and receive paths are symmetric; the accuracy is degraded by any source of asymmetry in the communication channel between master and slave.

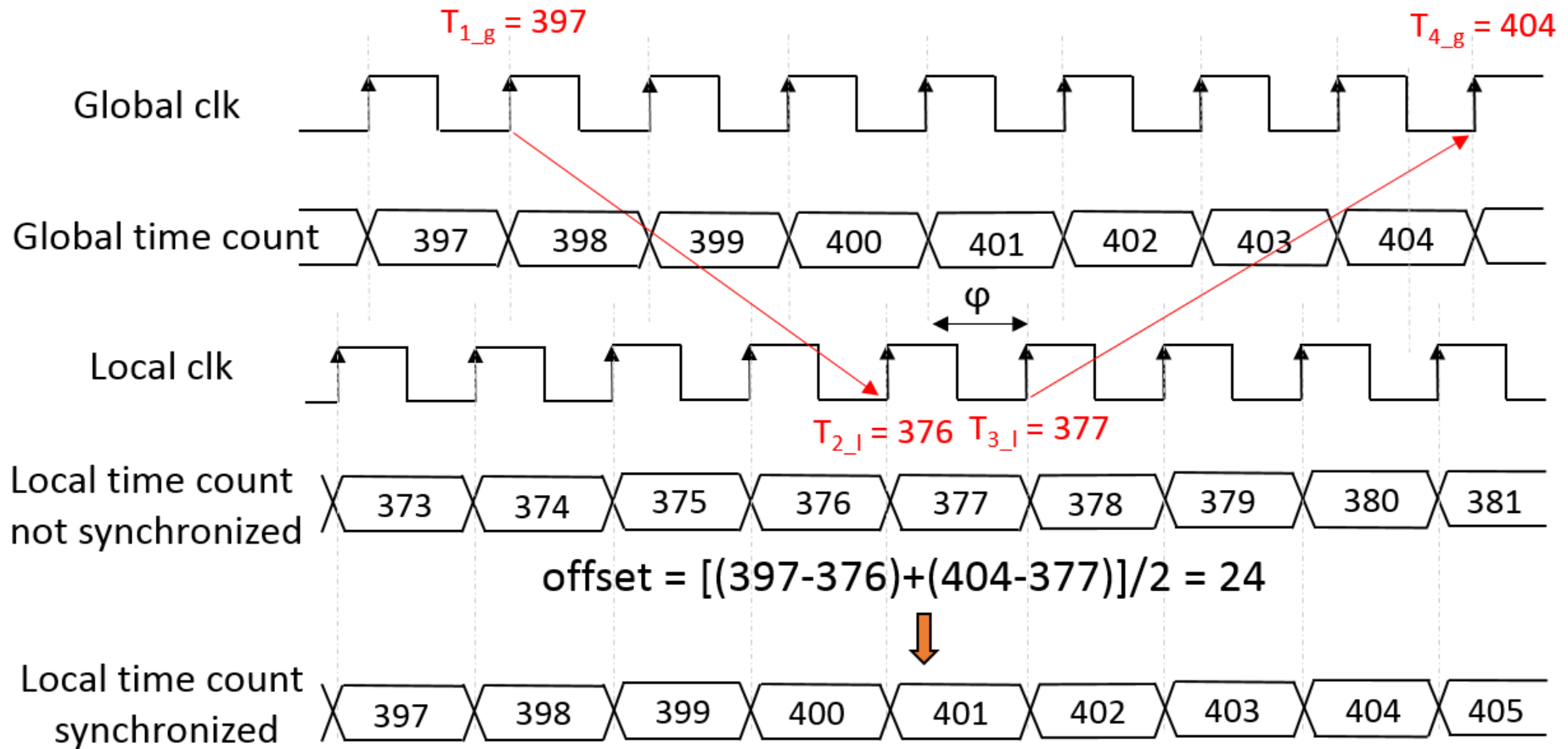
PTP Hardware Implementation Advantages

The FPGA implementation of PTP over a deterministic and low latency full duplex communication channel between master and slave gets rid of the main accuracy limitations introduced by PTP software implementations over standard Ethernet networks. The synchronization accuracy is extended to ± 1 global clock period.

- ✓ Timestamping
- ✓ Clock count
- ✓ Physical and data link layer symmetry



Offset Correction Example



ϕ is mainly determined by the transmission latency and the PTP cannot resolve this phase difference between global and local clock. ϕ is unknown but in principle, without variations of the cable length, it is invariant with a standard deviation imposed by jitter.

The Interconnection Model Implemented

PTP is not limited to Ethernet. The interconnection model implemented to ensure bidirectional messaging between master and slaves is based on the **CERN's timing, trigger and control (TTC)** system concept.

- ✓ Framing:

- Broadcast commands: 16-bit frames.
- Individually addressed commands/data: 42-bit frames.

- ✓ Error correction and detection:

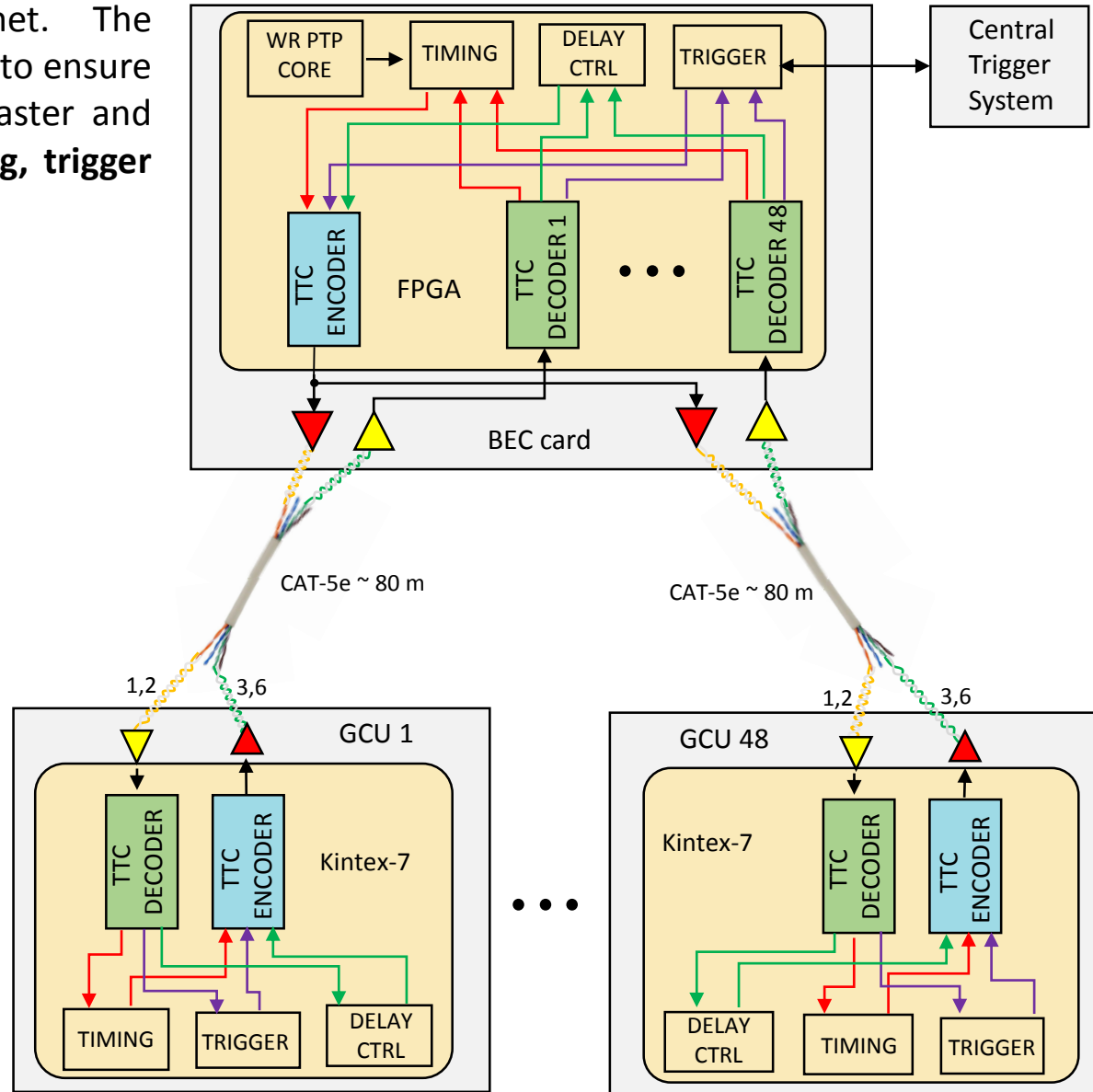
- Recovering from single bit errors (Hamming check sum)
- Detection of double bit errors.

- ✓ Cables length mismatch

- ✓ **Deterministic latency**

- ✓ Firmware asymmetry compensation.

- ✗ Cable asymmetry compensation



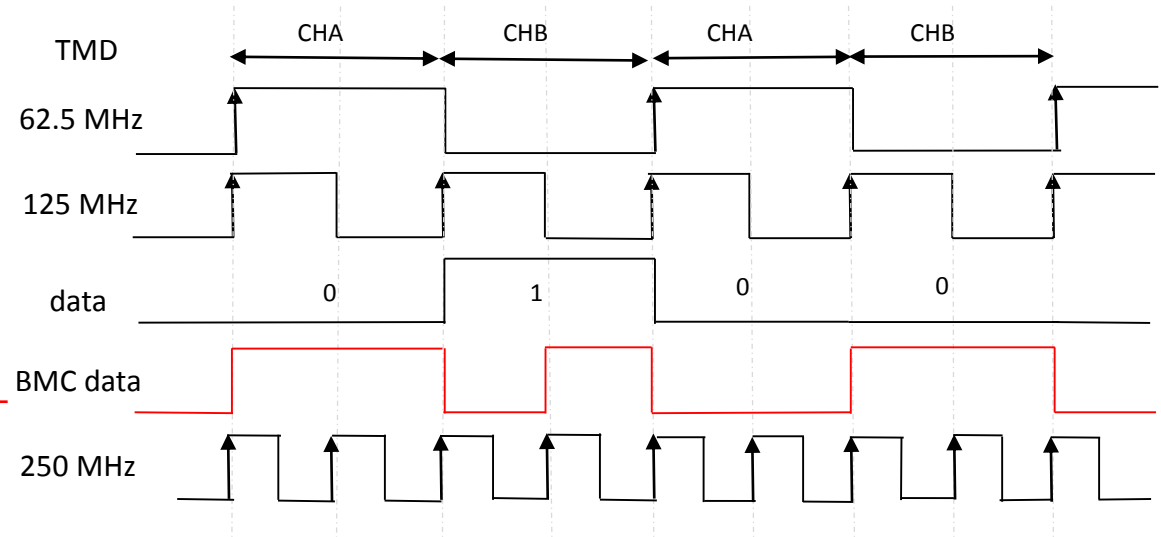
TTC Physical Layer and Clock Syntonization

The global clock signal is distributed to the frontend nodes as encoded information in two communication channels that are Time Division Multiplexed (TDM).

At physical layer data is Bi-phase Mark encoded (BMC):

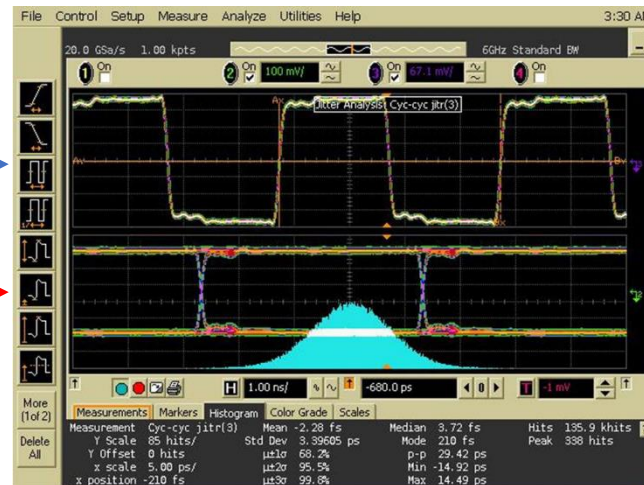
- data = 1 → bi-phase
- data = 0 → constant level

✓ DC balanced
✓ self-clocking



250 Mbps

Recovered
clock
BMC data



250 MHz

BMC
data

Kintex-7

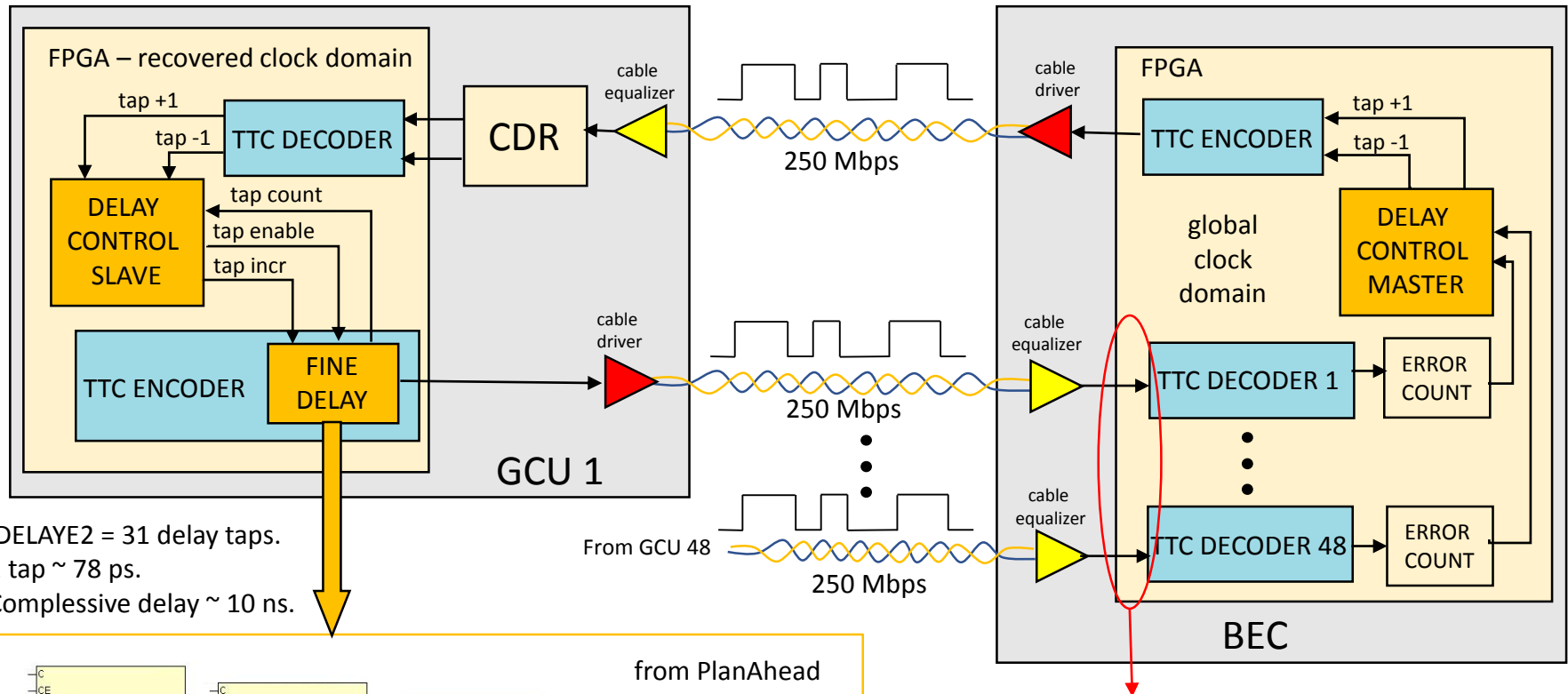
Syntonization

Serial link
synchronization

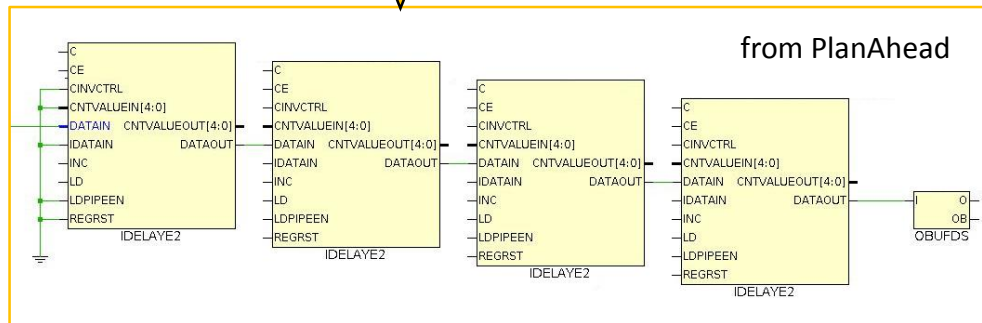
Low jitter

ADN2817
CDR

Serial Link Synchronization Problem



IDELAYE2 = 31 delay taps.
1 tap ~ 78 ps.
Compressive delay ~ 10 ns.

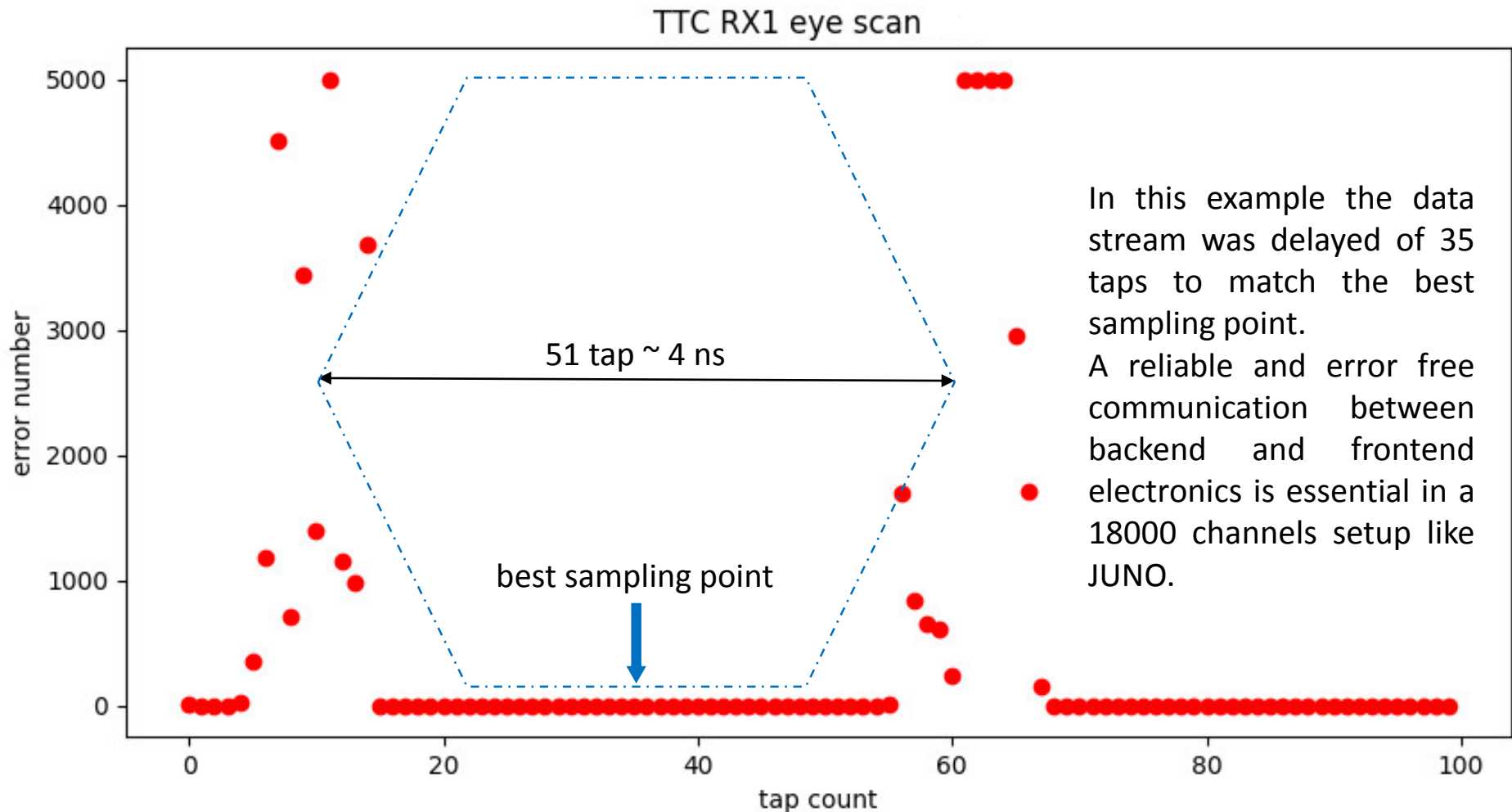


48 LVDS data streams in different phase relationship with the global clock are captured into the FPGA synchronous logic: we likely have the marginal capturing problem.

The issue has been solved using a cascade of 4 programmable delay primitives in the frontend FPGA, whose tap count is remotely incremented/decremented by the master delay control core running in the backend FPGA.

Serial Link Synchronization Solution

The data stream captured in the backend FPGA is delayed incrementally in steps of 78 ps and plotting the TTC decoder frame error count versus the tap count we get the information about the input data stream eye opening and the best sampling point.

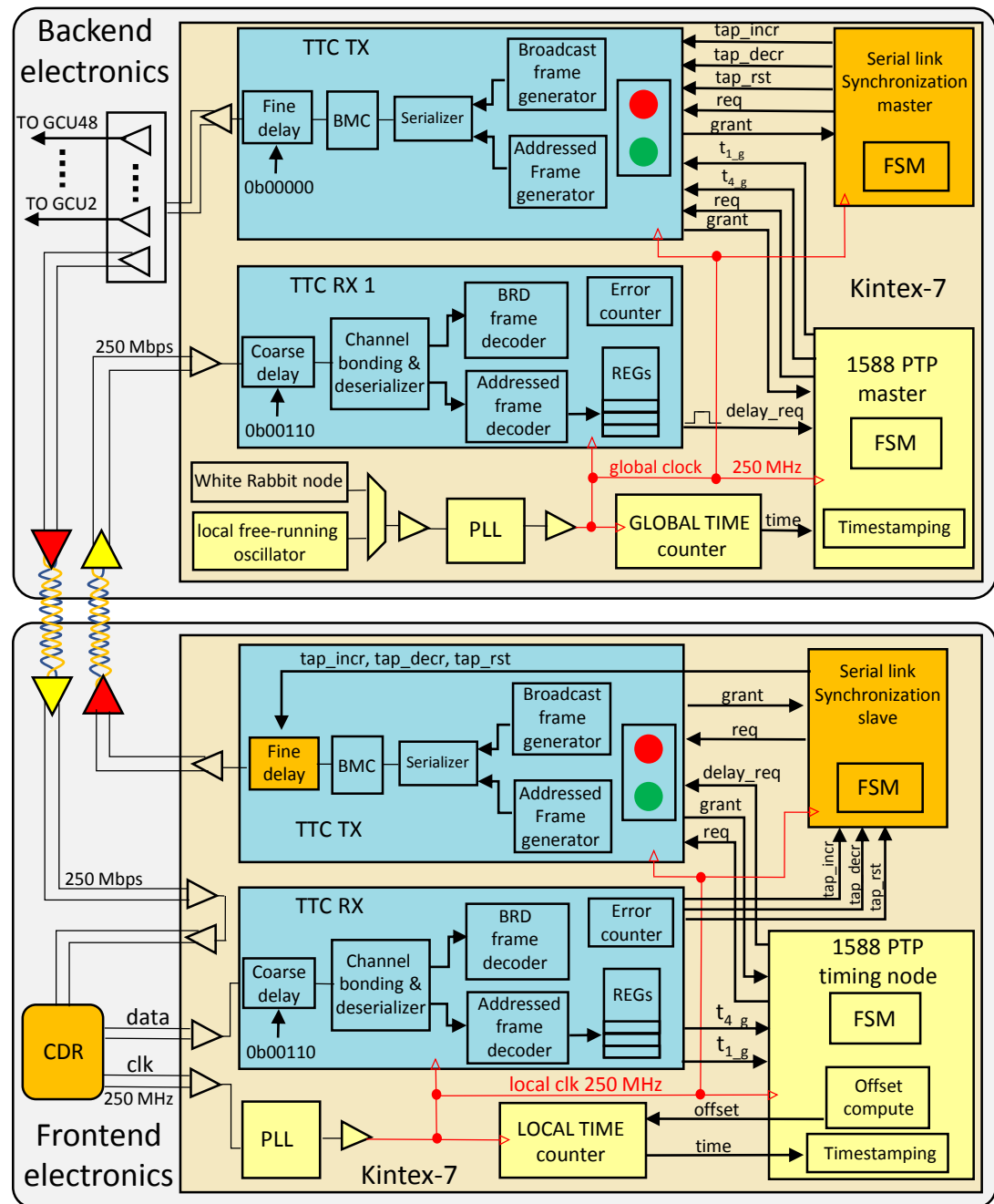


RTL Design Overview

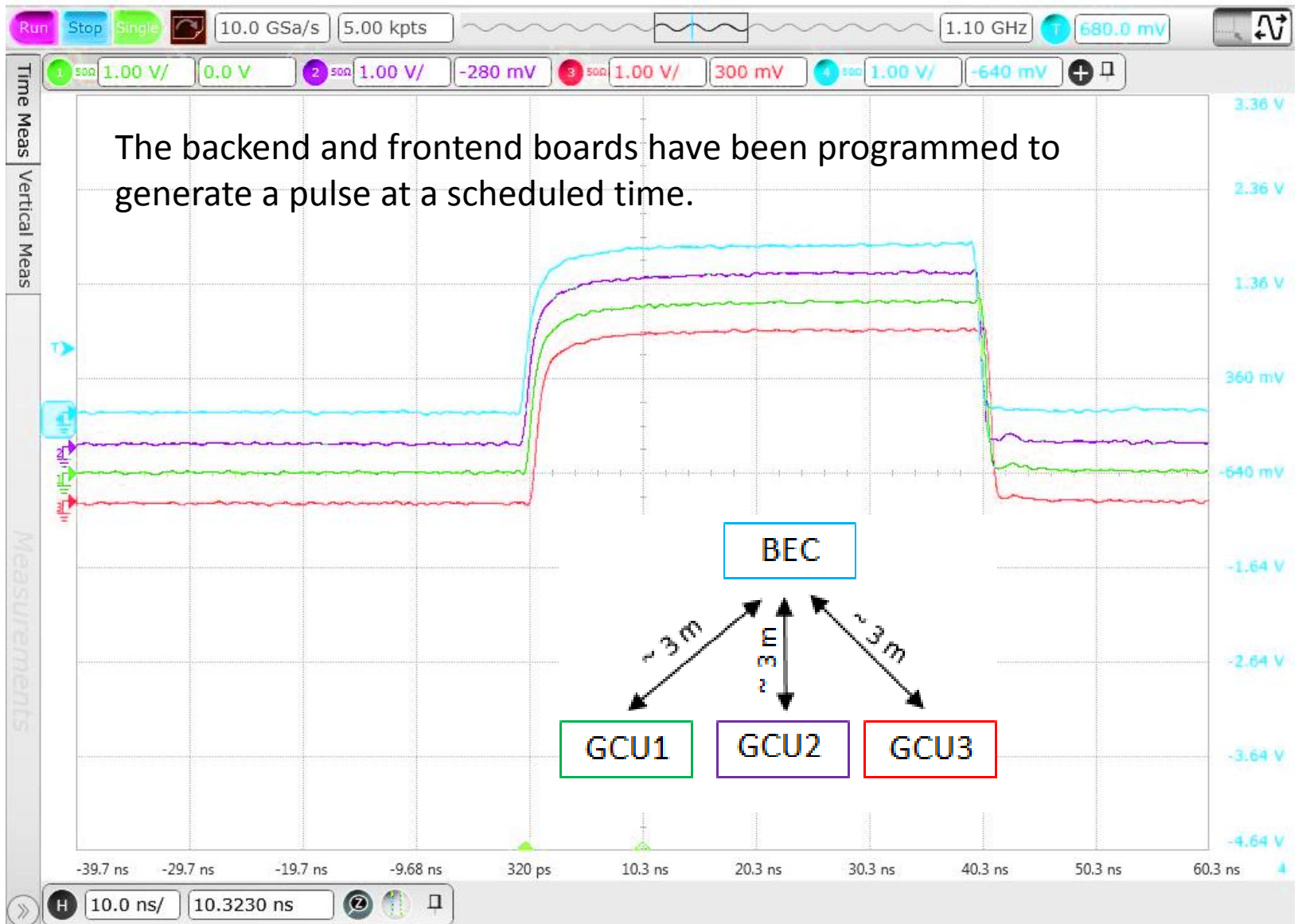
Legend:

- Syntonization and serial link synchronization
- Physical and data link layer
- Clock offset correction

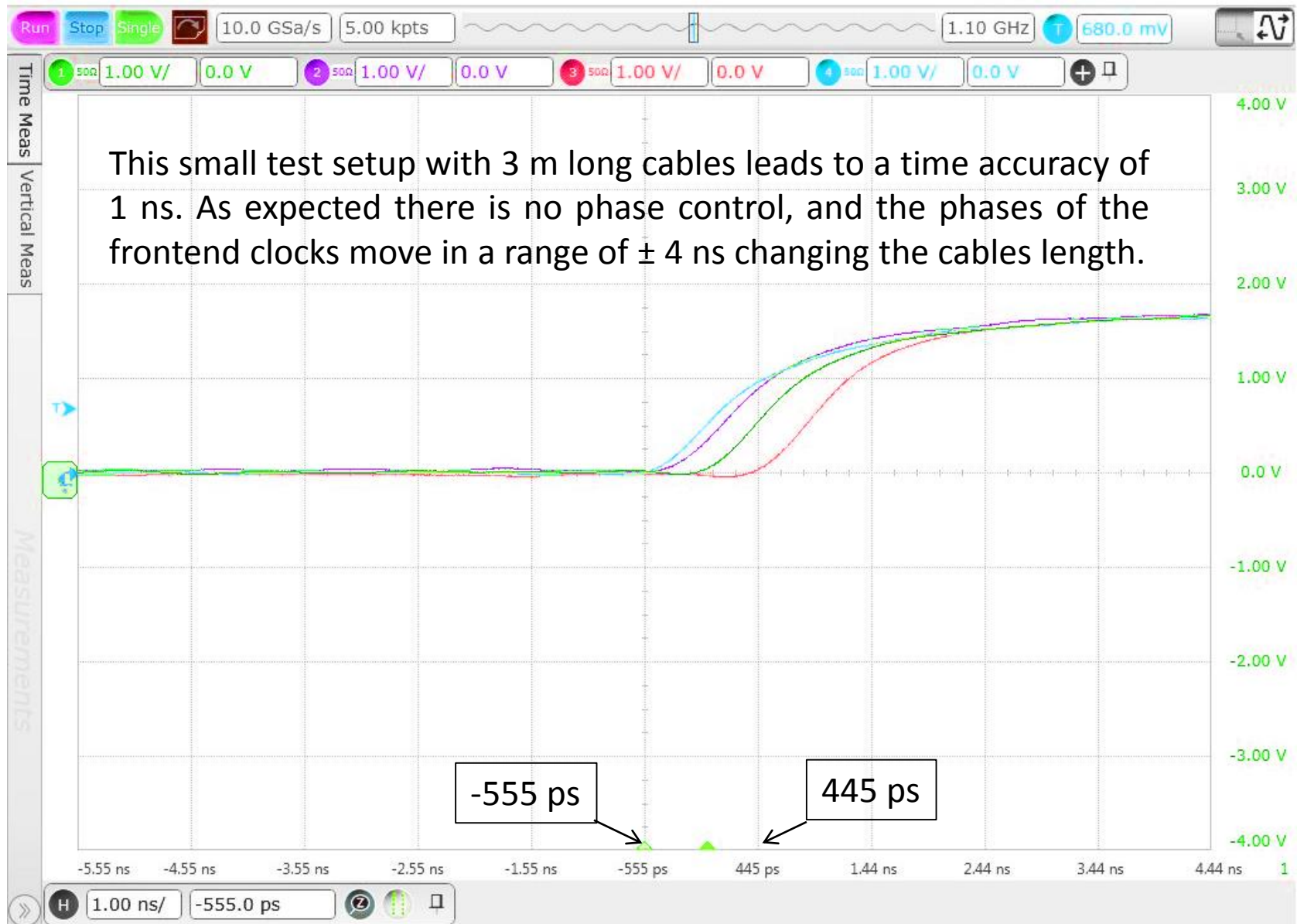
- ✓ All we need is a low cost FPGA in the backend, a low cost FPGA in the frontend and a CAT-5e cable.
- ✓ HR pins → low power and low % of FPGA resources usage.
- ✓ The VHDL code is generic, it may be easily synthesized for a different FPGA family and manufacturer.
- ✓ The PTP is conceived as a Finite State Machine (FSM).
- ✓ If a message is not delivered correctly a watchdog timer takes the FSMs back to IDLE state.
- ✓ The synchronization procedure is periodical.



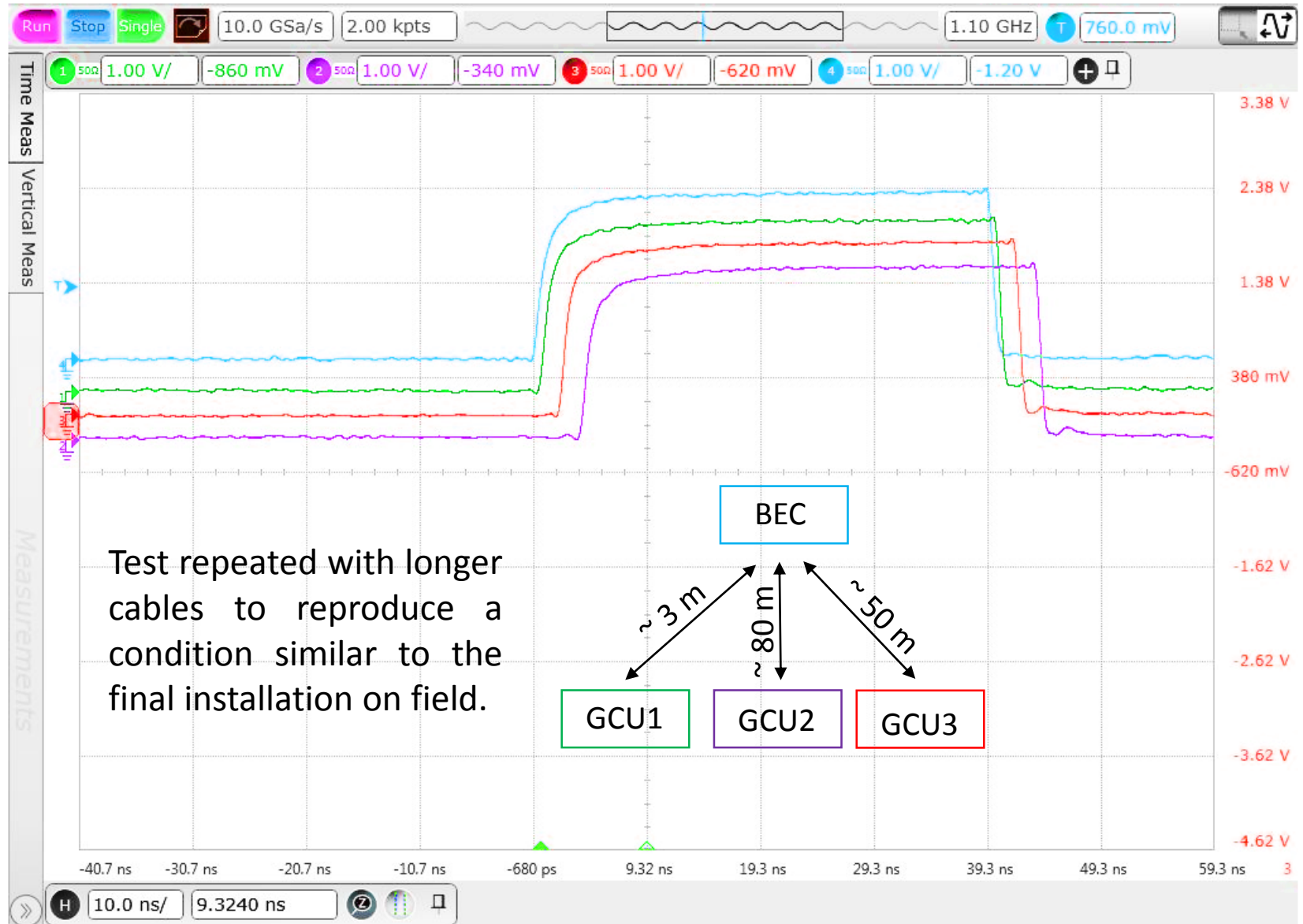
Test 1 Setup



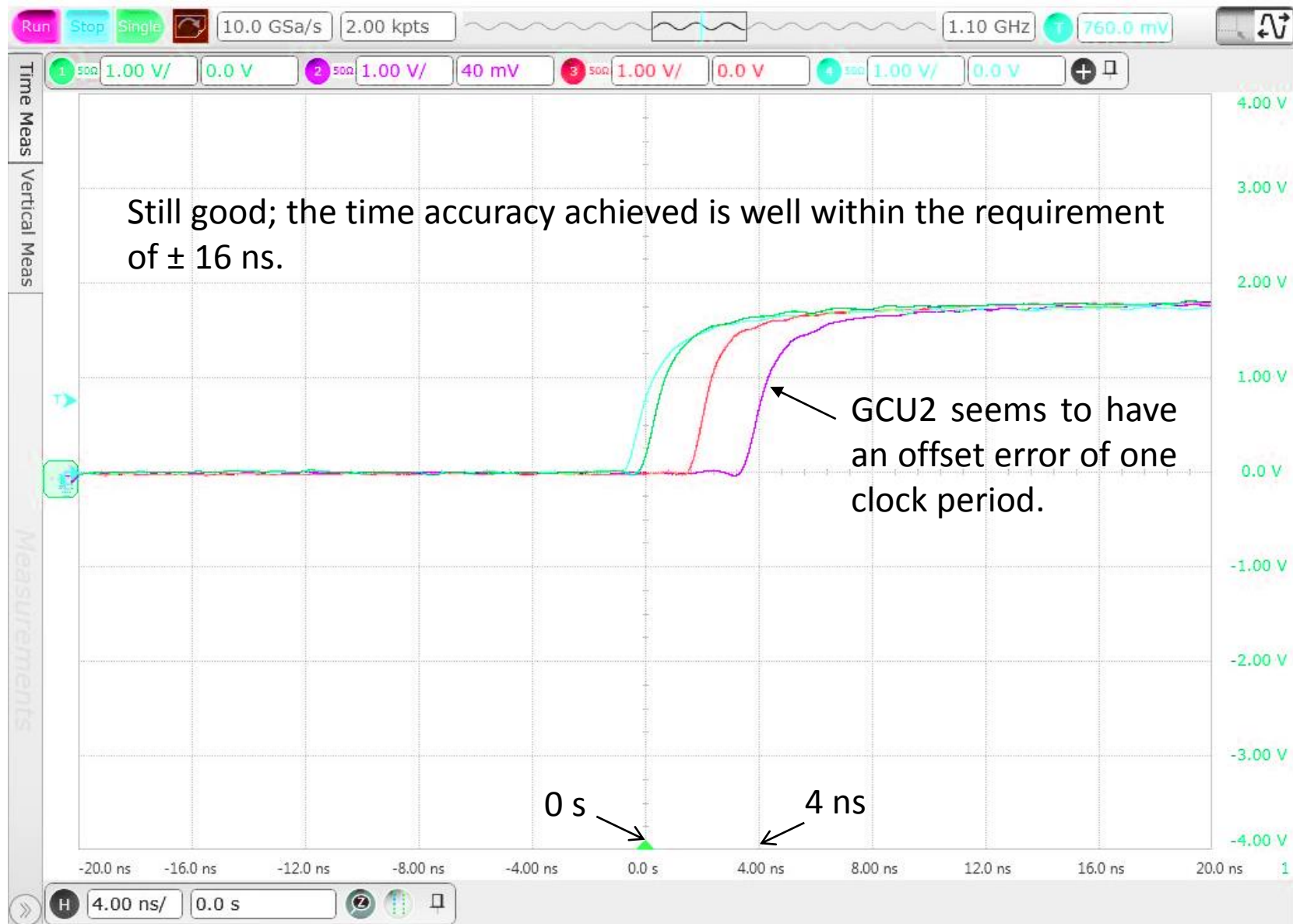
Test 1 Results



Test 2 Setup



Test 2 Results



Cable Asymmetry

	pair	propagation delay [ns]	delay skew [ns]	length [m]
CAT-5e 80 m cable	1,2	388	13	79.3
	3,6	378	3	77.3
	4,5	385	10	78.7
	7,8	375	0	76.7
	pair	propagation delay [ns]	delay skew [ns]	length [m]
CAT-5e 50 m cable	1,2	251	9	51.3
	3,6	244	2	49.9
	4,5	248	6	50.7
	7,8	242	0	49.5

This asymmetry of 10 ns generates the clock period offset error observed. Without any compensation the offset error introduced by the asymmetry of a 100 m long CAT-5e cable may be up to 25 ns.

- If the cable layout does not change after the installation, the asymmetry can be manually measured and compensated with coarse delay primitives in the firmware.
- The automatic measurement and compensation of cable length imbalance are possible only introducing in the frontend and backend electronics the hardware necessary to swap the transmit and receive differential pairs.
- The digital implementation of the PTP is compatible with a TTC optical distribution. The optical fiber asymmetry would be negligible claiming a ± 4 ns timing system.

Conclusions

The fully hardware implementation of the IEEE 1588-2008 PTP over a full duplex and deterministic latency communication channel based on the CERN TTC system enables the synchronization of thousands of timing receivers nodes with a resolution of few nanoseconds.

The proposed timing system has been developed for the JUNO experiment where the potting of underwater electronics imposes tight constraints on the communication medium between backend and frontend electronics, making commercial timing systems unattainable solutions.

The test results demonstrate that a time accuracy of ± 4 ns is achievable using two low cost FPGAs (one in the backend and one in the frontend electronics) and a communication medium, between the two FPGAs, consisting of a couple of twisted pairs in a CAT-5e cable.

The communication over copper cables is the only source of asymmetry of the implemented timing system and, if not compensated, may degrade the time accuracy.

The design is compatible with a TTC optical distribution that, outside the JUNO context, would extend the transmission range and get rid of the cable asymmetry problem.