Design of a general scientific CCD simulation and test system

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1.Introduction

With the rapid development of electronic technology, the scientific CCD detector has been widely used in many fields such as astronomy , medicine and industry due to its excellent quantum efficiency as high as 90% in visible wavelengths, ultra-low readout noise, high resolution and wide spectral response range. A scientific CCD detector system based on E2V 47-20 has been designed by us according to the observation requirements of the astronomical telescope system and the extreme low temperature as low as -80℃ of Antarctic. Therefore, it is very important to test the low-temperature-performance of the CCD controller. In order to achieve function and performance test of the scientific CCD controller, a general simulation and test system based on FPGA has been designed for the CCD controller, it can measure CCD controller including Clock-Bias Generator, ACDS circuit ,and other parameter, such as power, fan, temperature control module, crystal oscillator and shutter.

A general scientific CCD simulation and test system has been designed by us also according to the low temperature reliability, the overall structure is shown as Fig 1.

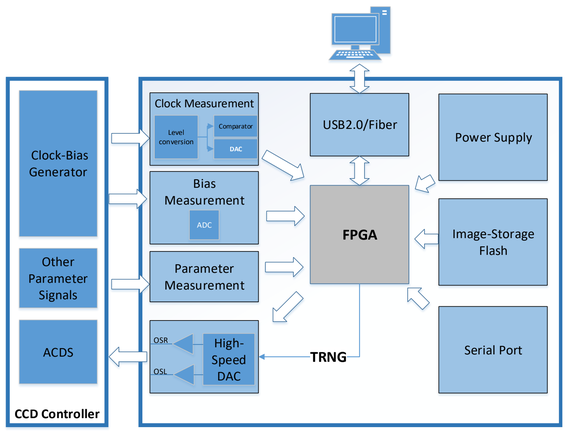

Fig 1. The Overall Structure of the system

2.System Design

The scientific CCD simulation and test system mainly includes three parts: communication module, controller parameter measurement module and video waveform simulation module.

The communication module consists of USB interface and Optical Fiber interface, communicating with the host computer in short distance or long distance condition.

The controller parameter measurement module includes the measurement of the voltage of power supply, fan speed, temperature, frequency of crystal oscillators, exposure time, parameters of CCD clocks and the voltage of CCD biases. The parameters of CCD clocks include the frequency, duty ratio, phase relation between each clock and the voltage of the high level and low level. The precision of time measurement can reach to 20 ns. The voltage measurement adopts the dichotomy to scan the high level and low level of each clock, and the precision of voltage measurement can reach to 0.5V. The advantage of the dichotomy scan level is that only one high-speed DAC is required to measure the high and low levels of the 15-channel clock, reducing the size of the simulation and test system. The biases voltage for the CCD detector are measured through successive and multiple sampling by an 18-bit ADC, and the precision can reach to 0.1V.

The video waveform simulation module consists of an arbitrary waveform generator with a high-speed DAC and high-speed TRNG, which can generate two arbitrary waveforms at the same time, simulating the right and left video channel of the CCD detector. A 500Msps DAC is used to generate the video waveform which will be output after an active filter. In order to simulate video signals with different noise, a true random number generator based on the oscillation ring in FPGA was implemented for adding random noise data to the DAC. The random number is synchronously superimposed on the DAC data so that the performance of video sampling circuit of the CCD controller could be verified fully. The system test is shown as Fig 2.

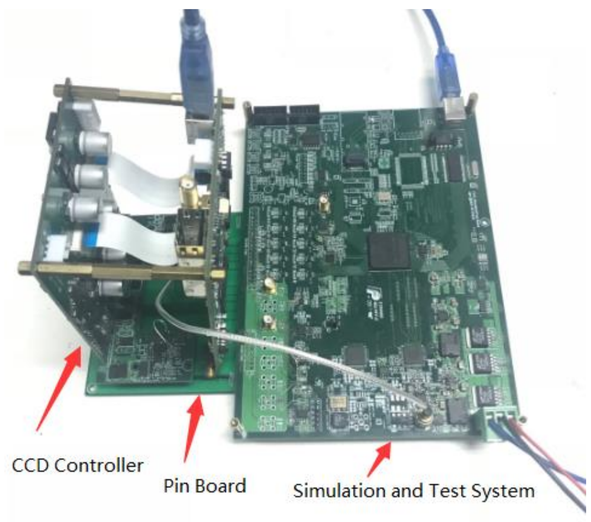

Fig 2. The Overall test picture

3.Test Result

The simulation and test system connects with the CCD controller through a plug connector. We have a made detailed test of the CCD controller with the simulation and test system. The results of the frequency, duty ratio, phase relation and the voltage of the high level and low level of the 15-channel clock are shown as Fig 3.

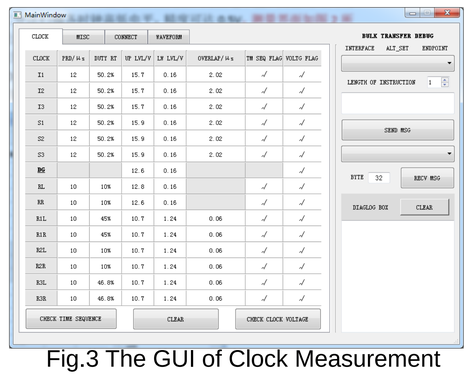

Fig.3 The GUI of Clock Measurement

And the Bias voltage value and bias voltage noise are shown as Fig 4. We can set any number of sampling points, and Quality is the noise RMS of the Bias voltage.

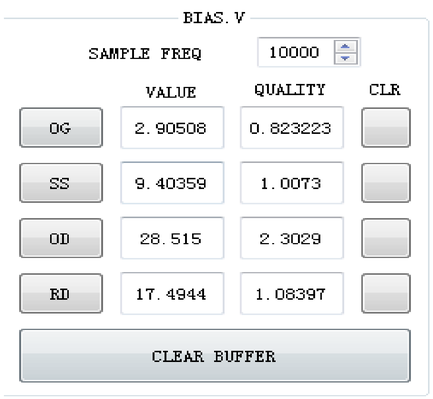

Fig.4 The GUI of Biases Voltage Measurement

4.Conclusion

The video sampling circuit of the controller includes the preamplifiers, ACDS circuit and a 18-bits ADC. The ACDS circuit mainly includes DC-recovery, two-way selection, integration and DC-offset module. After superimposing the different value of random noise, the simulated video waveform is output to the ACDS circuit and the ADC. The performance of the ACDS circuit and the ADC could be evaluated by obtaining the relationship between the added noise and the measured noise of the sampling circuit. In our test, the measured noise of the sampling circuit was about 7.3 ADUrms while no random data was superimposed on the DAC data. So when n-bit random data was superimposed on the DAC data, the theoretical noise of the measured result will be δ=√(1/6 〖（2^n-1）〗^2+〖7.3〗^2)， shown as RMS2 of Fig 5. Meanwhile, the actual noise of the measured result with n-bit random data used was shown as RMS1. We can seen that RMS1 and RMS2 could be well conformed.

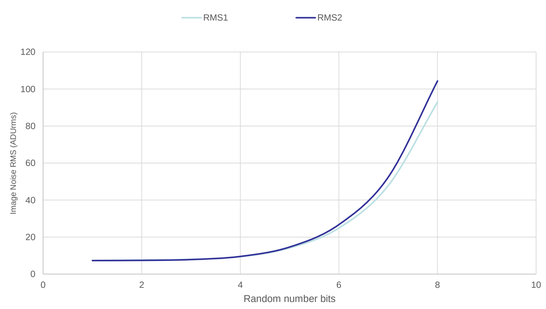

Fig 5. The Relationship between Image Noise and Random Number Bits

At present we have completed the simulation and test system. Besides, the simulation and test system has been tested for 7*24h continuous work in the 193K environment, the system kept stable work state, which shows the ability of long time working at low temperature. We have fully tested the current CCD controlled based on CCD47-20, improving the test efficiency.

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