Design of TDC ASIC based on Temperature Compensation

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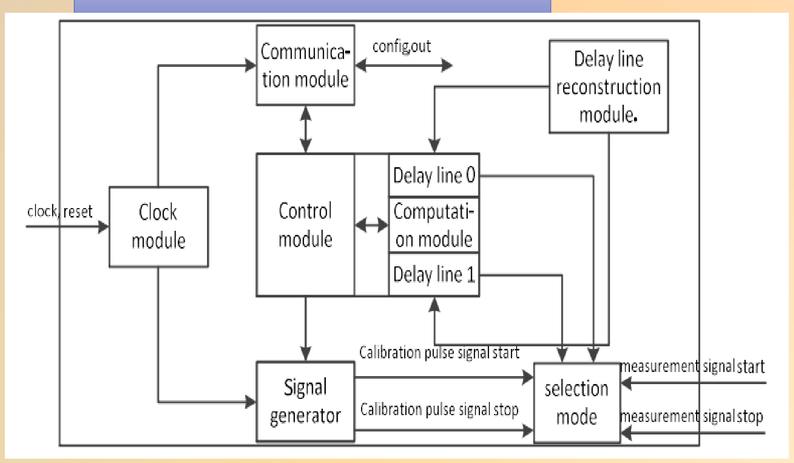
1·INTRODUCTION



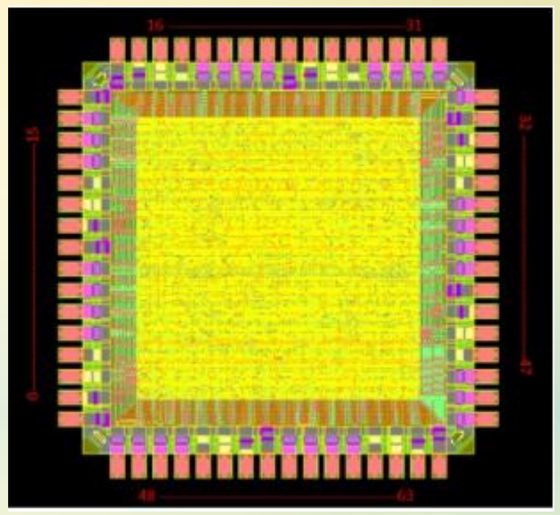
On the basis of requirement of CSNS, we designed a TDC chip with temperature compensation function in this paper, which employed TSMC 180nm process. Using delay unit bufx8 as the major method, delay lines in each level delayed input signal line through the bufx8 unit to realize fundamental measurement function. The time intervals of two fixed delay standard pulses did not change with temperature variation via intra-chip phase-locked loop. After that, the two standard pulses were sent to TDC internal delay line and measured their values. Then the measured values and standard values were compared. According to the result of comparing and decision switch, the structure of delay lines was reconstructed and their levels were recorded at the same time. We could ensure that the total length of the effective delay line were close to clock cycle as much as possible under the current temperature. The chip was tested after the completion of design. It was found that the time resolution of TDC ASIC was 73ps under 1.8V power supply at room temperature while the time resolutions were 103ps and 62ps at 85° and 0°, respectively.

2· IMPLEMENTATION

The difficulty and emphasis in the design process of the chip is the realization of delay line. The structure of TDC is shown as this. This design adopts TSMC 180nm process which bufx8 in the TSMC process is 53ps in the fastest delay and 113ps in the slowest delay after analysis, which all meeting the system's demand for time measurement. Therefore, we take the bufx8 as the main means to realize the delay, which delay cell is about 0.073ns in process corner ss (ss and ff can refer to the list process corner).
For TDC satisfying application at the request of the different temperature, the delay lines promise to be long enough to meet the total delay of one clock cycle in the fastest delay time circumstance. So the total series of the delay line is 189 and the total delay time is about 10 ns in the process corner ss.
By using the bufx8 as delay cell every level of delay line to delay the input signal line and each tap is sampled by a 100M clock. The sampling result of the delay line is output in thermometer format. Then the thermometer code is encoded by the coding module and then get the final binary delay information. The bufx8 delay in different voltage temperature is shown as Table.

Process	Voltage	temp	Delay
tt (typical)	1.8V	25	0.072259ns
ff(fast)	1.98V	0	0.053742ns
ss(slow)	1.62V	125	0.113863ns

The internal phase-locked loop chip realize two temperature-free pulse which the interval of these two pulses should be t0 (t0 only includes routing delay). The pulse as the input of the TDC internal delay line, which can obtain the measured value t1 after the delay line measurement. Compare the measured value t1 with the standard value t0, we can get the results of the comparison and according to the comparison result, combined with the judging switch the delay line structure is reconstructed and the number of delay lines series is recorded. The effective length of the delay line as close as possible in 10ns as one clock cycle with the same temperature. For example, in process corner tt, the judgment switch makes the effective delay line series a total of 136 and the series of the delay line is 136.
In process corner ff, the judgment switch makes the effective delay line series a total of 189. The delay line that series is recorded in the reconstruction output the binary data which can obtain the time easurement results after update according to the time delay line series in the reconstruction. Although small change taking in minimum resolution of new delay line, delay line measurement results did not change with the temperature in the test of the reconstructed delay line.



Area	1643 mm X 1501mm
Static Power	2.033e-06 W@100MHz
dynamic power	0.1454+0.0269 = 0.1723W@100Mhz
Total Power	0.1722W@100Mhz

3· PRELIMINARY RESULT

The satisfactory result is achieved with measuring a fixed intervals pulse under different temperatures. The test result at different temperatures is shown as this:

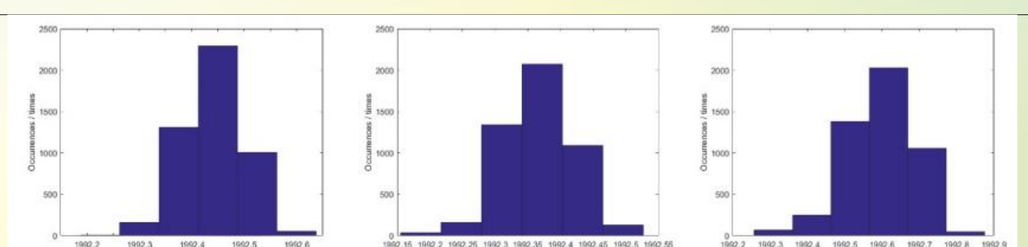


Fig.4-1 The test results in 25℃ Fig.4-2 The test results in 0℃ Fig.4-1 The test results in 85℃