A readout method based on 10 Gigabit Ethernet for Sipixel detector

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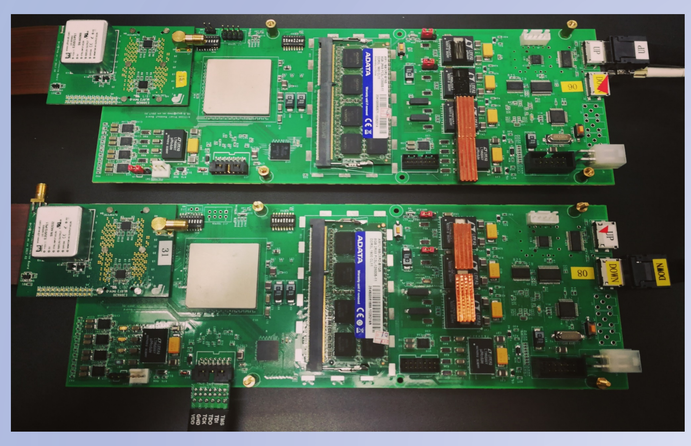
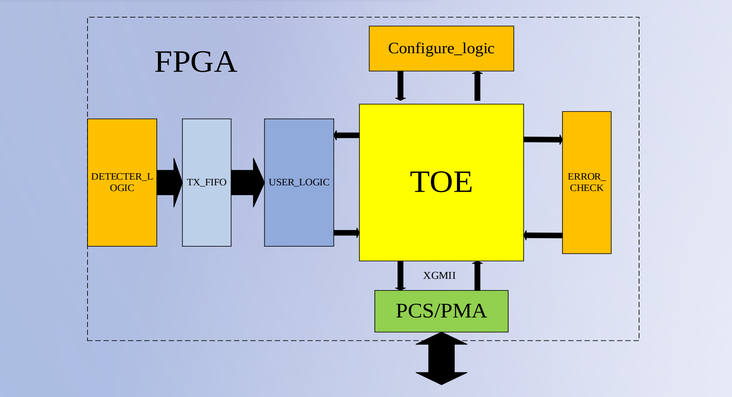
1. INTRODUCTION



HEPS-BPIX readout board

HEPS is a read-out electronics system based on the BPIX pixel array detector readout chip which is independently designed and developed by the institute of high energy physics. The read-out electronics system uses Field-Programmable Gate Array (FPGA) as the core of digital logic. In order to complete the basic function of the pixel detector, the read-out system need to be set up the configuration and read out data chain of the BPIX readout chip. The prototype of the detector consists of 16 sensor modules, covering an effective detection area of 17.28 cm * 12.48 cm. The detection energy interval is 8 keV -20 keV.

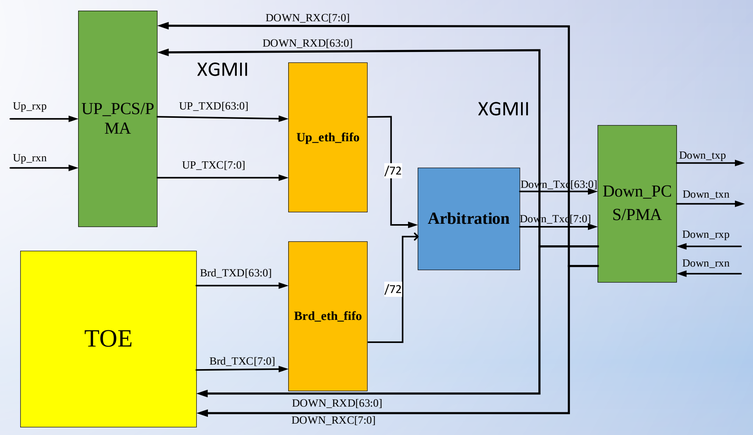
2. IMPLEMENTATION

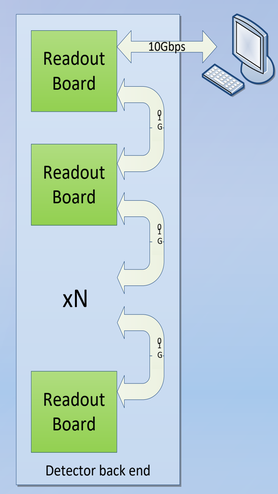


Simple block diagram of the FPGA firmware.

The firmware is mainly divided into two parts, one is the TCP data processing module and the other is the UDP data parsing module. The way of TCP/UDP data transmission between XTOE and user layer is strictly adhered to the timing relationship required by XTOE IP core.

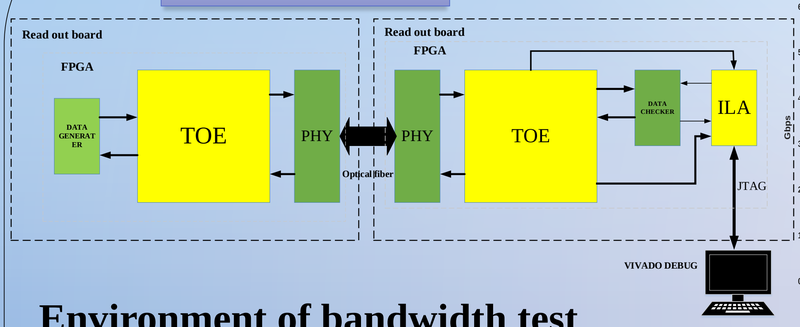
For sipixel detector, The parameters of the BPIX pixel array chip and the setting of the trigger signal require to be configured through the UDP protocol. A kind of timing is adopted to read and write internal registers. The UDP logic module parses the data and translates packets into the address and data, which is provided to read and write the corresponding register. To reduce the complexity of the interface and the connection cables, the firmware utilize the connection mode of the daisy chain. It can not only to process the TCP packets from the read-out board, but also the data from the upstream readout board. The upstream data are connected through NANO_PITCH. Consequently, both the upstream and the downstream data are processed simultaneously by arbitration module. Therefore multiple boards can share the same bandwidth.



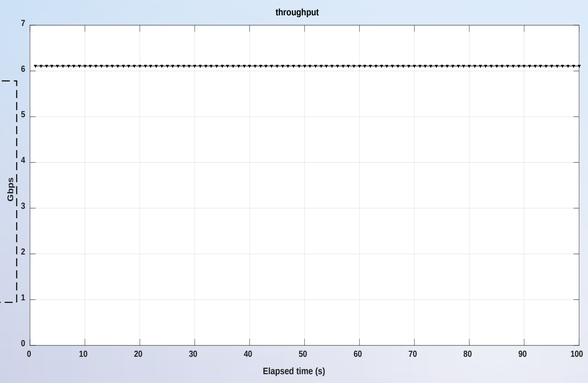


The structure of the upper-computer software.

3. RESULTS



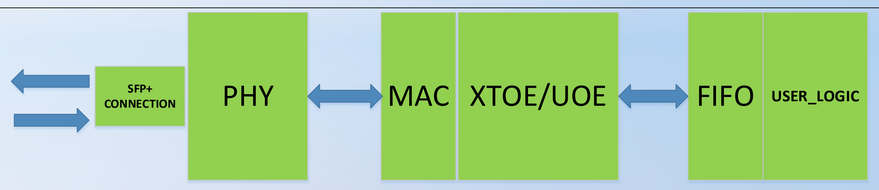
Environment of bandwidth test

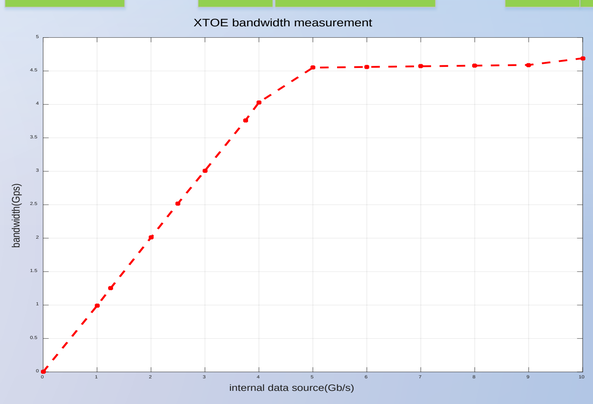


The result of Test maximum throughput between 100 seconds

Two boards are connected each other through the SFP module. Vivado debugger sample the registers'counts which are calculated by internal logic block and save the data as CSV format, then get the maximum bandwidth by MATLAB.

The UDP parsing module through Netcat to verify whether the firmware can read or write internally defined registers.
The experiment uses FPGA as data sources to generate data of different throughput and matches FIFO to test the linearity of the bandwidth.





The source from 0 to 10Gbps are generated via two clock (125MHz 156.25mhz) and different bit width data. At the same time ,IPERF measure the bandwidth as the server port.

This readout method has been partially verified and implemented, which can be configured and real-time transfer data through XTOE. Meanwhile, the firmware can readout data from multiple boards by the daisy chain mode.