The Electronics Design of Error Field Feedback Control System in KTX

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1. Introduction

KTX (Keda Tours eXperiment) is a new RFP (reversed field pinch) device at the University of Science and Technology of China. In this article a feedback control system to solve the error field problem is presented. It is extremely important to build up a feedback system for this new fusion device. The main part of the system is two different boards with their independent function modules. Sample module is used to acquire and to manipulate the data from Rogowski coils around the vertical gap. Coil control module gets the data from sample module and gives a feedback signal to the active error field control power amplifier.

2. The installation position of system

The vacuum vessel and the conducting shell in KTX device are mounted on a movable platform. This structure, called 'double-C', allows the machine to be opened easily without dissembling the poloidal field windings around.

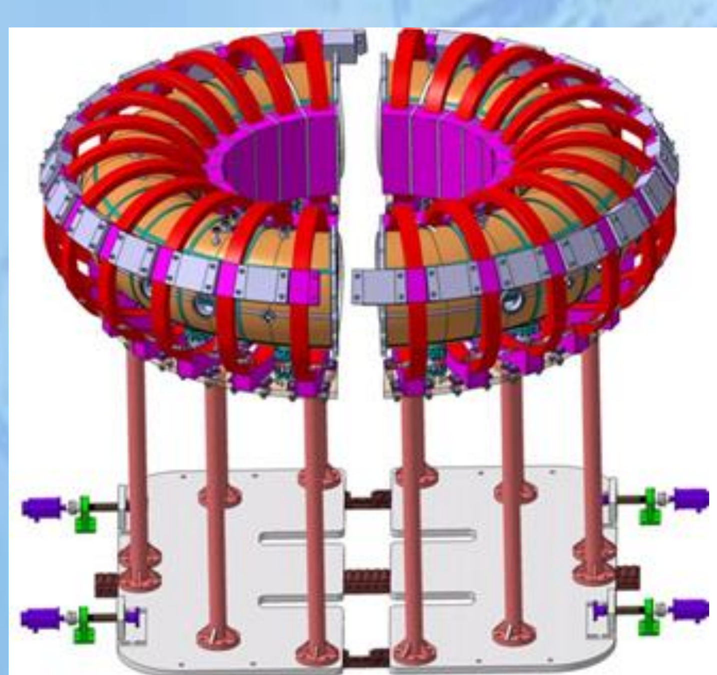

Fig. 1 double-C design

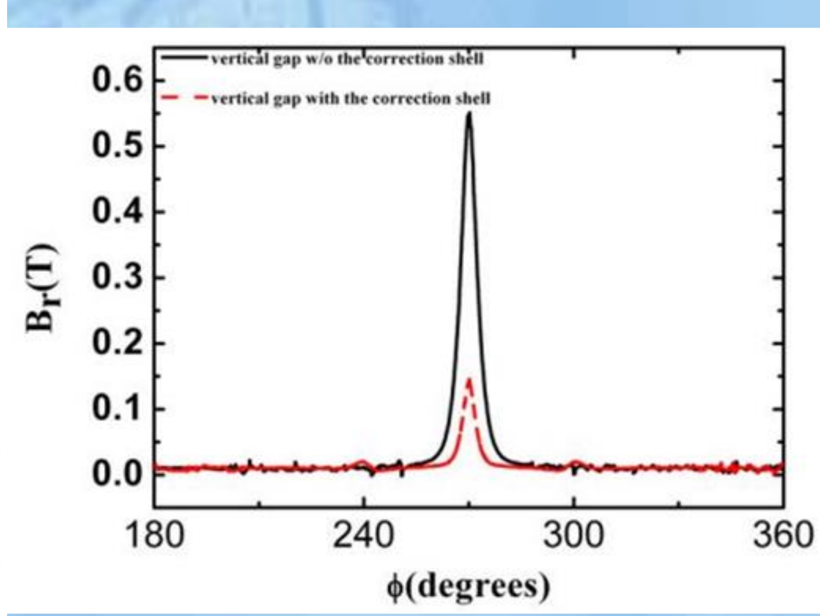

Fig. 2 simulation of error field

However, the vertical error field which may deform the shape of equilibrium surface and cause disruption and mode lock will be the more critical interference due to this structure. According to the simulation, the error field of the vertical gap may lead to around one degree declination of signal-to-noise ratio, which cannot be tolerated..

3. Control method

The mutual inductance between two coils should not be ignored. The mutual inductance function is:

$$\overleftrightarrow{U_{OUT}} = v\overleftrightarrow{M}\cdot(\overleftrightarrow{U_{IN}}\cdot\beta_R+\alpha_0)$$

U_{OUT} , U_{IN} are the voltage of the input and output. And v is the reciprocal of amplification factor of the power amplifier.
α_0 *and* β_R.are adjustable parameters. $\overleftrightarrow{M}$ is the mutual inductance matrix, which is measured:

$$M=\begin{pmatrix} 620 & -7 & -1.67 & 0 & \cdots & 0 & -1.67 & -7 \\ -7 & 620 & -7 & -1.67 & \ldots & 0 & 0 & -1.67 \\ -1.67 & -7 & 620 & -7 & \cdots & 0 & 0 & 0 \\ 0 & -1.67 & -7 & 620 & \cdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 620 & -7 & -1.67 \\ -1.67 & 0 & 0 & 0 & \cdots & -7 & 620 & -7 \\ -7 & -1.67 & 0 & 0 & \cdots & -1.67 & -7 & 620 \end{pmatrix}\mu H$$

A PID (proportional–integral–derivative) controller is a loop feedback mechanism widely used in industrial control systems and a variety of other applications.
The typical function of PID controller is:

$$u(t) = K_P e(t) + K_i\int_0^t e(\tau)\,d\tau + K_d\frac{de(t)}{dt}$$

The discrete implement function is:

$$u(t_k) = u(t_{k-1}) + K_P\left[\left(1+\frac{\triangle t}{T_i}+\frac{T_d}{\triangle t}\right)e(t_k)+\left(-1-\frac{2T_d}{\triangle t}\right)e(t_{k-1})+\frac{T_d}{\triangle t}e(t_{k-2})\right]$$

$$T_I = K_p/K_I,\ T_d = K_d/K_p, \triangle t \text{ is the sample period}$$

4. Architecture of system

The system is composed of two different modules: the sample module and the coil control module. Sample module is used to acquire and to manipulate the data from Rogowski coils around the gap. Coil control module gets the data from sample module and gives a feedback signal to the active error field control power supply

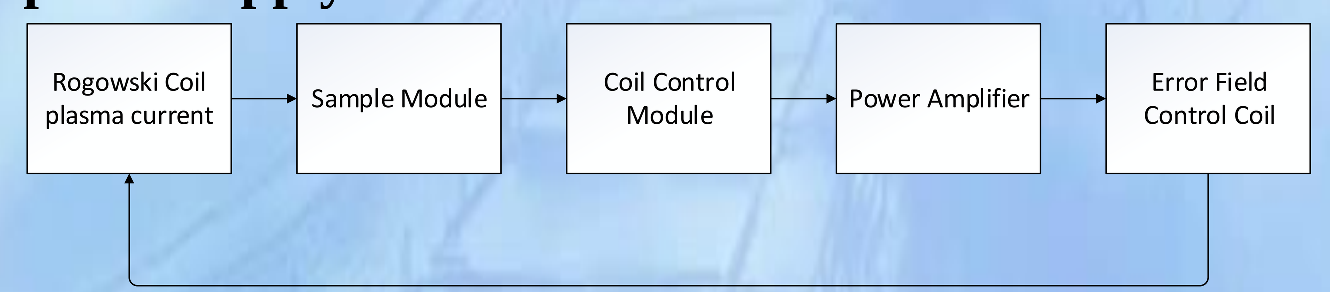

Fig. 3 Hardware architecture of system

16 rogowski coils send a bipolar analog signal to the sample module. After a two-step amplification, the signal is digitalized by ADC. FPGA catches the data from it, and do the calculation synchronously. Then the FPGA sends the data to the coil control module through RS485. DDR2 and network are back-up.

FPGA in the coil control module gets data from RS485 interface, and divide data into 16 parts to control correspond power amplifier.

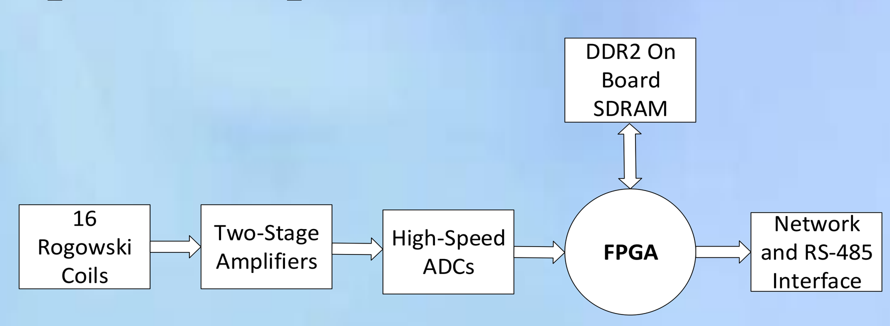

Fig. 4 the structure of sample module

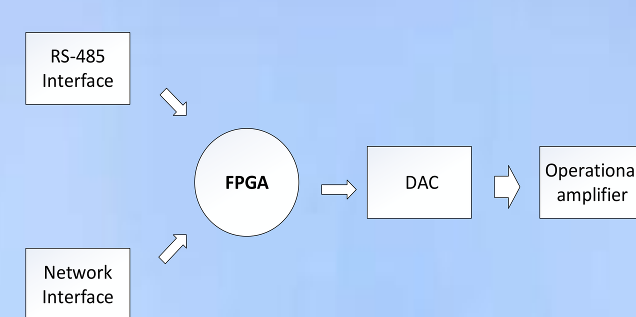

Fig. 5 the structure of coil control module

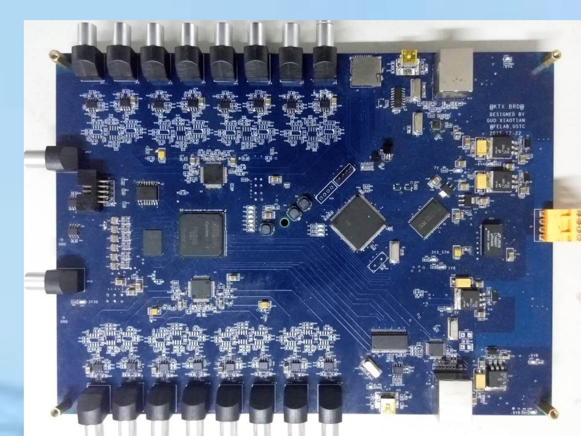

Fig. 6 sample module board

Fig. 7 coil control board

5. Results

Figure 8 shows the result of DAC, ADC and RS485 on SignalTap II. It indicates that the system can get the signal from the Rogovski coils and send the feedback normally

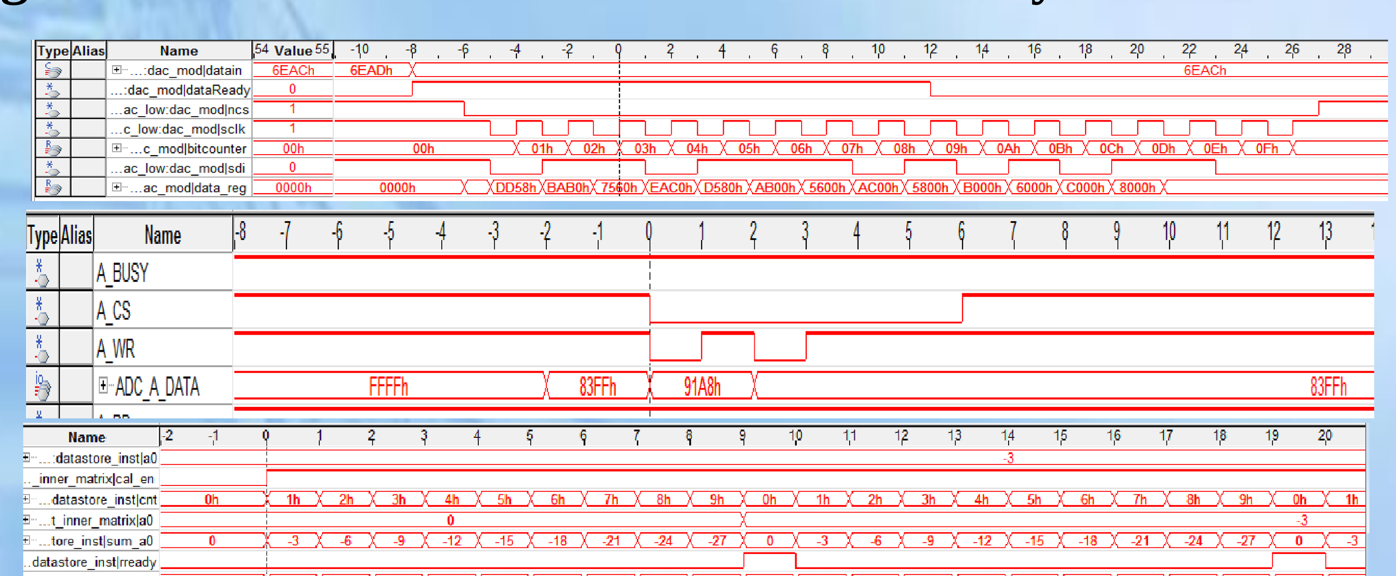

Fig. 6 DAC、ADC、RS485 results with Signal Tap II.

6. Conclusion

This work focus on designing a feedback system to reduce the error field of vertical gap. FPGA is the core component of the whole system. It control the whole process and calculation in a low latency, which makes the error field descend.