General purpose readout board πLUP: overview and results.

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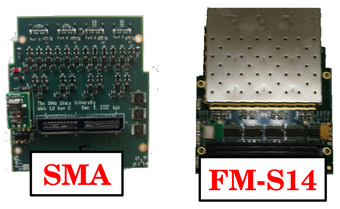
Abstract

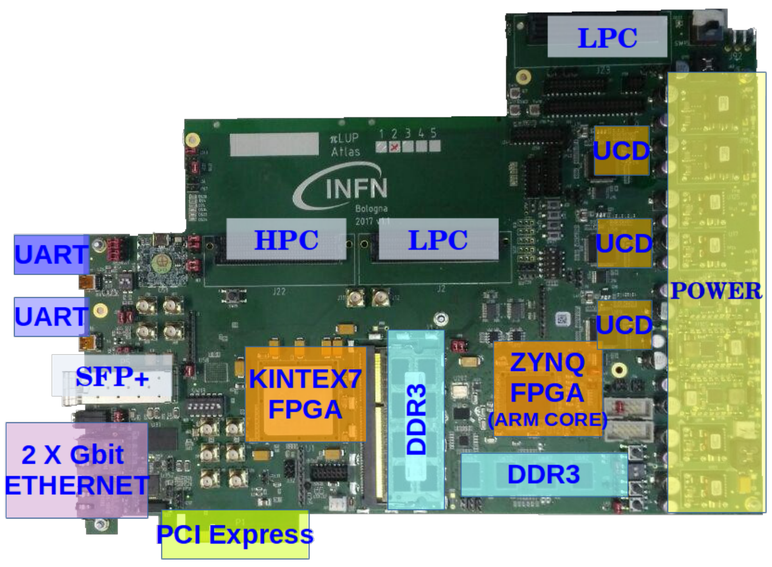
This work gives an overview of the PCI-Express board πLUP, focusing on the motivation that led to its development, the technological choices adopted and its performance. The πLUP card was designed by INFN and University of Bologna as a possible readout interface to be used after the upgrade of the Pixel Detector of the ATLAS and CMS experiments at LHC. The same team in Bologna also designed and commissioned the ReadOut Driver (ROD) board - currently implemented in all the four layers of the ATLAS Pixel Detector (Insertable B-Layer, B-Layer, Layer-1 and Layer-2) - and acquired in the past years expertise on the ATLAS readout chain and the problematics arising in such experiments. Although the πLUP was designed to fulfill a specific task, it is highly versatile and might fit a variety of applications, some of which will be discussed in this work. Two 7th-generation Xilinx FPGAs are mounted on the board: a Zynq-7 with an embedded dual core ARM Processor and a Kintex-7. The latter features sixteen 12.5 Gbps transceivers, allowing the board to interface easily to any other electronic board, electrically and/or optically, at the current desired bandwidth of the experiments for LHC. Many data-transmission protocols have been tested at different speed. Two batches of πLUP boards have been fabricated and tested; two boards in the first batch (version 1.0) and four boards in the second batch (version 1.1), encapsulating all the patches required for the first version.

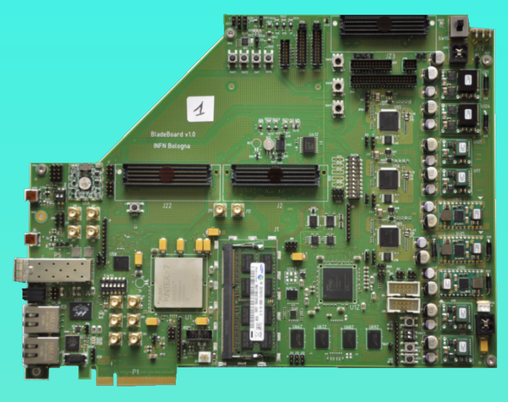
πLUP: READOUT BOARD PROPOSAL

- The Bologna **πLUP card** is a 16 layers PCI Express board capable of interfacing to several different other boards or front-ends and processing data at high speed. Main components:
- 7-series **Xilinx®** FPGAs
  - ✔ **Kintex®7** XC7K325T for trigger and data processing
  - ✔ **Zynq® Z020** with physical dual-core ARM Cortex-A9
- 1 x **PCIe Express** interface (**4GB/s** towards the PC memory)
- 16 x **GTX@ 10Gb/s**
  - ✔ 8 x PCIe connector
  - ✔ 1 x SFP+ connector
  - ✔ 1 x SMA connector
  - ✔ 4 x HPC FMC connector
  - ✔ 1 x LPC FMC connector
- 1 x **HPC** (400-pin) FMC
- 2 x **LPC** (160-pin) FMC
- DDR3 2x667 MHz
- ARM Dual-Core A9
- 16 layers – stackup

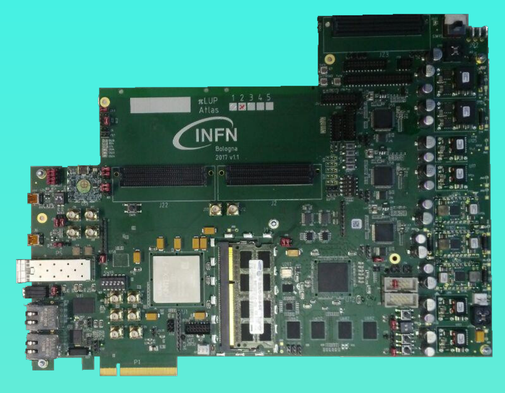
Different commercial **FMC mezzanines** can be plugged to the board







Version 1.0
(2 boards produced)



Version 1.1
(4 boards produced)

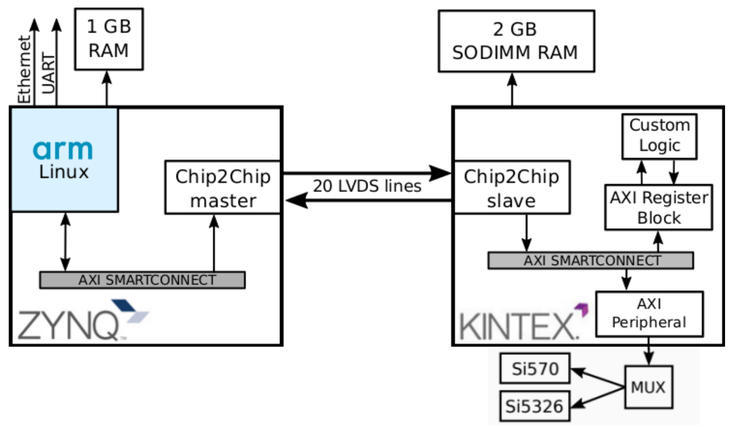
πLUP applications

The main applications for the πLUP board are:

- **Readout control system:** front-end interface, online data processing, histogramming and data transfer via PCIe bus. Max bandwidth: **4 GB/s** (8 lanes PCIe gen 2 max speed) or **7.9 GB/s** (8 lanes PCIe gen 3 max speed)
- **Data generator/ front-end emulator**. Max bandwidth: **10 GB/s** (8x10Gbps transceivers)
- **Bridge** between two different systems: connection between two different readout systems that use different protocols or different communication physical layers.

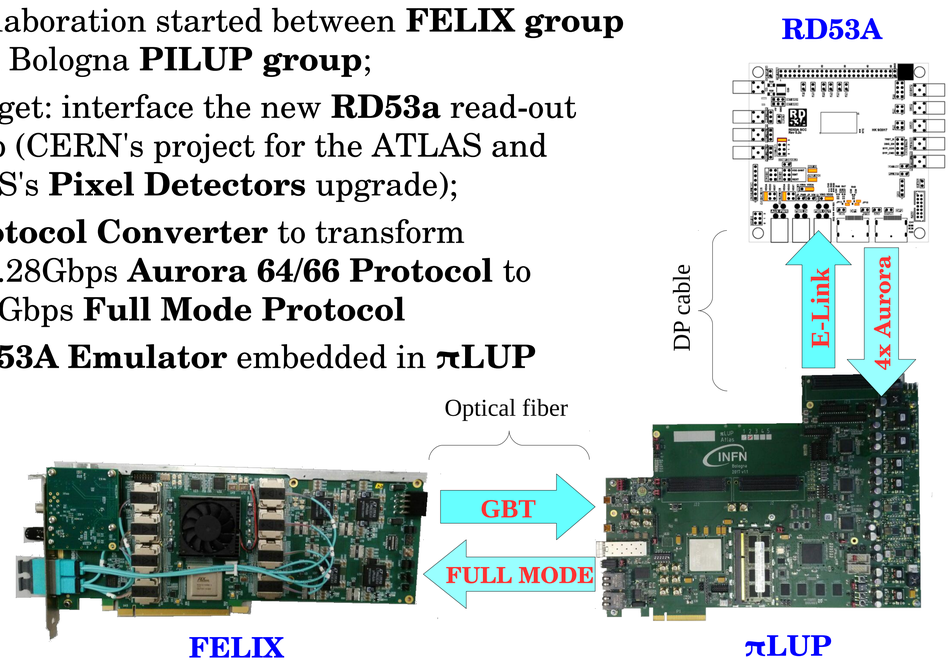
Software Architecture

- **Master** (ZYNQ) / **Slave** (KINTEX) architecture
- **Chip2Chip** to extend AXI bus to the Kintex.
- Any application without an AXI interface is controlled with a register block directly mapped on the AXI bus.
- **Petalinux** kernel on ARM core



πLUP application: Protocol Converter

- Collaboration started between **FELIX group** and Bologna **PILUP group**;
- Target: interface the new **RD53a** read-out chip (CERN's project for the ATLAS and CMS's **Pixel Detectors** upgrade);
- **Protocol Converter** to transform 4x1.28Gbps **Aurora 64/66 Protocol** to 9.6 Gbps **Full Mode Protocol**
- **RD53A Emulator** embedded in **πLUP**



πLUP Results

- All **16 GTx transceivers** tested
- Several **Protocols** Tested:
  - **GBT** (4.8 Gbps)
  - **Full Mode** (9.6 Gbps)
  - **Aurora 64b/66b** (4x 1.28 Gbps, 1x 5.12)
  - **Ethernet** 10 Gbps
- **PCI Express** tested
  - **Gen 2**: max user payload: 3.1 GB/s
  - **Gen 3**: under development

I/O Connector	Open Area (5 Gbps)	Open Area (10 Gbps)
HPC FMC MGT 0	11952	2784
HPC FMC MGT 1	9008	2272
HPC FMC MGT 2	10480	2512
HPC FMC MGT 3	11280	2480
SFP+	10432	2320
SMA MGT	6704	512

OPEN AREA RESULTS
RUN AT **5/10 Gbps**
PRBS **31-BIT** AND **BERR** 10^{-9}

XILINX IBERT TEST (loobpack)

EYE DIAGRAMS
(**10 Gbps**
PRBS **31-BIT** AND BER 10^{-9})