**General purpose readout board πLUP: overview and results.**

Nico Giangiacomi1,2, Fabrizio Alfonsi1,2, Gabriele d’Amore1,2, Gabriele Balbi3, Davide Falchieri1, Alessandro Gabrielli1, Giuseppe Gebbia1, Giuliano Pellegrini3, Davide Severini1,2

1 Speaker, 2 University of Bologna, 3 INFN Bologna, nico.giangiacomi@bo.infn.it

**Abstract**

This work gives an overview of the PCI-Express board πLUP, focusing on the motivation that led to its development, the technological choices adopted and its performance. The πLUP card was designed by INFN and University of Bologna as a possible readout interface to be used after the upgrade of the Pixel Detector of the ATLAS and CMS experiments at LHC. The same team in Bologna also designed and commissioned the ReadOut Driver (ROD) board - currently implemented in all the four layers of the ATLAS Pixel Detector (Insertable B-Layer, B-Layer, Layer-1 and Layer-2) - and acquired in the past years expertise on the ATLAS readout chain and the problematics arising in such experiments. Although the πLUP was designed to fulfill a specific task, it is highly versatile and might fit a variety of applications.

**πLUP: READOUT BOARD PROPOSAL**

- The Bologna πLUP card is a 16 layers PCI Express board capable of interfacing to several different other boards or front-ends and processing data at high speed. Main components:
  - 7-series Xilinx® FPGAs
  - Kintex®7 XC7K325T for trigger and data processing
  - Zynq® Z7000 with physical dual-core ARM Cortex-A9
  - 1 x PCIe Express interface (4GB/s towards the PC memory)
  - 16 x GTX8x 10Gb/s
    - 8 x PCIe connector
    - 1 x SFP+ connector
    - 1 x SMA connector
    - 4 x HPC FMC connector
    - 1 x LPC FMC connector
  - 1 x HPC (400-pin) FMC
  - 2 x LPC (160-pin) FMC
  - DDR3 2x667 MHz
  - ARM Dual-Core A9
  - 16 layers – stackup

**Software Architecture**

- **Master** (ZYNO) / **Slave** (KINTEX) architecture
- Chip2Chip to extend AXI to the Kintex
- Any application without an AXI interface is controlled with a register block directly mapped on the AXI bus.
- **Petalinux** kernel on ARM core

**πLUP Results**

- All 16 GTx transceivers tested
- Several Protocols Tested:
  - GBT 4.8 Gbps
  - Full Mode 9.6 Gbps
  - Aurora 64/66b 9.6 Gbps
  - Ethernet 10 Gbps
- PCI Express tested
  - Gen 2: max user payload: 3.1 GB/s
  - Gen 3: under development

<table>
<thead>
<tr>
<th>I/O Connector</th>
<th>Open Area (5 Gbps)</th>
<th>Open Area (10 Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HPC FMC MGT 0</td>
<td>11052</td>
<td>2784</td>
</tr>
<tr>
<td>HPC FMC MGT 1</td>
<td>9008</td>
<td>2272</td>
</tr>
<tr>
<td>HPC FMC MGT 2</td>
<td>10480</td>
<td>2512</td>
</tr>
<tr>
<td>HPC FMC MGT 3</td>
<td>11260</td>
<td>2480</td>
</tr>
<tr>
<td>SFP+</td>
<td>10432</td>
<td>2320</td>
</tr>
<tr>
<td>SMA MGT</td>
<td>6704</td>
<td>512</td>
</tr>
</tbody>
</table>

**πLUP application: Protocol Converter**

- Collaboration started between FELIX group and Bologna PILUP group;
- Target: interface the new RD53a read-out chip (CERN’s project for the ATLAS and CMS’s Pixel Detectors upgrade);
- Protocol Converter to transform 4x2.5Gb/s Avalanche 64/66 Protocol to 9.6 Gbps Full Mode Protocol
- RD53A Emulator embedded in πLUP

**πLUP applications**

The main applications for the πLUP board are:

- **Readout control system**: front-end interface, online data processing, histogramming and data transfer via PCIe bus. Max bandwidth: 4 GB/s (8 lanes PCIe gen 2 max speed) or 7.9 GB/s (8 lanes PCIe gen 3 max speed)
- **Data generator/ front-end emulator**: Max bandwidth: 10 GB/s (8x10Gbps transceivers)
- **Bridge** between two different systems: connection between two different readout systems that use different protocols or different communication physical layers.