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General purpose readout board π LUP: overview and results.

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This work intends to give an overview of the PCI-Express board π LUP, focusing on the motivation that led to its development, the technological choices adopted and its performance. The π LUP card was designed by INFN and University of Bologna as a possible readout interface to be used after the upgrade of the Pixel Detector of the experiments ATLAS or CMS at LHC. The same team in Bologna also designed and commissioned the ReadOut Driver (ROD) board currently implemented in all the four layers of the ATLAS Pixel Detector (Insertable B-Layer, B-Layer, Layer-1 and Layer-2) and acquired in the past years expertise on the ATLAS readout chain and the problematics arising in such experiments.

Although the π LUP was designed to fulfill a specific task, it is highly versatile and might fit a variety of applications, some of which will be discussed in this work. Two 7th-generation Xilinx FPGAs are mounted on the board: a Zynq-7 with an embedded dual core ARM Processor and a Kintex-7. The latter features sixteen 12.5 Gbps transceivers, allowing the board to interface easily to any other electronic board, electrically and/or optically, at the current desired bandwidth of the experiments for LHC. Many data-transmission protocols have been tested at different speeds; results will be discussed later in the work.

Two batches of π LUP boards have been fabricated and tested; two boards in the first batch (version 1.0) and four boards in the second batch (version 1.1), encapsulating all the patches required for the first version.

Description

PICe π LUP

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