Contribution ID: **398** Type: **Poster presentation**

The Readout Supervisor firmware for controlling the upgraded LHCb detector and readout system.

Thursday, June 14, 2018 3:50 PM (1 minute)

In 2019, the LHCb experiment at CERN will undergo a major upgrade where its detector electronics and the entire readout system will be replaced. The goal is to read-out all events at the full LHC frequency of 40 MHz, reaching a total data rate of ~40 Tb/s. In this context, a new timing, trigger and readout control system has been developed: its main tasks are to distribute centrally the clock, the timing information and to synchronize all elements in the readout system: from the very last Front-End ASIC to the building of events to be stored. The heart of the timing and readout control system is a VHDL firmware core that is now finalized and currently in use in test-benches and test-beams by the upgraded sub-detectors, for their initial commissioning phase. Such firmware core is able to generate all necessary processes to keep the synchronization of all readout elements with the LHC bunch crossing as well as it is able to generate asynchronous commands for calibration or test purposes. It is also able to accommodate for specific recipes to handle varying running conditions, by using a generic and fully configurable approach. In this paper, the philosophy and the implementation behind such firmware are described in details, posing particular emphasis to the real-time logical processes that were developed in order to satisfy the requirements of synchronization and readout control of the upgraded LHCb detector.

Description

trigger, data throughput

Institute

CERN

Speaker

Federico Alessio

Country

Switzerland

Minioral

Yes

Primary author: ALESSIO, Federico (CERN)

Presenter: ALESSIO, Federico (CERN)

Session Classification: Poster 2

Track Classification: Data Acquisition