µTCA DAQ system and parallel reading in CANDLES experiment

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CANDLES experiment

- Search for Neutrino-less Double Beta Decay (**0**νββ) from **^{48}Ca**

⇒ Violate Lepton number conservation ⇒ **Physics beyond SM**

⇒ Very rare events: $T_{1/2}(^{48}Ca) > 10^{22}$ years *[1]* (not observed yet)

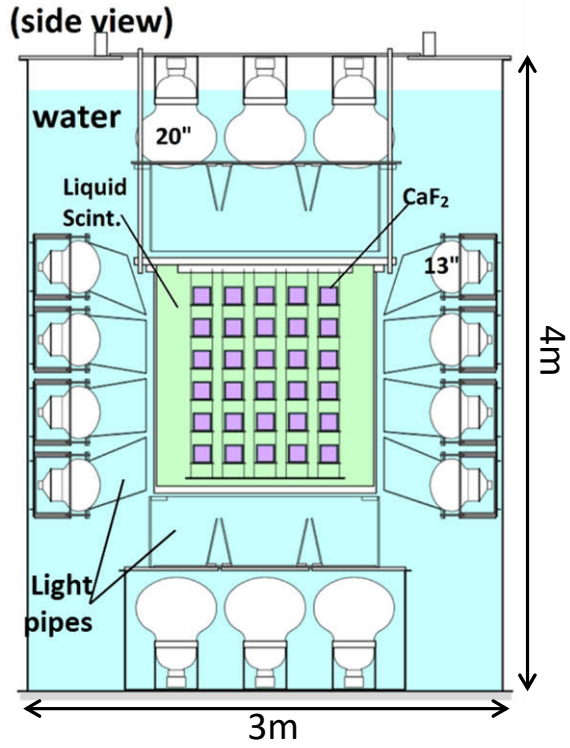
- We need:
  - Large amount of source

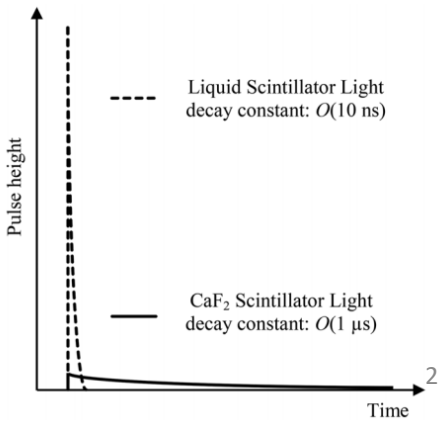
  ⇒ 96 crystals of CaF_2 (detector and source): 300g of ^{48}Ca
  - Low background

  ⇒ Passive shielding: set up at Kamioka (2700m.w.e underground)

  ⇒ 4π active shielding: CaF_2 immerged in Liquid Scintillator (LS)
- Difference in pulse shape: LS (10ns), CaF_2 (1μsec)

  ⇒ ***PSD (Pulse Shape Discrimination) + FADC***
- 62 PMTs surrounding: 48 on side, 14 at top and bottom
- Everything is mounted inside a cylindrical water tank (^{h}4mx$^{\phi}$3m)





[0] CANDLES website: http://www.rcnp.osaka-u.ac.jp/~umehara/Public/index.html?Lang=EN

[1] S. Umehara et al. (2008), Phys. Rev. C 78, 058051.

Requirement for DAQ system

❖ Background near $Q_{\beta\beta}$ of ^{48}Ca:

Most background: removed by active shielding

- ○ 2νββ => need energy resolution
- ○ External background (n,γ) => need passive shielding
- ○ Impurities background:
  - ▪ BiPo ($^{214}Bi \rightarrow ^{214}Po$) sequential decay => need PSD
  - ▪ ^{208}Tl β-decay: remove by tagging preceding α-decay

⇒ **Need small dead-time at 20cps (CANDLES trigger rate)**

⇒ **demand for DAQ**

❖ Waveform: ▪ measured by 500 MHz-8bits FADC

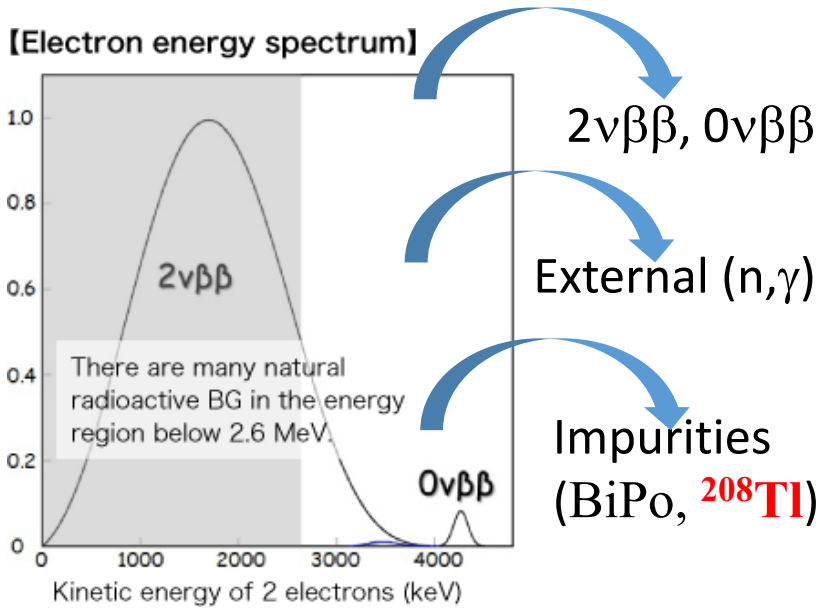
▪ 640Bytes×74Channels(~50kB)

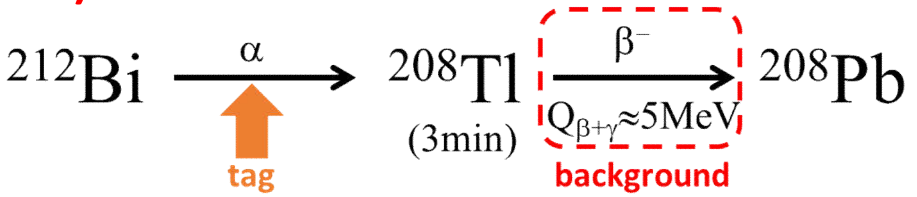
❖ 2006, we started development of FADCs on ATCA

⇒ Ref [2], [3], [4]

❖ 2016, new μTCA DAQ system was introduced

⇒**THIS TALK**





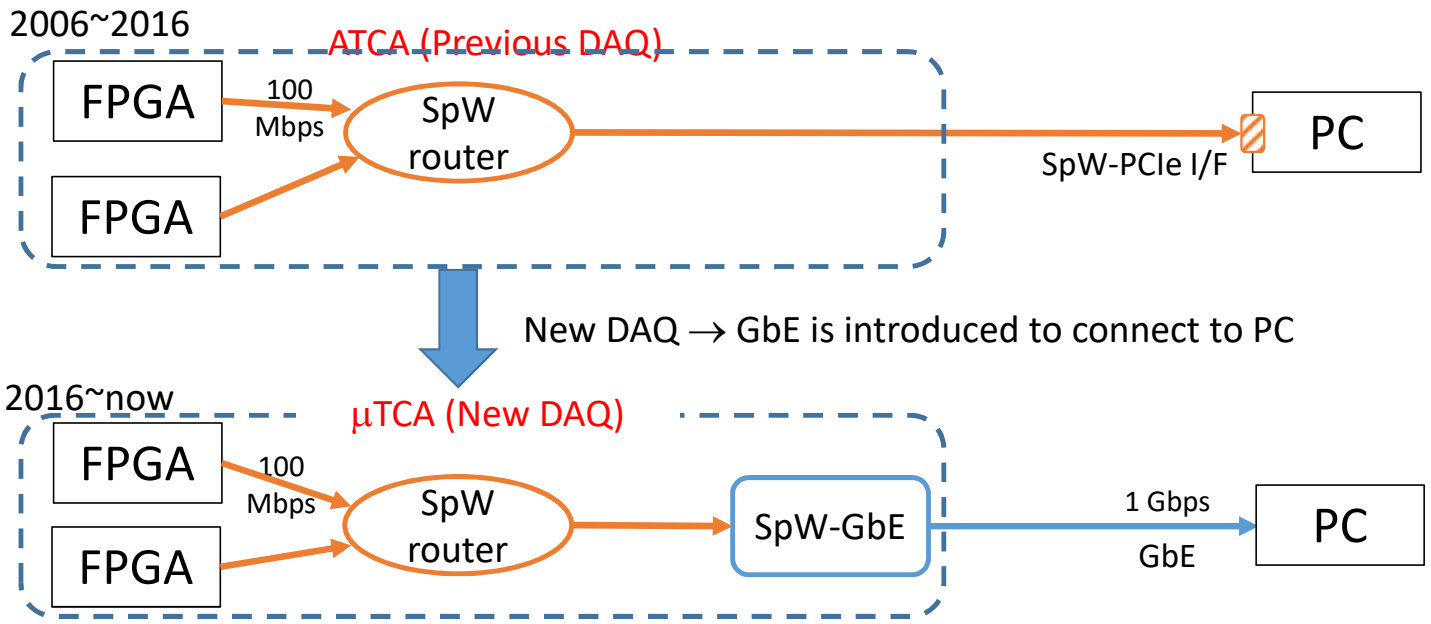
Beta-decays of ^{208}Tl behave as background of CANDLES

[2] Nomachi and Ajimura, IEEE Trans. Nucl. Sci., Vol. 53, No. 5, 2006.
[3] K. Suzuki, Real Time Conference, 2014 (Nara, Japan).
[4] T. Maeda, Real Time Conference, 2014 (Nara, Japan).

SpaceWire network in DAQ system

SpaceWire
- connect sub-systems onboard spacecraft [5]
- developed from DS-links [6]
- 10~200Mbps (100Mbps in CANDLES), bi-directional, full-duplex data
- Point-to-point data links (LVDS) and flexible routing switches

→ Adequate and flexible at FE



❖ **SpW for FADC-to-PC (previous DAQ – ATCA [3])**
- SpW I/F in FPGA
- SpW-to-PCIe I/F in PC
- **Short latency**

❖ **SpW-GbE for FADC-to-PC (new DAQ - μTCA)**
- SpW-GbE converter
- Easy interface to PC
- **High latency**

[3] K. Suzuki, Real Time Conference, 2014 (Nara, Japan).
[6] http://cds.cern.ch/record/363094
[5] http://spacewire.esa.int/content/Standard/Standard.php: SpW is ECSS-E-ST-50-12C

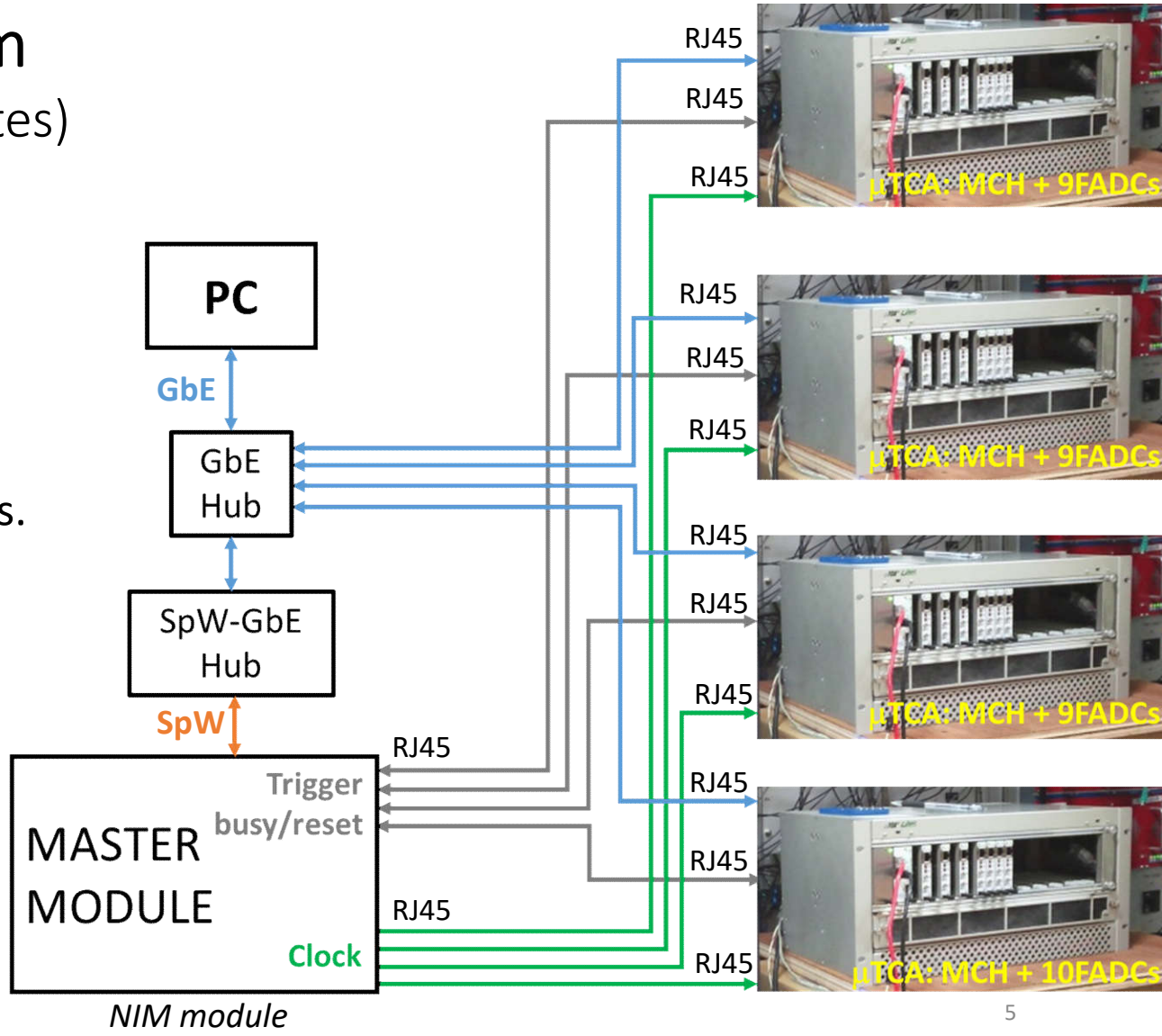
Set up of new DAQ system

(74 channels => divided in 4 crates)

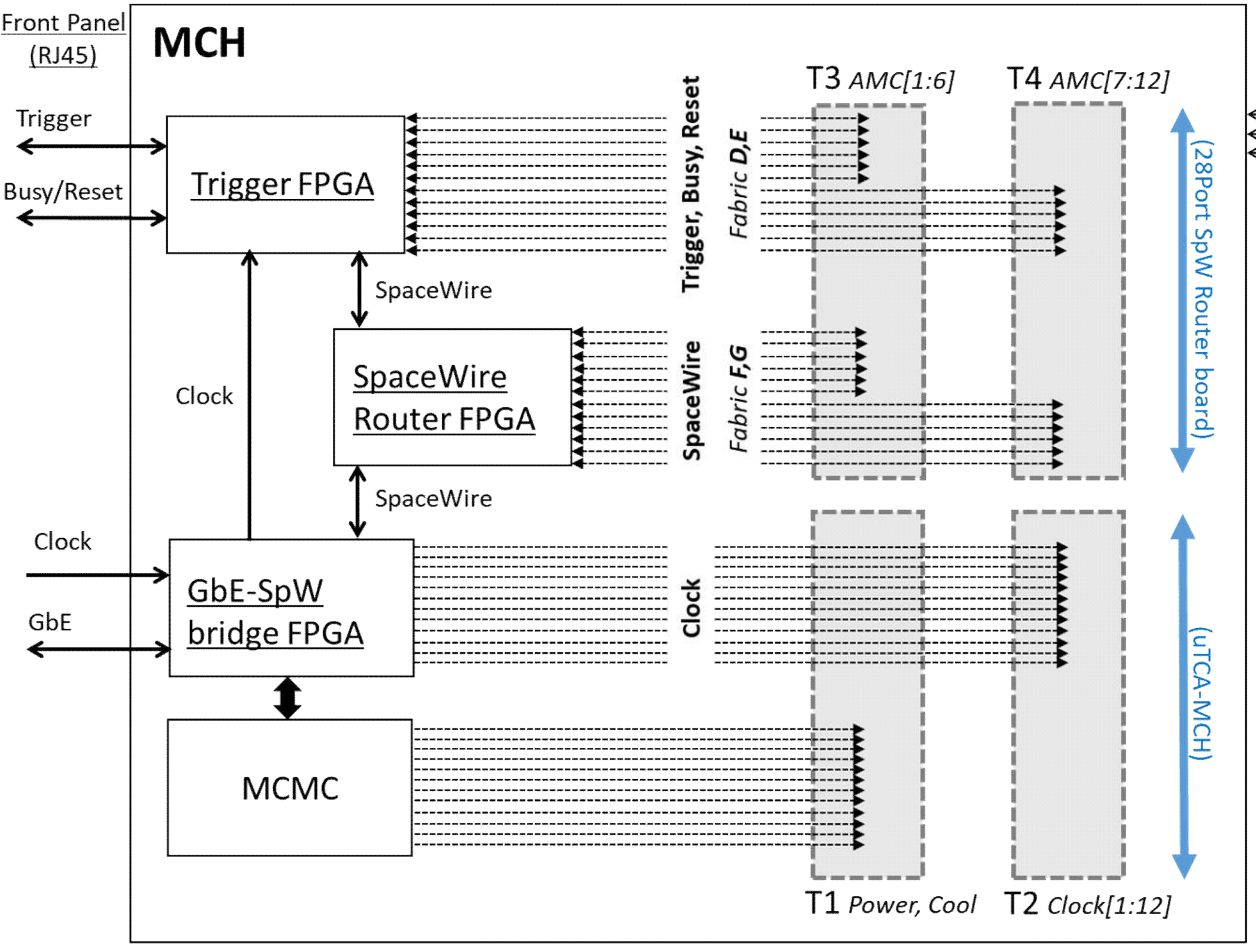
- Each crate: 1 MCH + 9~10 FADCs (2Channels/FADC)
- Master Module
  distributes clock and trigger signals.

- We need:

1.Readout data via SpW/GbE
2.Collect local trigger
  → Broadcast global trigger
3. Clock distribution



Inside MCH: 3 FPGAs (GbE-SpW, Trigger, SpW Router)



Development of MCH:
Cooperation with JAXA[7], Shimafuji[8]

- GbE-SpW bridge FPGA
  - GbE-SpW I/F
  - Common clock (Tongue2)
- Trigger FPGA (trigger/busy/reset)

⇒Receive/distribute trigger/busy/reset from/to FADCs (x12)

⇒Fat pipe 4,5 <-> Fabric D,E (Tongue3,4)
(FADCs) (MCH)

- SpW Router FPGA

⇒Connect Trigger, GbE-SpW, FADCs

⇒Fat pipe 6,7 <-> Fabric F,G (Tongue3,4)
(FADCs) (MCH)

(All 3 FPGAs: Spartan6 XC6SLX100)

[7] JAXA: http://global.jaxa.jp/
[8] Shimafuji: http://www.shimafuji.co.jp/

Data Readout:

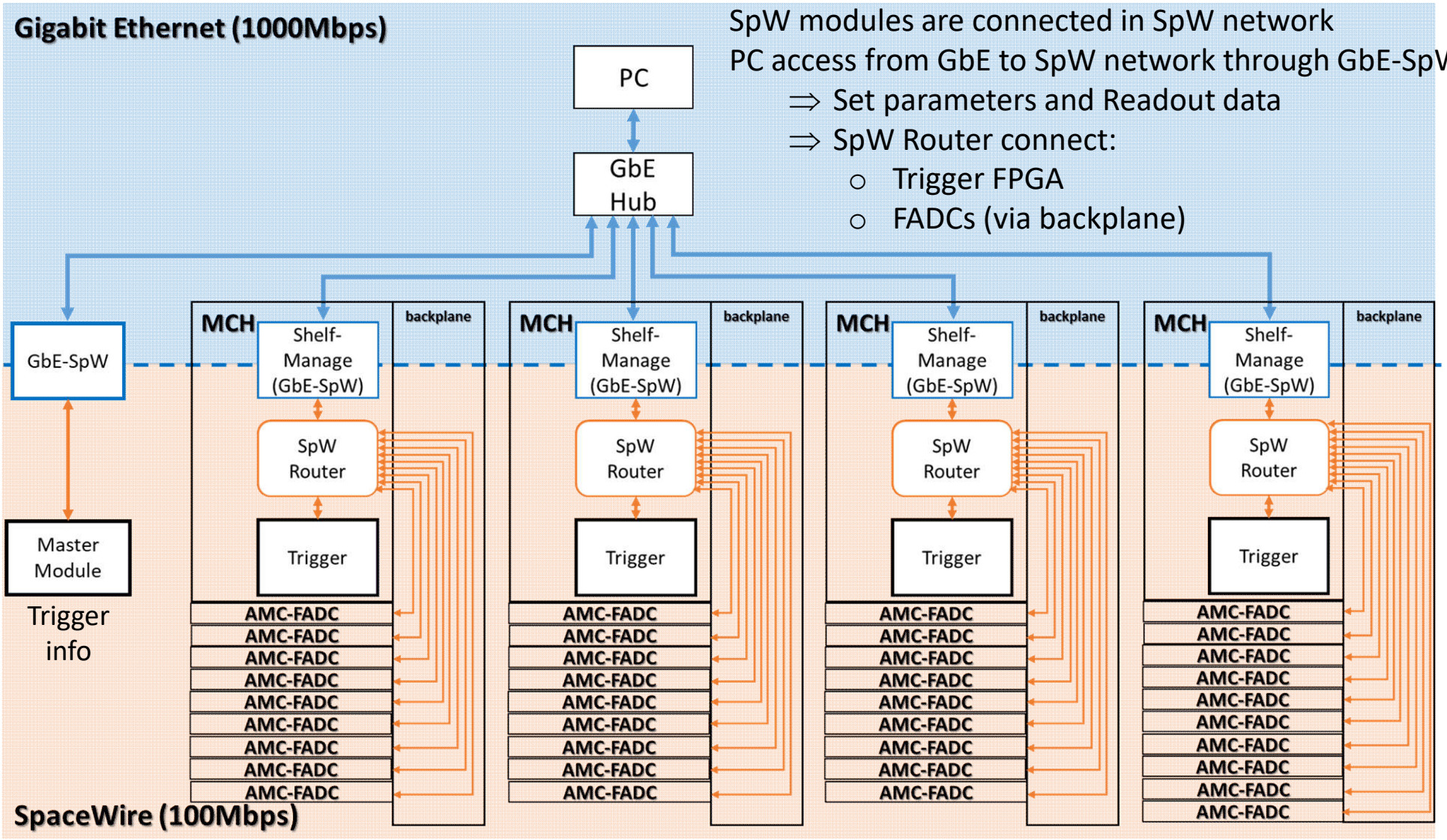
SpW modules are connected in SpW network

PC access from GbE to SpW network through GbE-SpW I/F

⇒ Set parameters and Readout data

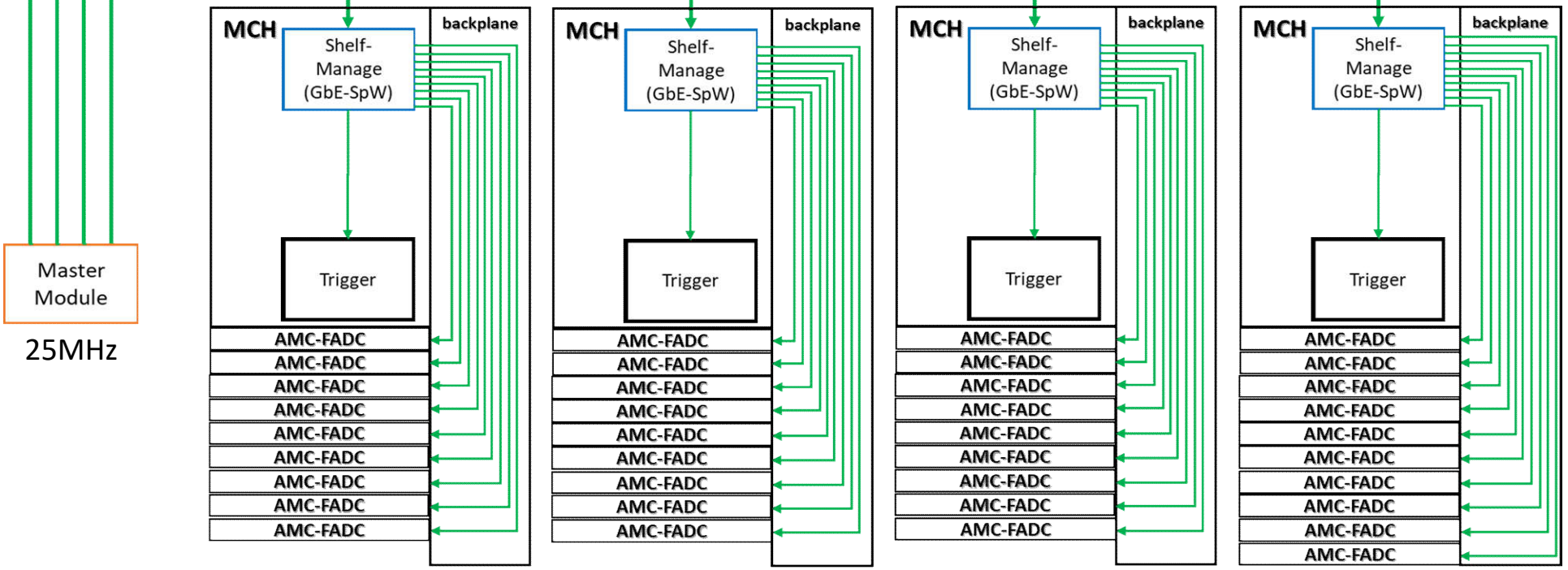
⇒ SpW Router connect:

- Trigger FPGA
- FADCs (via backplane)



Clock Distribution: (25MHz from Master Module)
Clock signals: Master Module → 4 MCHs
MCHs → Trigger and FADCs (via backplane)
In FPGA(*) of FADC(**): PLL 125MHz (Readout buffer)
Clock Synthesizer 500MHz (ADC)

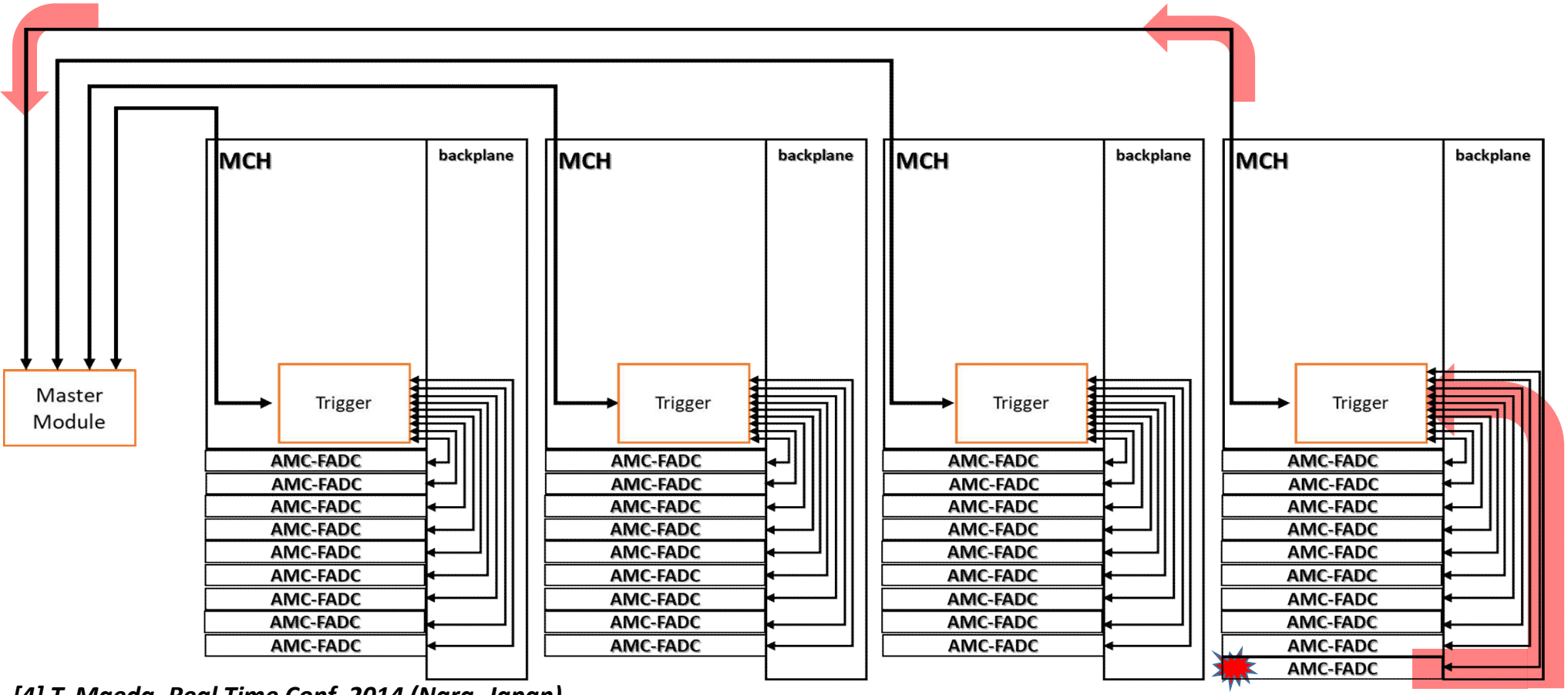
(*) Cyclone 4 EP4CE30; (**) ADC08DL502 (Texas Instrument)



Trigger: select CaF_2 event using Dual Gate trigger[4]

Gather local triggers: FADCs → Trigger → Master Module

Distribute global trigger: Master Module → Trigger → FADCs



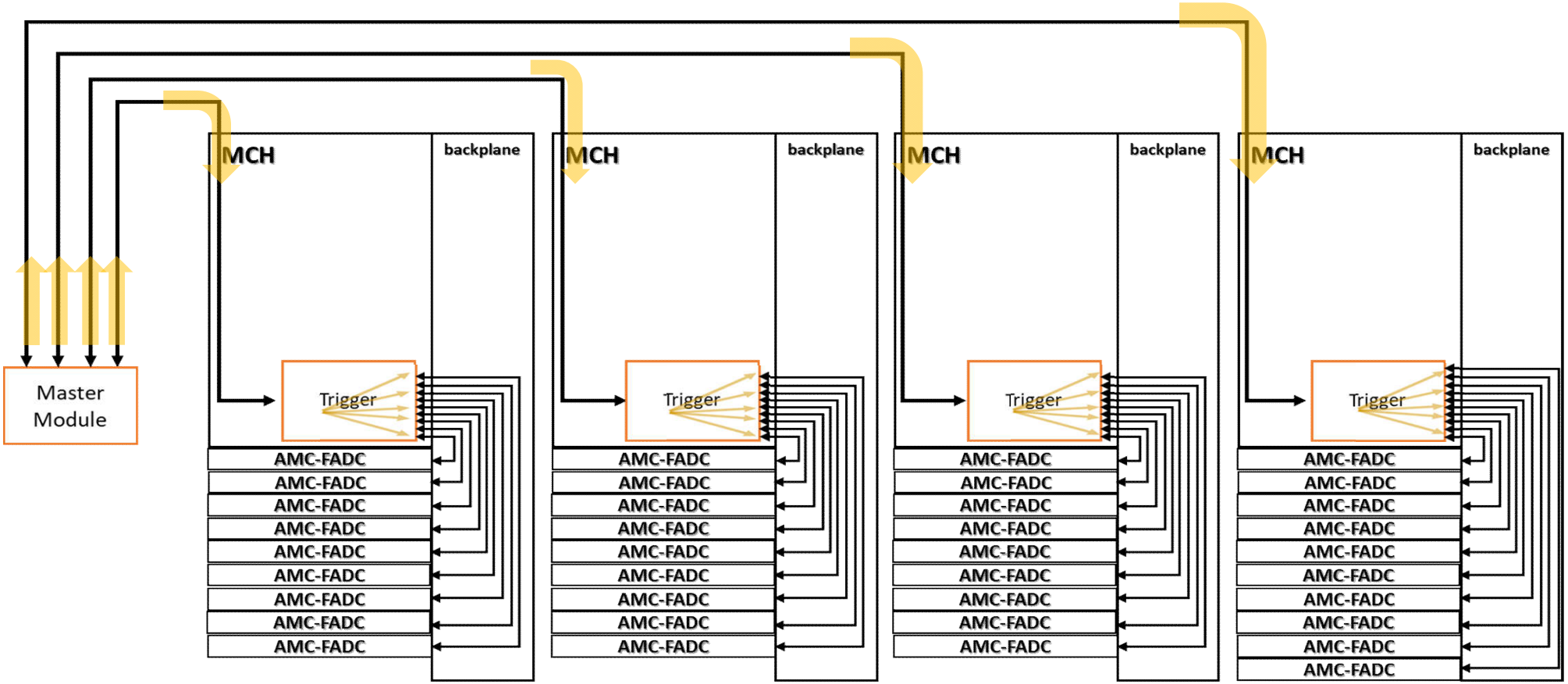
[4] T. Maeda, Real Time Conf. 2014 (Nara, Japan)

Trigger: select CaF_2 event using Dual Gate trigger[4]

Gather local triggers: FADCs → Trigger → Master Module

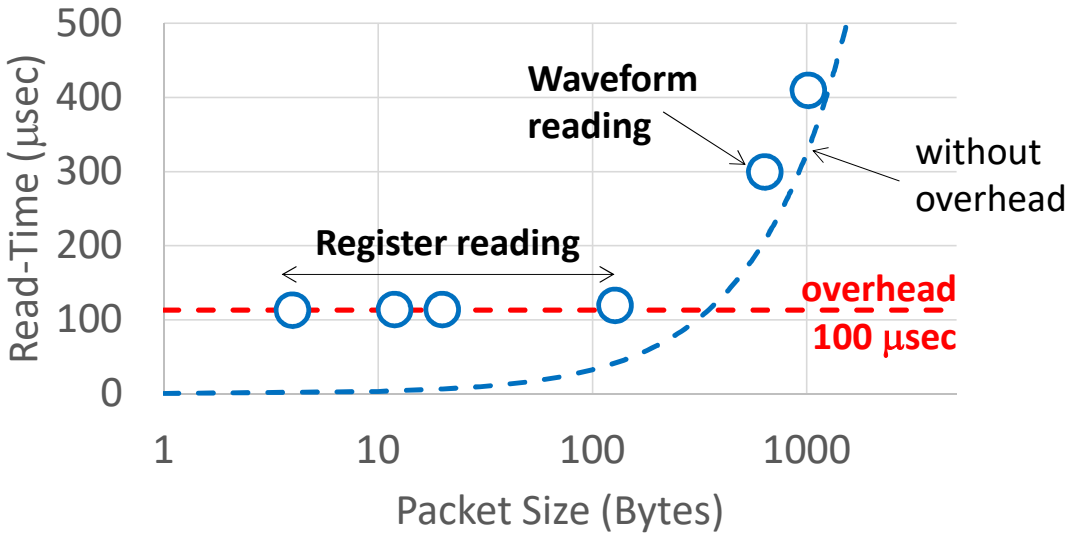
Distribute global trigger: Master Module → Trigger → FADCs

⇒ When global trigger comes, waveform is stored in buffer



[4] T. Maeda, Real Time Conf. 2014 (Nara, Japan)

SpaceWire readout



- SpW with RMAP (Remote Memory Access Protocol [5])
- RMAP: transaction of request and reply
- SpW-GbE: long latency ~100µsec

⇒ Due to long turnaround time

⇒ Utilization is small

⇒ Parallel reading to reduce read-time

⇒ "crate parallel" and "event parallel"

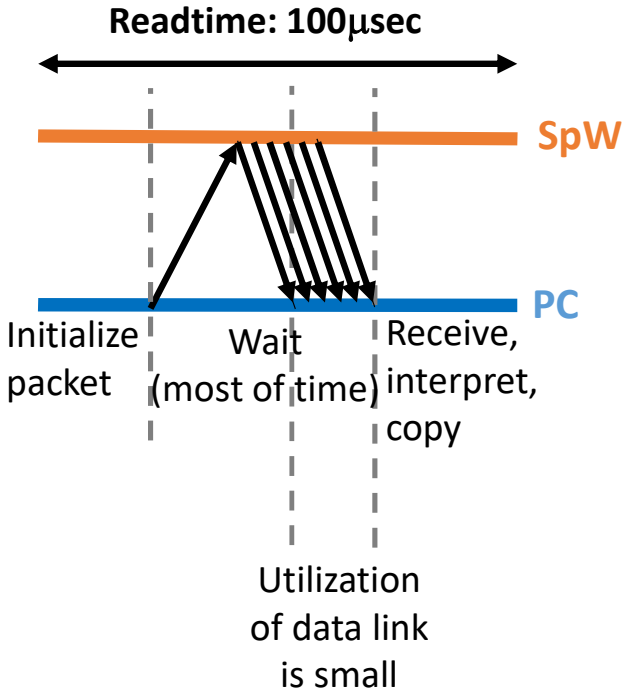
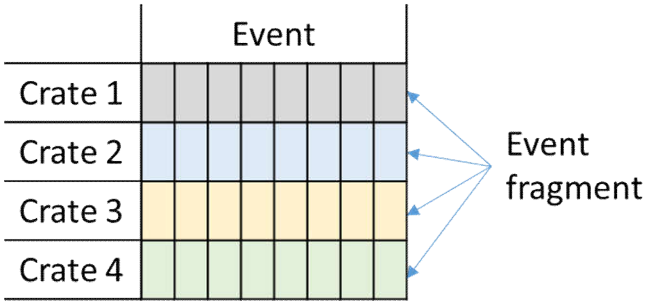


Fig. Read Time in one transaction
Most of time is waiting time.
Utilization if very small

[5] http://spacewire.esa.int/content/Standard/Standard.php: RMAP is ECSS-E-ST-50-52

SpaceWire readout: parallel readout

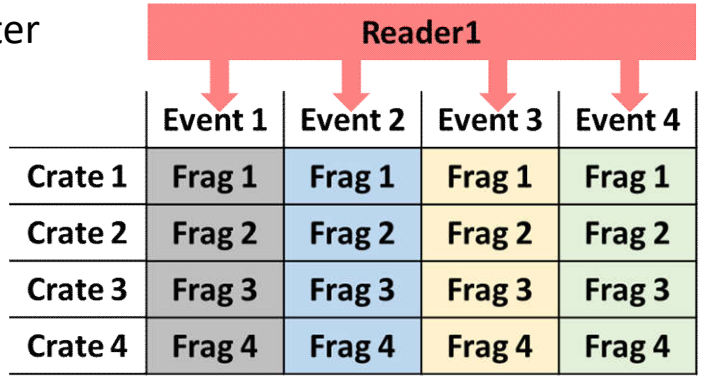
- 74 FADC channels ⇒ 4 crates
- Event fragments in each crate
- With no parallel reading, PC reads all crates one by one (full data set)



With "crate parallel":

- Data in 4 crates are read at the same time

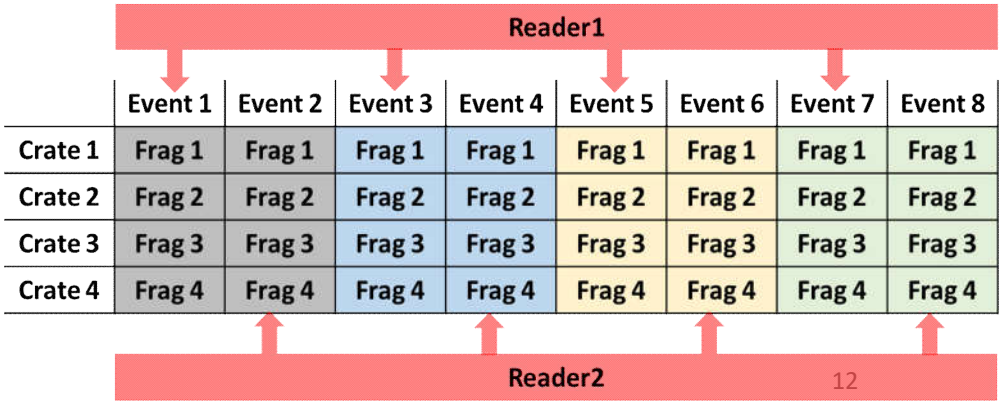
⇒ x4 times faster



With 2 "event parallel":

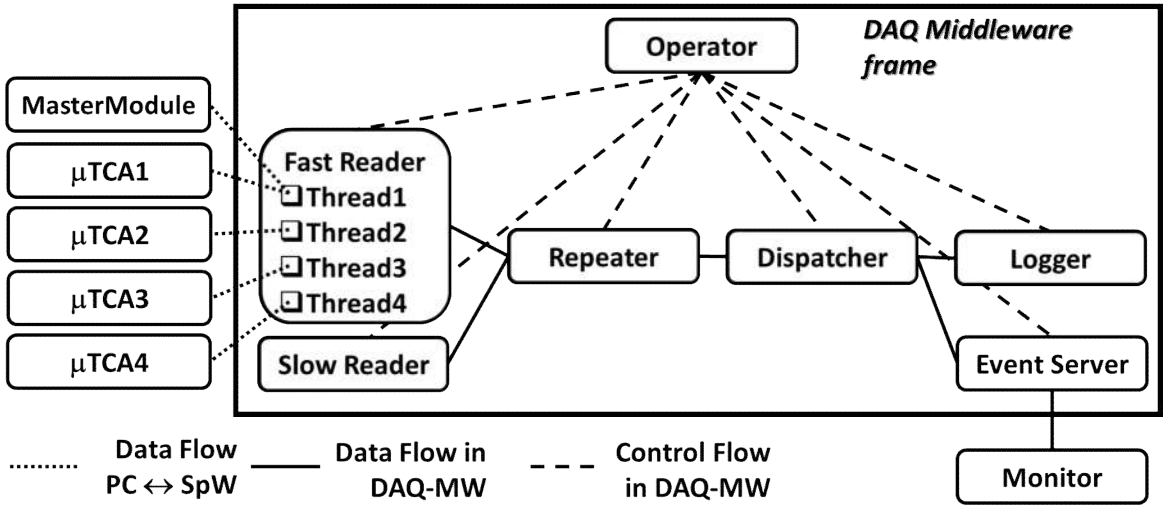
- 2 readers readout events at the same time

⇒ x8 times faster



DAQ-Middleware configuration

- Fast Reader (for FADCs)
- Slow Reader (HV, temperature, etc.)



- In CANDLES, we use DAQ-Middleware framework (by KEK [9]) for DAQ software
- This DAQ software was developed in previous ATCA system [3]

  ⇒ We reused DAQ-MW in this μTCA system

  ⇒ Crate Parallel readout inside Fast Reader
- "Event Builder": not introduced in our DAQ-MW
- With multithread, event building inside Fast Reader.

[3] K. Suzuki, Real Time Conference, 2014 (Nara, Japan).
[9] http://daqmw.kek.jp/

Read-time in parallel readout

Configuration	Read-Time/event (msec)	Data rate* (MB/sec)
1 thread	40.4 ± 3.1	1.23
2 threads	20.2 ± 1.2	2.45
4 threads	10.1 ± 0.6	4.90

* Event data size: ~50kBytes (49.552 kBytes)

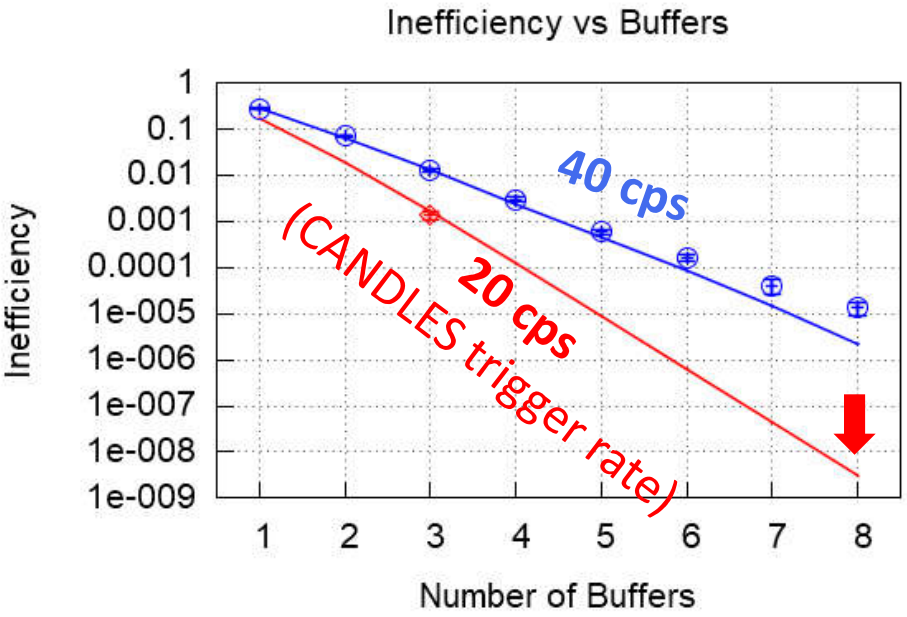
- We configure DAQ-MW to measure with 1, 2, 4 threads to check read time

$\Rightarrow$ Sharing data from all 4 μTCA crates:

  - 1 thread: 1 crate/time
  - 2 threads: 2 crates/time
  - 4 threads: 4 crates/time

- Read-time is reduced x4 times with 4 threads: ~40msec $\rightarrow$ ~10msec

❖DAQ performance with Multiple Buffers



measurement
calculation

For reducing dead-time, we use 8 event buffers as derandomizer.

With read-time/event 10msec, we can calculate inefficiency as a function of event buffer.

For 20cps (CANDLES trigger rate), inefficiency with 8 event buffers is $<10^{-8}$

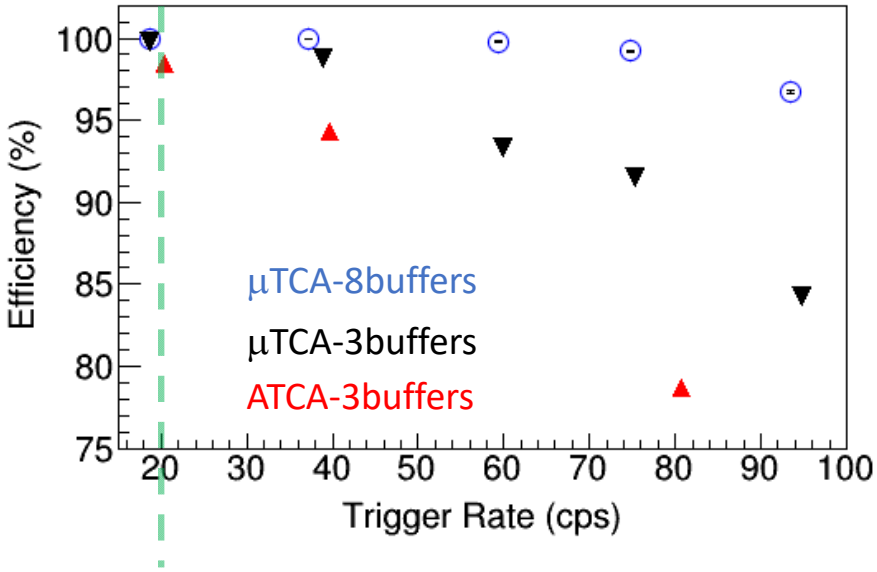
›1 event lost after ~60days to data taking

⇒Too long to measure

- Thus, we calculate and measure at 40cps

⇒ Consistence: data and calculation

❖DAQ performance μTCA



CANDLES trigger rate

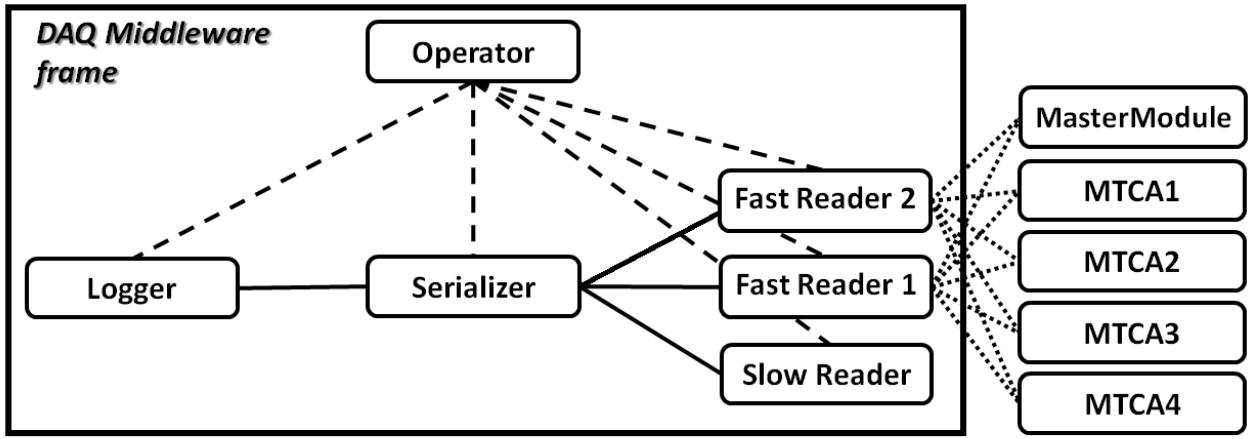
- Check efficiency at different trigger rate
- Parallel readings: 4 threads/1PC
- μTCA: 3 buffers and 8 buffers
- ATCA: 3 buffers (previous DAQ)
- **At 20cps**:

ATCA (3 buffers / 3 PCs)	Efficiency 98%~99%
μTCA (8 buffers / 1 PC)	No event lost after 63hr of data taking [*] ⇒ Inefficiency < 10^{-6}

⇒ **μTCA has *enough performance for CANDLES***

[*] more than 4.2×10^6 events

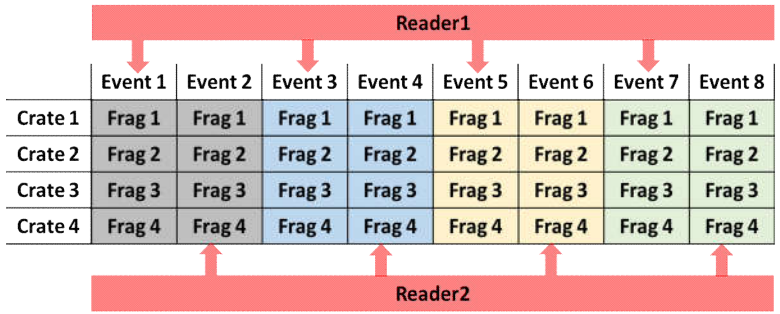
“Event Parallel” for high trigger rate



Control Flow in DAQ-MW

Data Flow in DAQ-MW

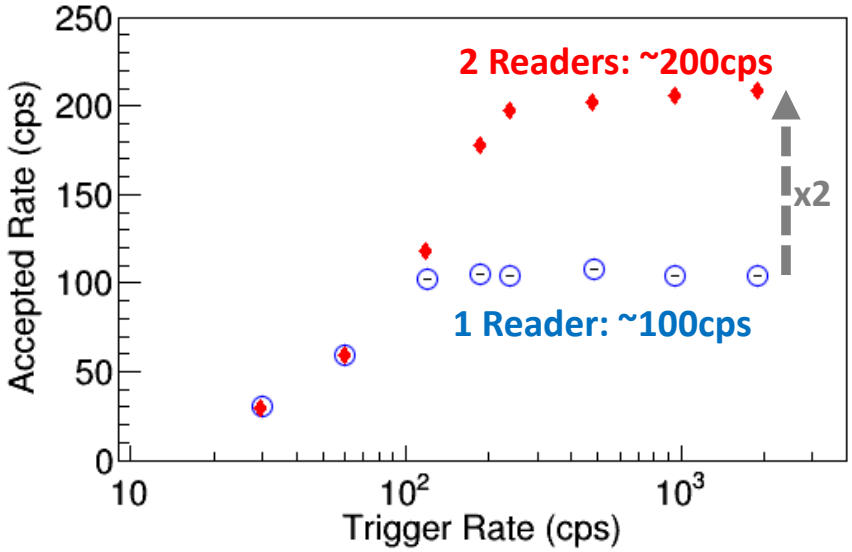
Data Flow PC ↔ SpW



- “Event parallel”: read event in buffers in parallel
  ⇒2 Fast Readers (4 threads/reader) read 8 buffers of all FADCs
  ⇒one for odd buffers and one for even buffers

RI source used in calibration
⇒ High trigger rate (upto a few kHz)
⇒ All buffers are always occupied (event buffers not help)
⇒ Need high throughput
⇒“event parallel” readout is effective

Accepted Rate of “Event Parallel”



- Accepted rate measurement

⇒Changing random trigger rate (30Hz to 2kHz)

⇒Compare 2 (Fast) Readers and 1 (Fast) Readers

- Max Rate (1 Reader): ~100cps
- Max Rate (2 Readers): ~200cps

⇒ x2 times faster

SUMMARY (1)

- New μTCA DAQ is introduced in CANDLES with:
  - New AMC-FADCs: 8 “Event Buffers” to reduce dead-time
  - SpaceWire-to-GigabitEthernet (SpW-GbE) network
- SpW-GbE network has overhead due to software

  ⇒We handle it with parallel readout
- Module parallel with multiple threads is introduced

  ⇒4 threads: **read-time reduced 4 times** (~40msec down to ~10msec)
- Inefficiency(at 20cps – CANDLES trigger rate) is < 10^{-6} from experiment data.

  ⇒In our estimation, we can achieve <10^{-8} (~60days of measurement)

SUMMARY (2)

- At high trigger rate: event buffers are always occupied

$\Rightarrow$ Need high throughput (instead of event buffers)

$\Rightarrow$ “Event parallel” can increase the throughput

$\Rightarrow$ Set up 2 Readers reading 8 event buffers

$\Rightarrow$ accepted rate is increased x2 times (100cps -> 200cps)

THANK YOU FOR YOUR ATTENTION