FPGA Based Pico-second Time Measurement System for a DIRC-like TOF Detector

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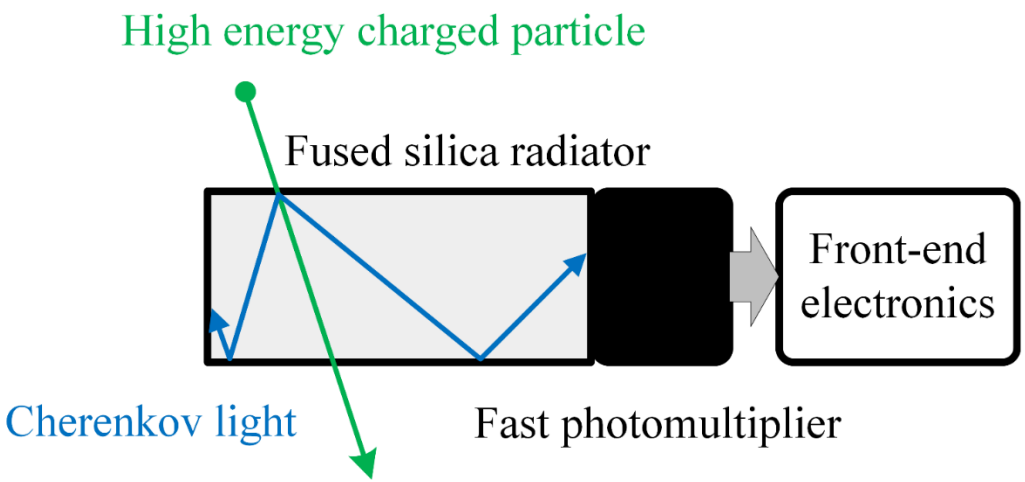
DIRC-like TOF Detector



Challenges:

High timing resolution

Multi-channel integration

DIRC-like TOF Detector

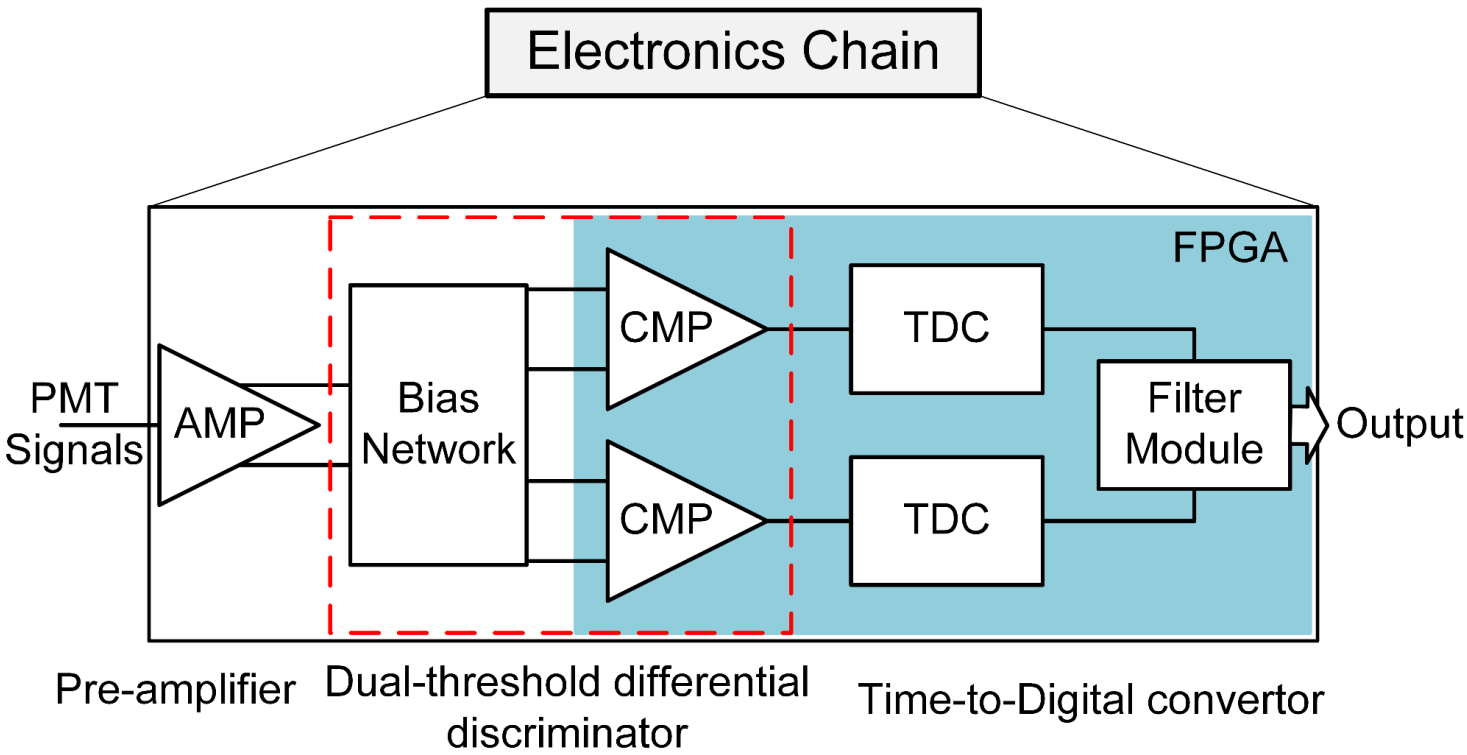
Constant-fraction discriminator

- ✓ Small amplitude time-walk
- × Complex realization circuit
- × Parameters depend on signal waveform

Waveform sampling

- ✓ Reconstruct and analyze the signal shape
- × High sampling rate ADC
- × Complex data interface

Pico-second time measurement system



Pre-amplifier

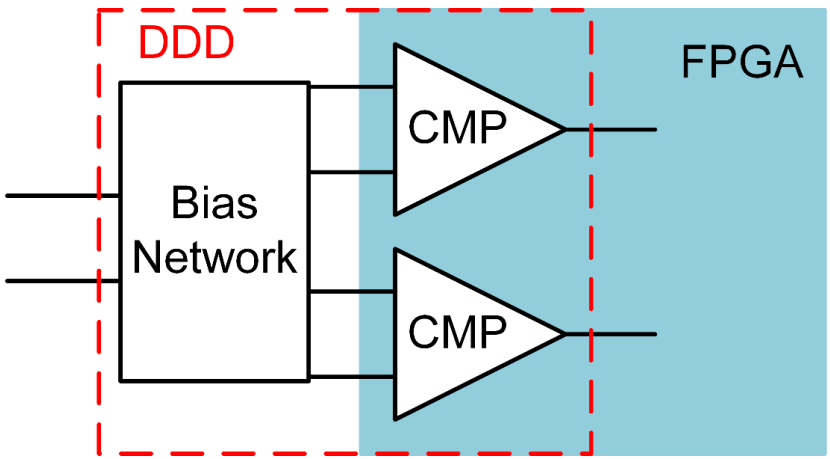
- Amplify signal from MCP-PMT
- Convert single-end input to differential output

LMH6882 from TI

- Dual channel Differential amplifier
- High bandwidth 2.4GHz for $2V_{PPD}$ output
- Programmable voltage gain from 6 dB to 26 dB

Picture is from http://www.ti.com/product/lmh6882/description

Dual-threshold differential discriminator (DDD)

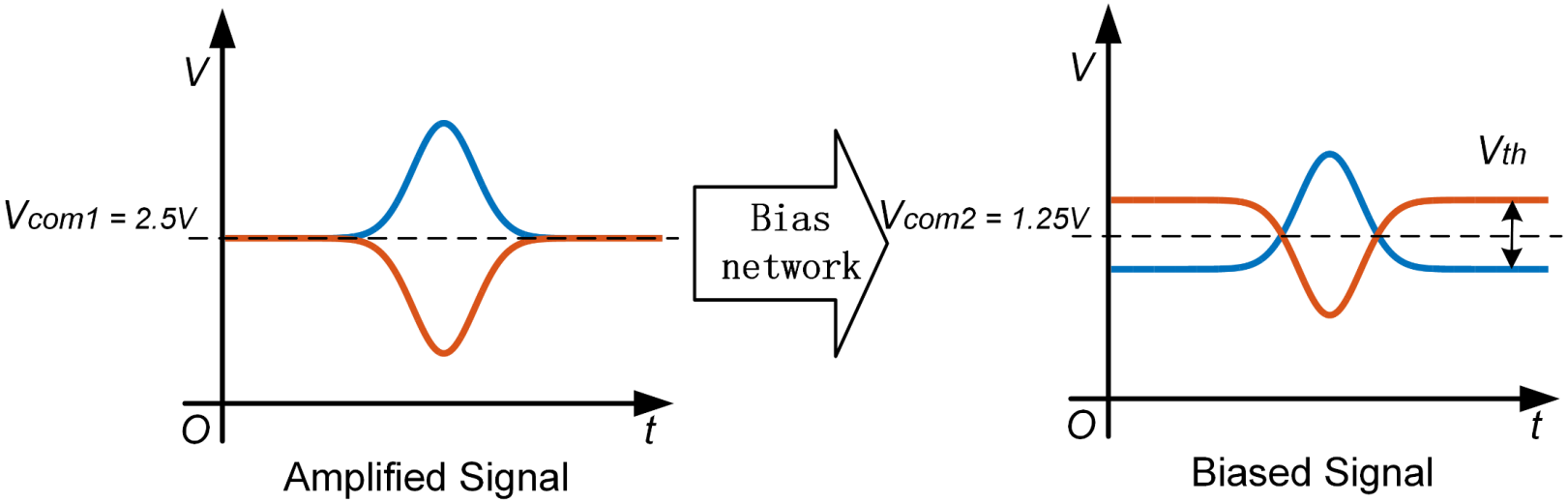


Differential comparator is based on LVDS receiver in FPGA.

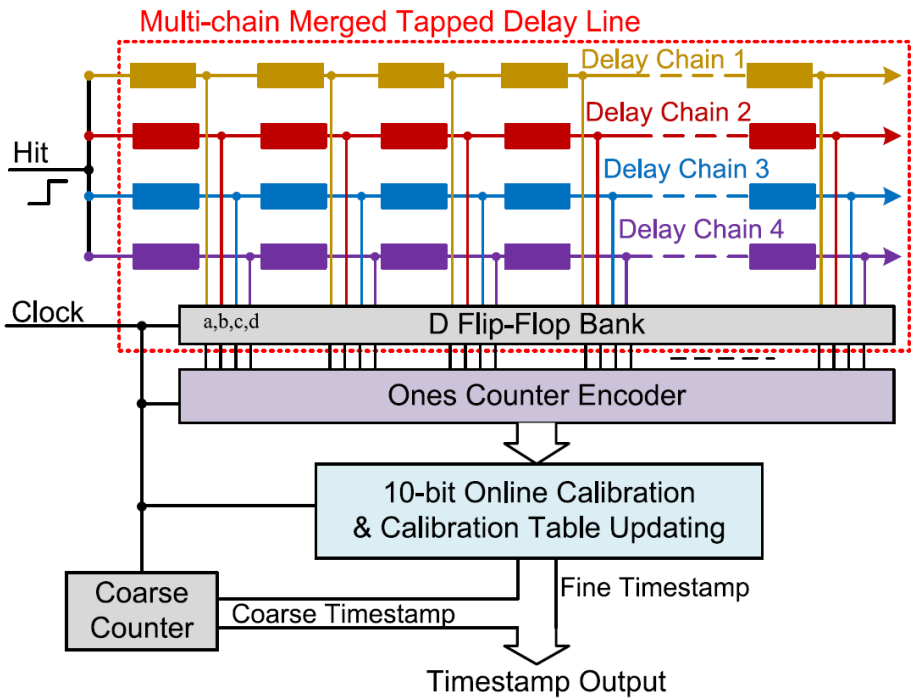
Bias Network is composed of resistors and capacitors.

- Change common-mode voltage
- Provide threshold voltage
- Feed the signal into two discriminator

Dual-threshold differential discriminator (DDD)



FPGA-based Time-to-digital convertor (TDC)



Coarse counter generates the coarse timestamp.

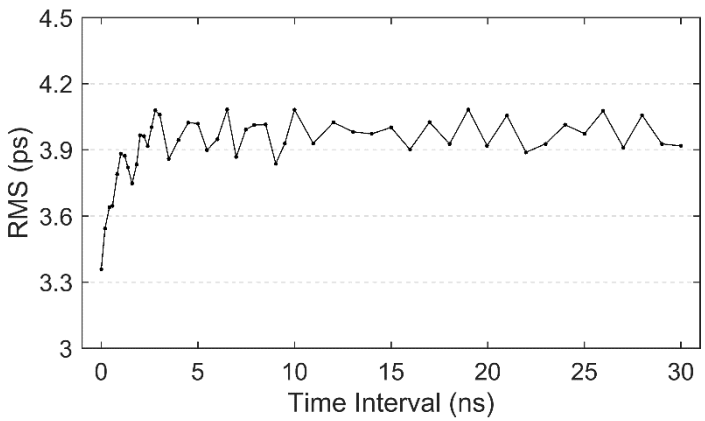
Multi-chain merged TDL transmits the hit signal for time interpolation.

Encoder and calibration table convert TDL output into fine timestamp.

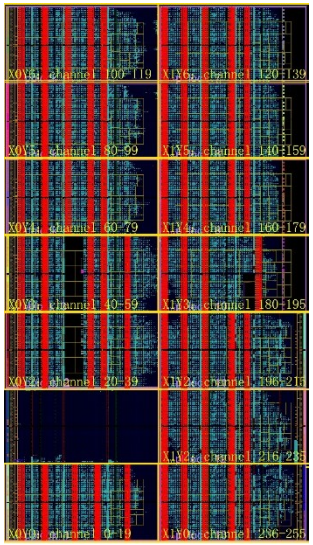
Y. Wang, J. Kuang, C. Liu, and Q. Cao. "A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA." *IEEE Transactions on Nuclear Science* 64.10 (2017): 2713-2718.

Advantages of FPGA-based TDC

- High performance



- High integration



4-chain TDL TDC average time precision is 3.94ps.

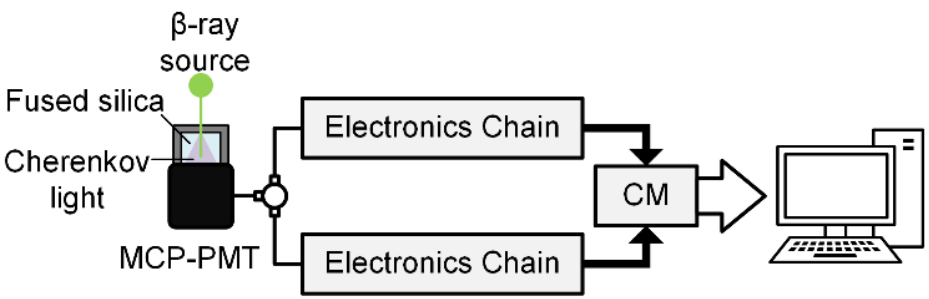
256-channel TDC in one Kintex-7 FPGA.

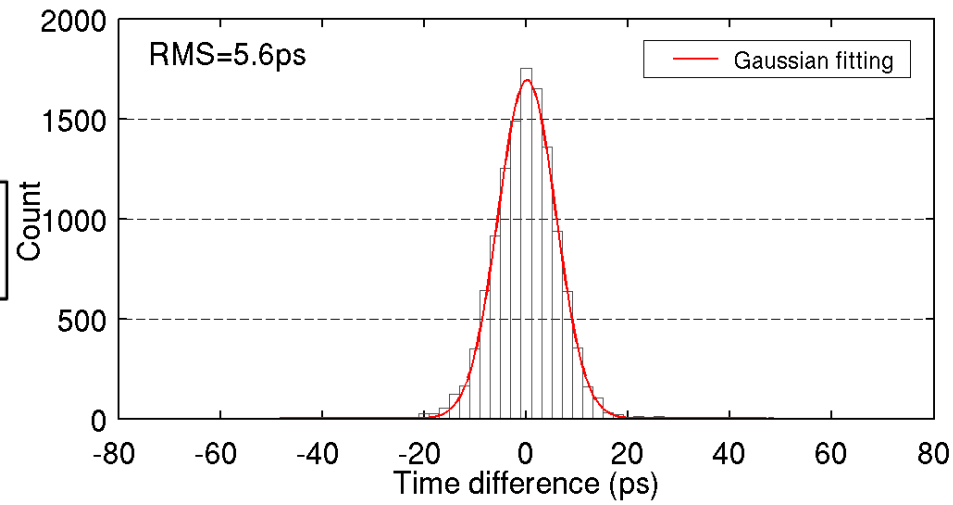
Y. Wang, J. Kuang, C. Liu, and Q. Cao. "A 3.9-ps RMS Precision Time-to-Digital Converter Using Ones-Counter Encoding Scheme in a Kintex-7 FPGA." *IEEE Transactions on Nuclear Science* 64.10 (2017): 2713-2718.

Z. Song, Y. Wang, and J. Kuang. "A 256-channel, high throughput and precision time-to-digital converter with a decomposition encoding scheme in a Kintex-7 FPGA." Journal of Instrumentation 13, no. 05 (2018): P05012.

Electronics Performance Test

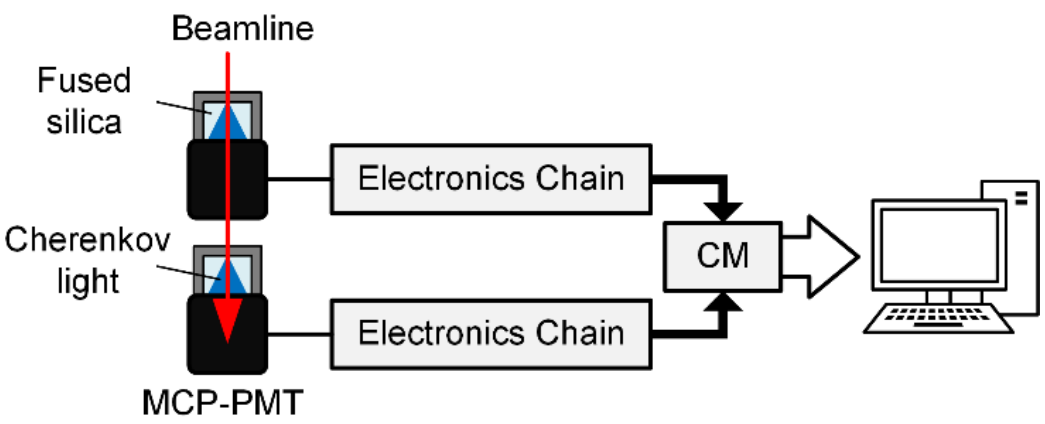
Radiator : JC-H02 fused silica 15 mm × 15 mm × 20 mm
MCP-PMT: Hamamatsu R3809U

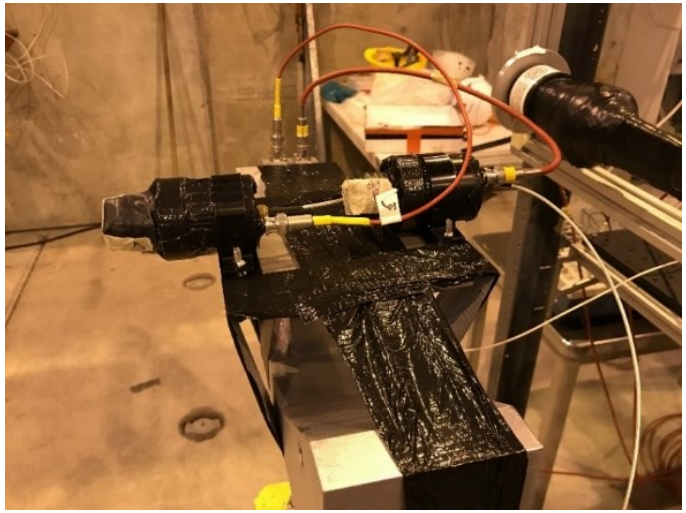




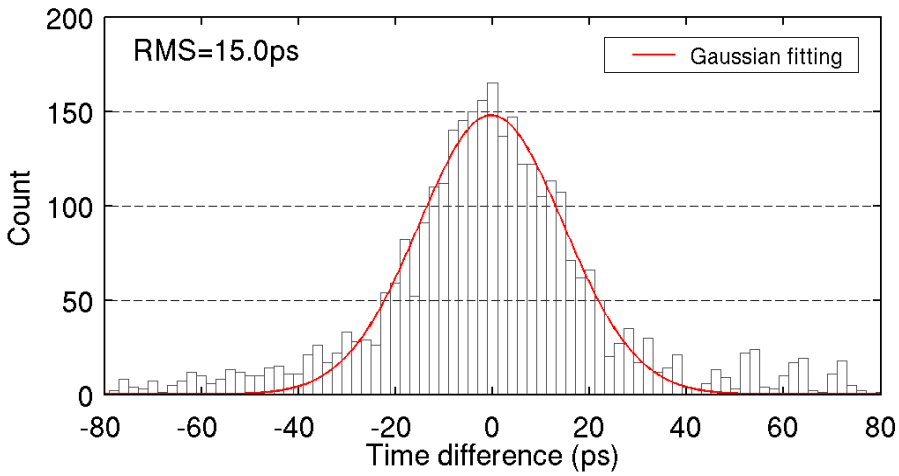
Beam Test

The beam test was in H4 (150 GeV/c, Muon) at CERN.





Beam Test Result



The size of test beam was wide.

Dual threshold values were not optimized.

Conclusion

- FPGA-based differential comparator and TDC can minimize the number of components that shows great potential in applications for multi-channel integration.

- Electronic performance test result shows that the electronics scheme has excellent time performance.

Acknowledgement

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Thanks!